

FPGAs: More than you really wanted to know

“Desktop publishing” ... but for logic



30-NOV-2011

Who is this guy?

- **Steve Knapp**

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- 408-627-7771

- **Addicted to programmable logic since 1985**

- Intel, Xilinx, Triscend (purchased by Xilinx)
- Field application engineer
- Design tool developer
- Intellectual property core developer
- Customer

General Agenda

- **What is an FPGA?**
- **How do FPGAs differ from other chips?**
- **Buzzwords, talking the talk**
- **Who uses FPGAs?**
- **Why do companies use FPGAs?**
- **Who makes FPGAs and related device?**
- **A quick survey of devices**
- **How do companies develop FPGAs?**
- **Creating an application**
- **Pre-canned functions (IP cores)**
- **Making sure it works**
- **Debugging**
- **Programming**

Are there any topics you want to add or emphasize?

Producing a Blockbuster



- **Requirements**
 - High volume
 - Affordable
 - Timely

Book Production Costs

Fixed Costs

- **Labor**
 - Author
 - Editor
 - Graphics Designer
 - Illustrator
 - Production Designer
 - Copy checker
- **Imaged printing plates**
- **Facilities**
 - High-volume printing facility

Variable Costs

- **Paper**
 - So cheap that it practically grows on trees!
- **Printing**
 - Black and white
 - Color
- **Binding**

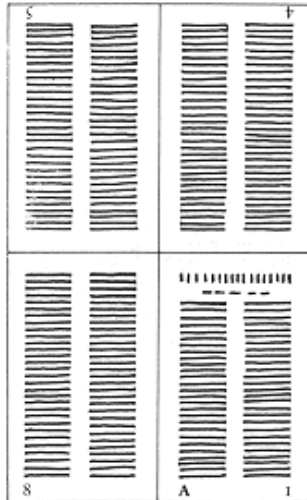
High-Volume Printing

- **Lowest unit cost**
- **BIG fixed infrastructure costs**
- **Set up costs per job**
- **Costs amortized (spread) across all units**

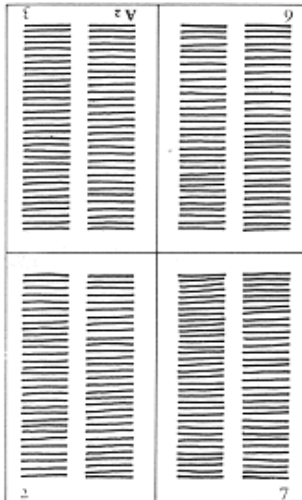


Printing Multiple Images

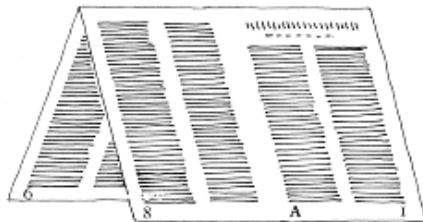
Quarto front



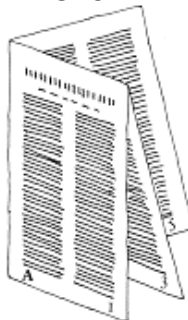
Quarto back



Fold



Fold

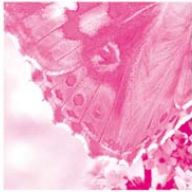


- **Multiple pages printed as a *signature sheet***
 - 4 pages (quarto)
 - 8 pages (octavo)
 - 16 pages (16mo)
- **Folded signatures assembled into book**

Costs Increase per Color



CYAN



MAGENTA



YELLOW

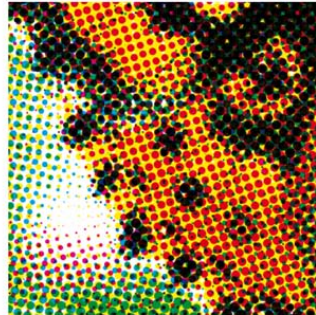


BLACK

- **Lowest cost is one color**
- **Full color costs more**
 - Cyan
 - Megenta
 - Yellow
 - Black
- **Specialty items**
 - Varnish (sheen)
 - Leafing (metallic lustre)
 - Foil stamping
 - Die cut

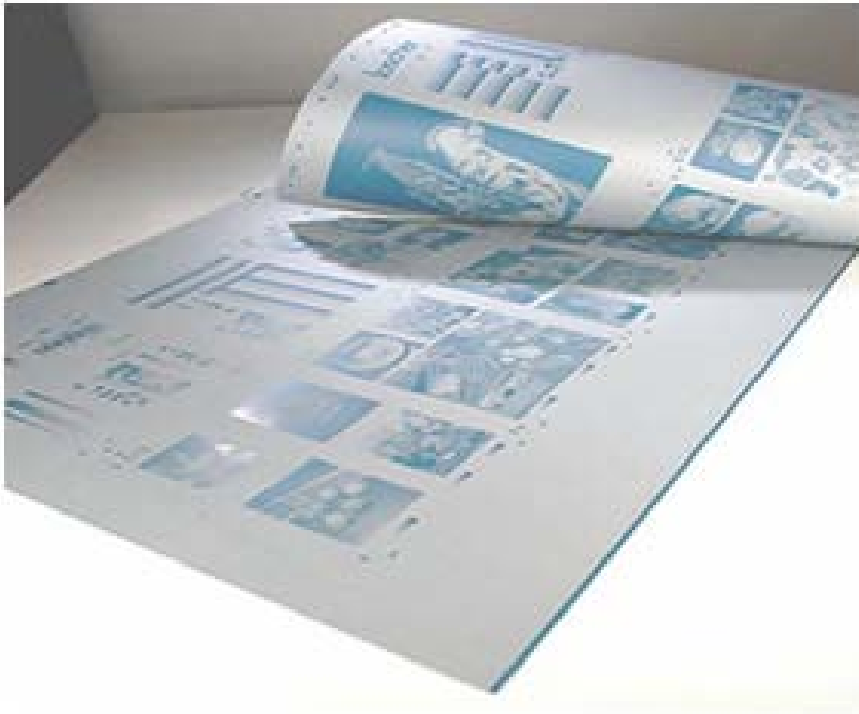


FINAL CMYK



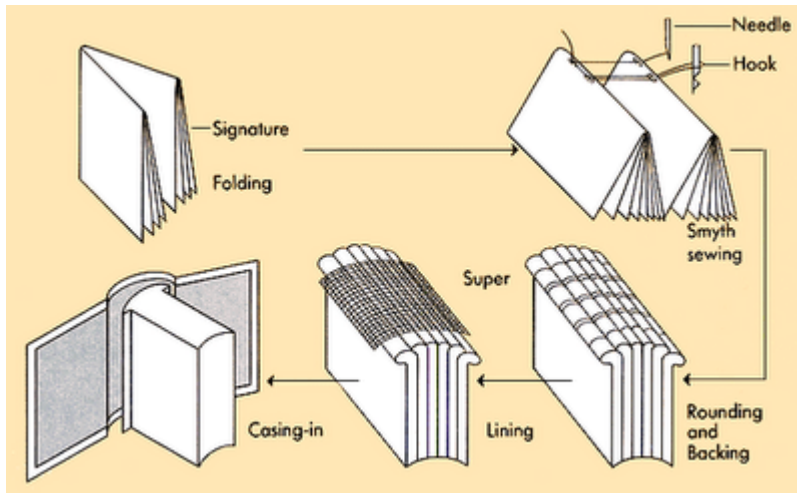
DETAIL VIEW

Offset Printing Imaged Plates



- **One plate per color, per signature**
 - A significant up-front investment
- **Cost and time of developing the plates makes offset printing less desirable for small production runs**

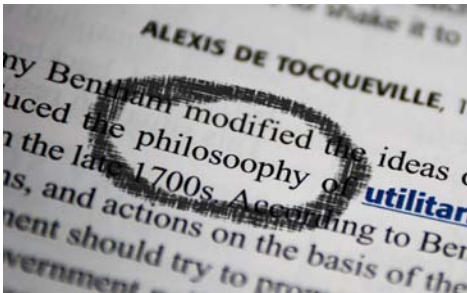
Packaging



- **Hardcover**
 - Dustcover
 - Embossing
 - Cases
- **Paperback**
 - Saddle stitching
 - Perfect binding
 - VeloBind
 - Spiral
 - Comb

What Could Go Wornng?

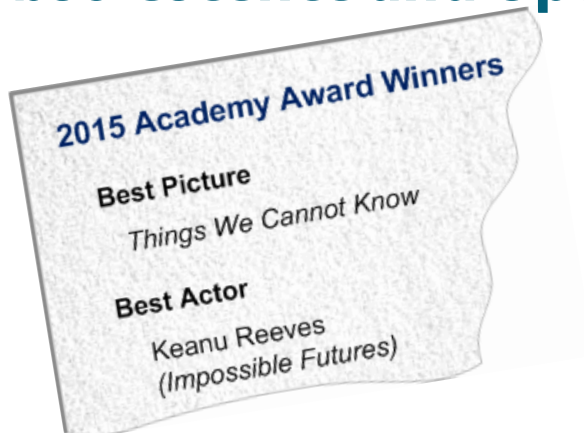
Product Flaws



Not Enough Volume to Justify Production

- Like this presentation!

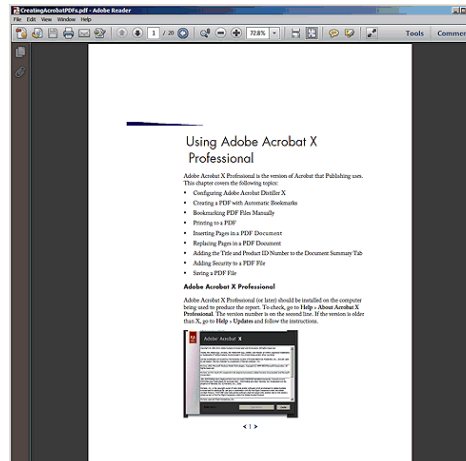
Obsolescence and Updates



Customer Customization

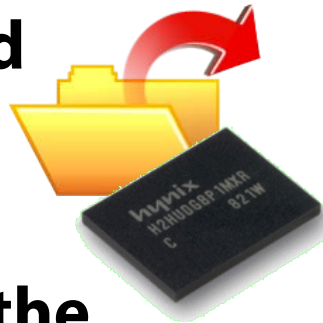


Solutions to the Problem

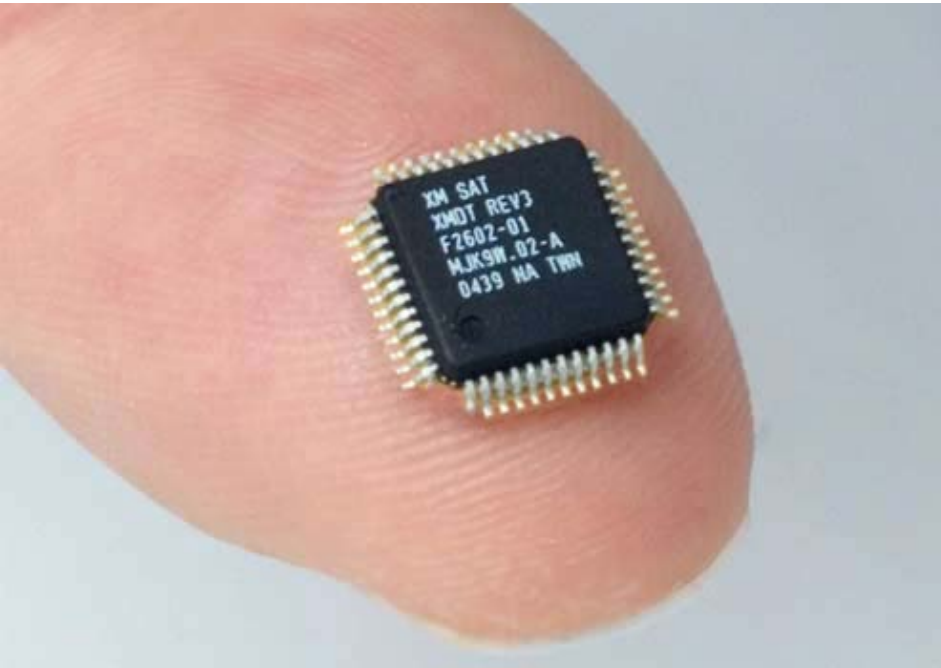


eBook Reader Business Model

- Reader costs more than most high-volume paper books
- Content downloaded and saved into nonvolatile memory
- eBook reader reads the nonvolatile memory to display the “application”
- Easy and timely updates



Producing a Blockbuster Chip



- **Requirements**
 - High volume
 - Affordable
 - Timely

Chip Production Costs

Fixed Costs

- **Labor**
 - Architect
 - Design engineer
 - Verification engineer **S**
 - Test engineer
 - Packaging engineer
 - Process engineer
 - Manufacturing engineer
- **Mask Sets**
- **Facilities**
 - High-volume fabrication facility

Variable Costs

- **Silicon**
- **Processing**
 - Number of layers
 - Exotic processes
- **Packaging**

High-Volume Fabrication

- **Multi-BILLION dollar facility**
- **Costs amortized (spread) across all units**



Raw Materials

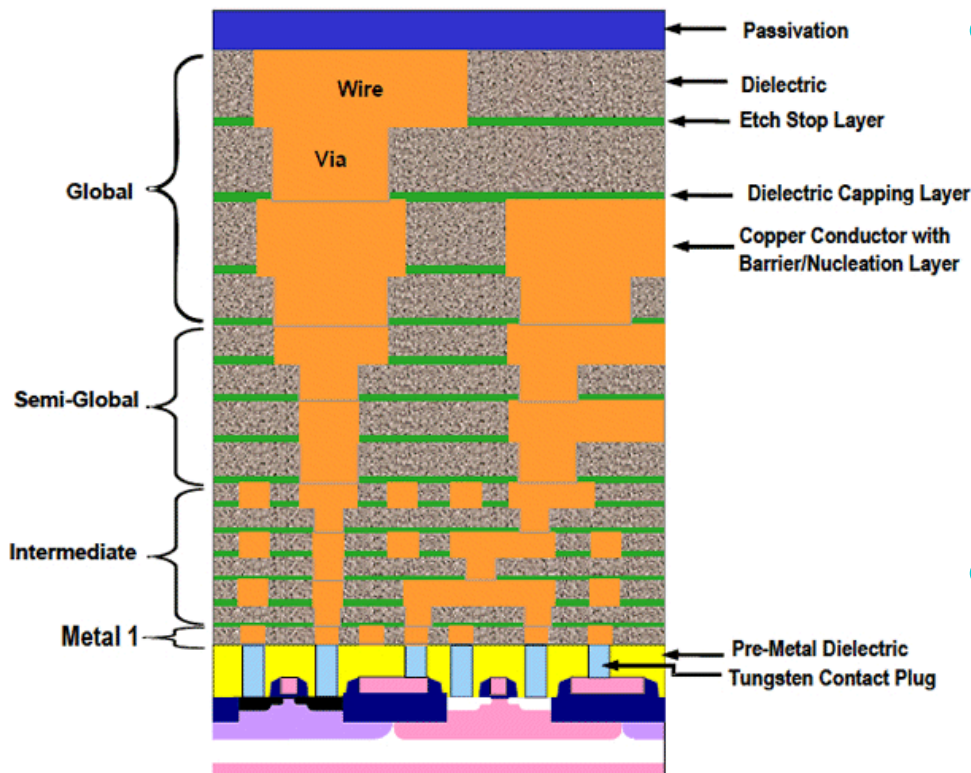
- So cheap, we let kids play with it



- Silicon extracted from sand or quartz
- Highly purified
- Grown as ingots
- Sliced into wafers

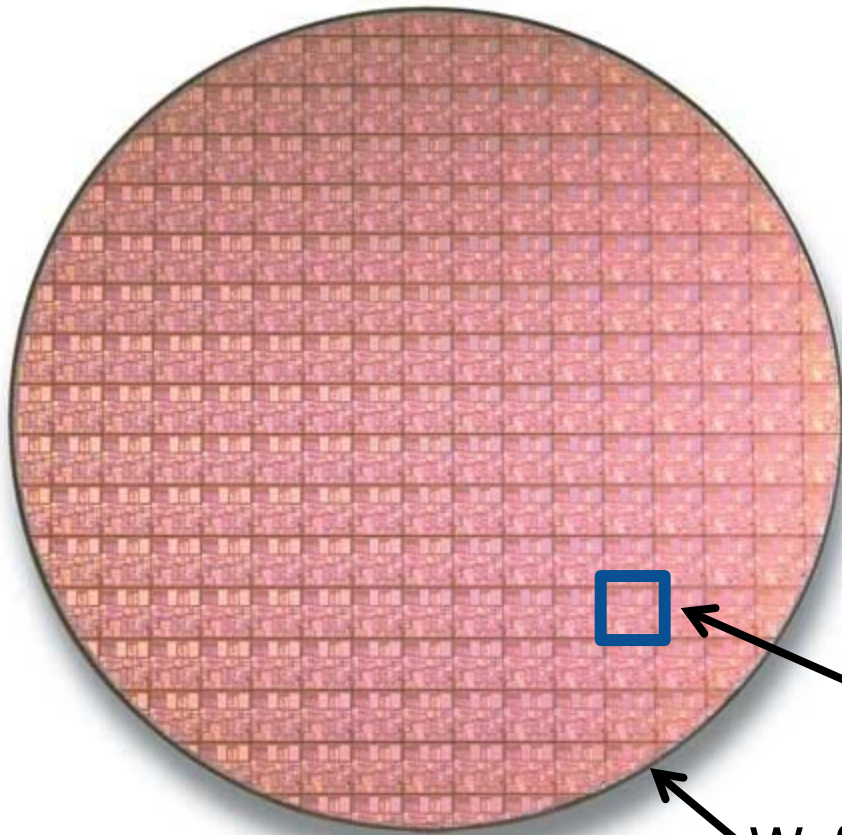


Costs Increase per Layer

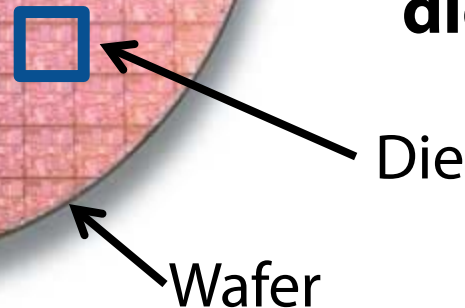


- **All semiconductor devices require multiple process layers**
 - Transistors
 - Multiple layers of metal
 - Dielectric
- **Specialty processes**
 - Floating gate
 - Anti-fuse

Printing Multiple Images



- **A chip (die) is printed multiple times on each silicon wafer**
- **Each layer aligned and printed**
- **Sawed into individual die later**

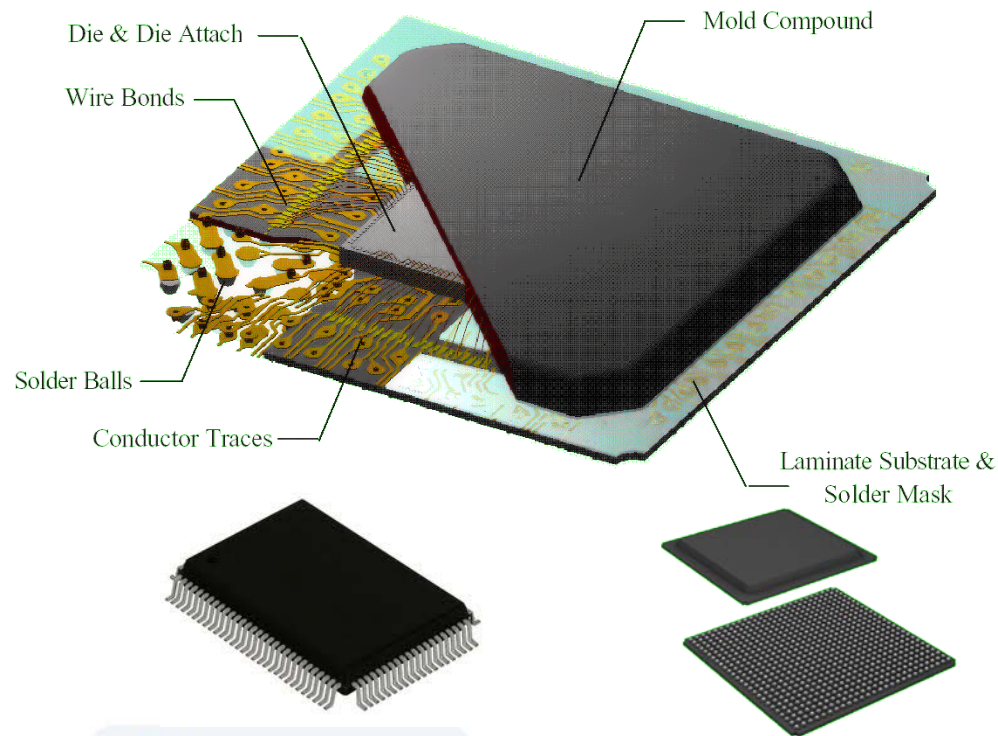


Photomask set



- **One per layer**
 - A significant up-front investment
 - Can cost millions of dollars for leading-edge processes
- **Cost and time of developing the masks makes small production runs less desirable (more expensive)**

Packaging



- Tens to thousands of connections
- Through-hole or surface mount
- With or without leads
- Ball Grid Arrays
- Multi-chip stacked die
- No package at all (raw die)

DiePlus™											
CS36	CS63	CC72	CS110	CB81	CB121	QN84	CB132	CB196	CB284	VQ100	
.4 mm pitch	.4 mm pitch	.5 mm pitch	.4 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	.5 mm pitch	
2.5 X 2.5 mm	3 X 4 mm	4 X 5 mm	4 X 5 mm	5 x 5 mm	6 X 6 mm	7 X 7 mm	8 X 8 mm	8 X 8 mm	12 X 12 mm	14 X 14 mm	

What Could Go Worng?

Design Flaws



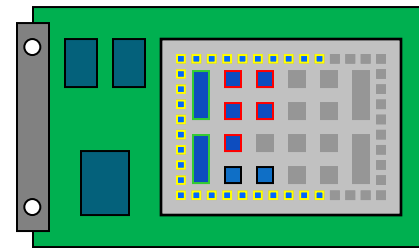
Not Enough Volume to Justify Production



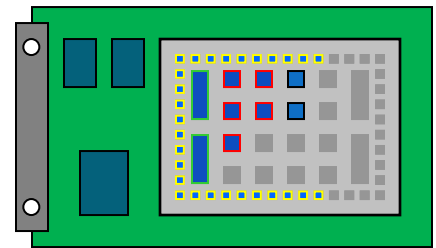
Obsolescence and Updates

NEW
IMPROVED! **4D TV!**

Customer Customization



Customer A



Customer B

Prevailing
Technology

Custom Products

All layers
customized

One layer
customized

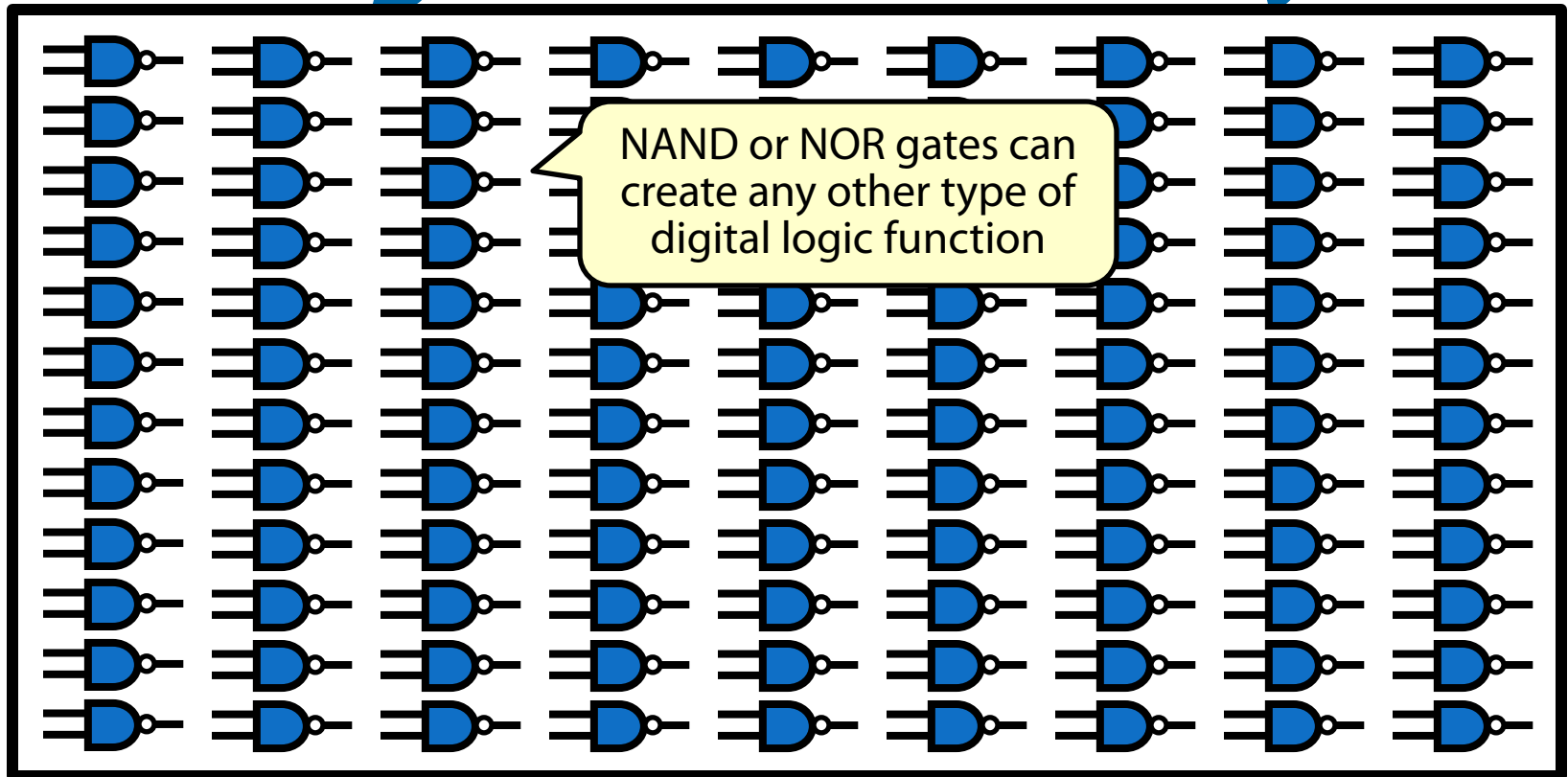
Full Custom

Standard
Cell

Gate Array

Structured
ASIC

The Original "Gate Array"

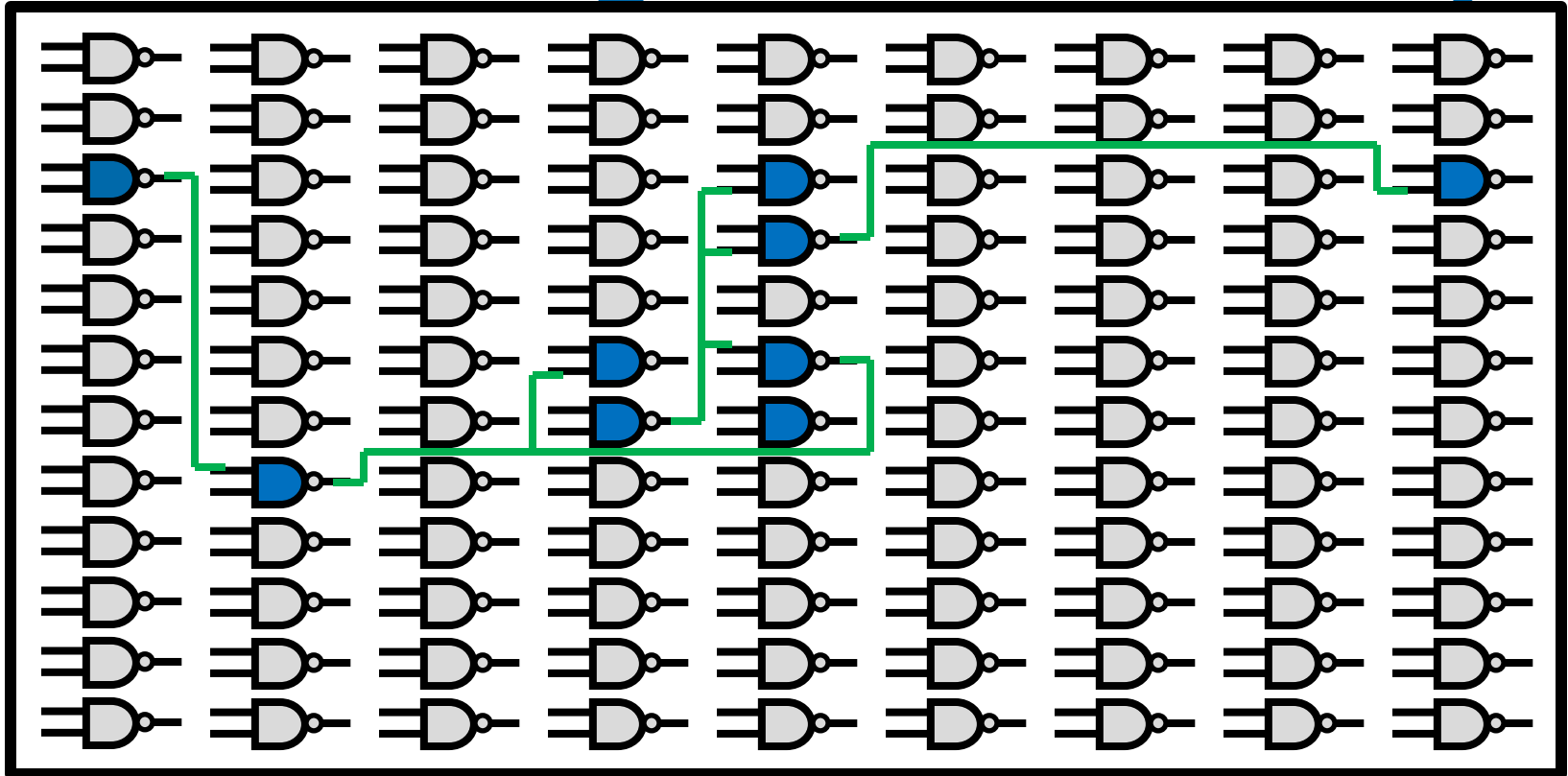


Final metal layer(s) added later

Build all but final metal layer(s)

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Customizing the Gate Array

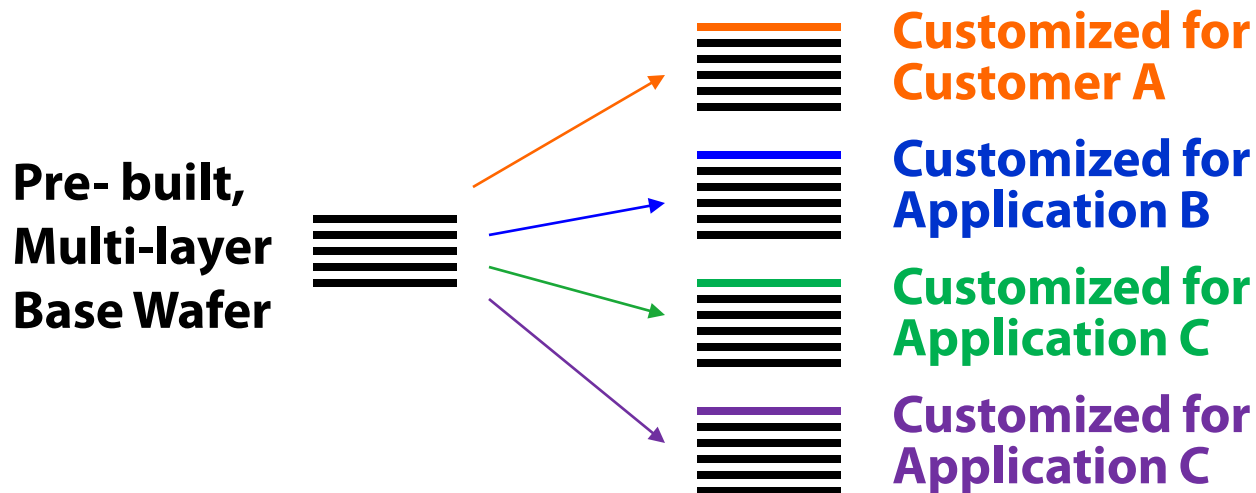


Final metal layer(s) are user-customized mask set(s)

Pre-built layers

Application Specific ICs (ASIC)

- **Customize the application with just one mask layer**
 - Greatly reduced mask costs
 - Weeks to months of turn-around time



Gate Array Implications

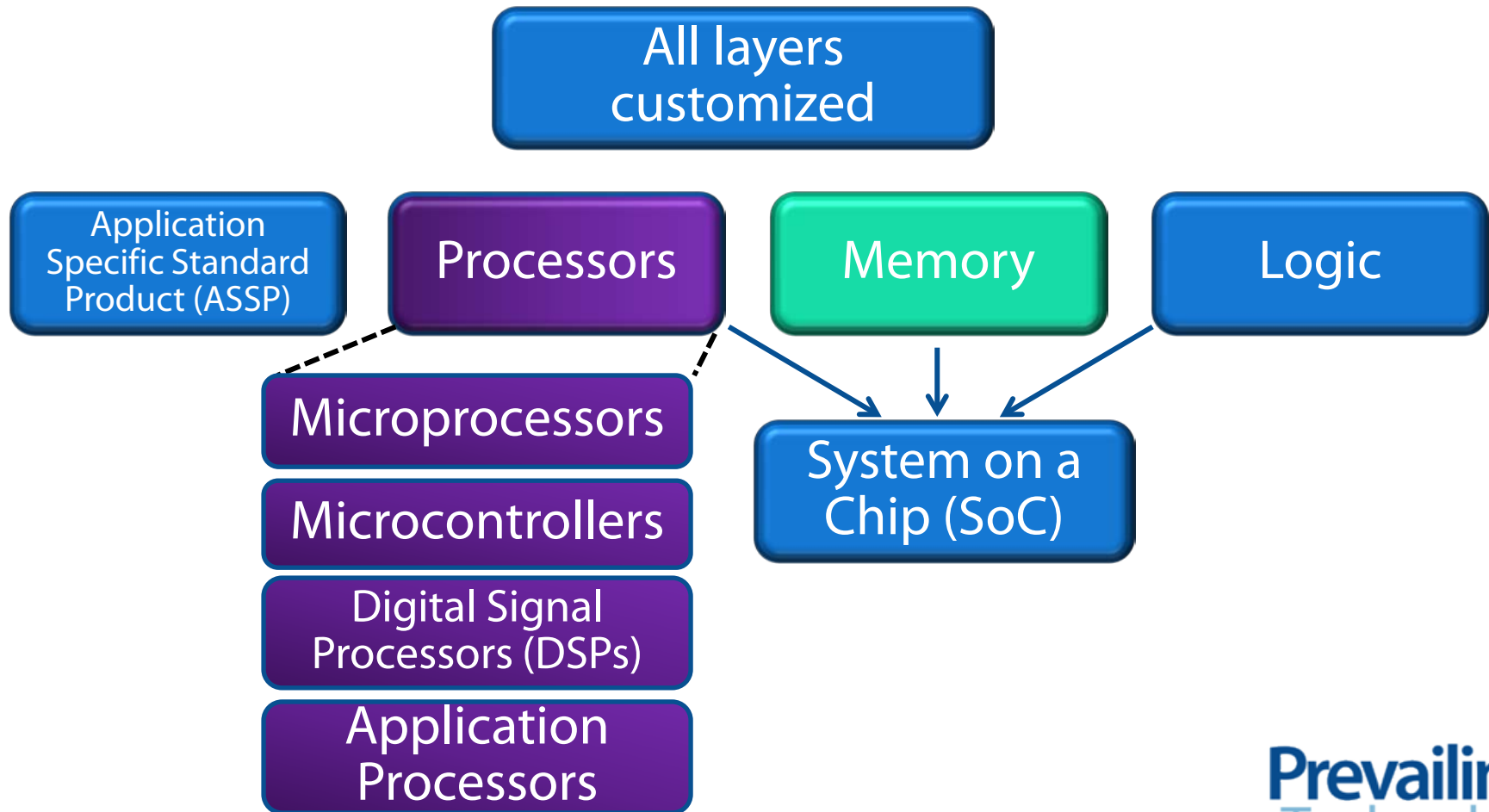
- **Customized mask**

- Non-recurring engineering (NRE) costs
- Manufacturing lead times
- Additional verification effort
- Test program for custom device
- Inventory costs and risks

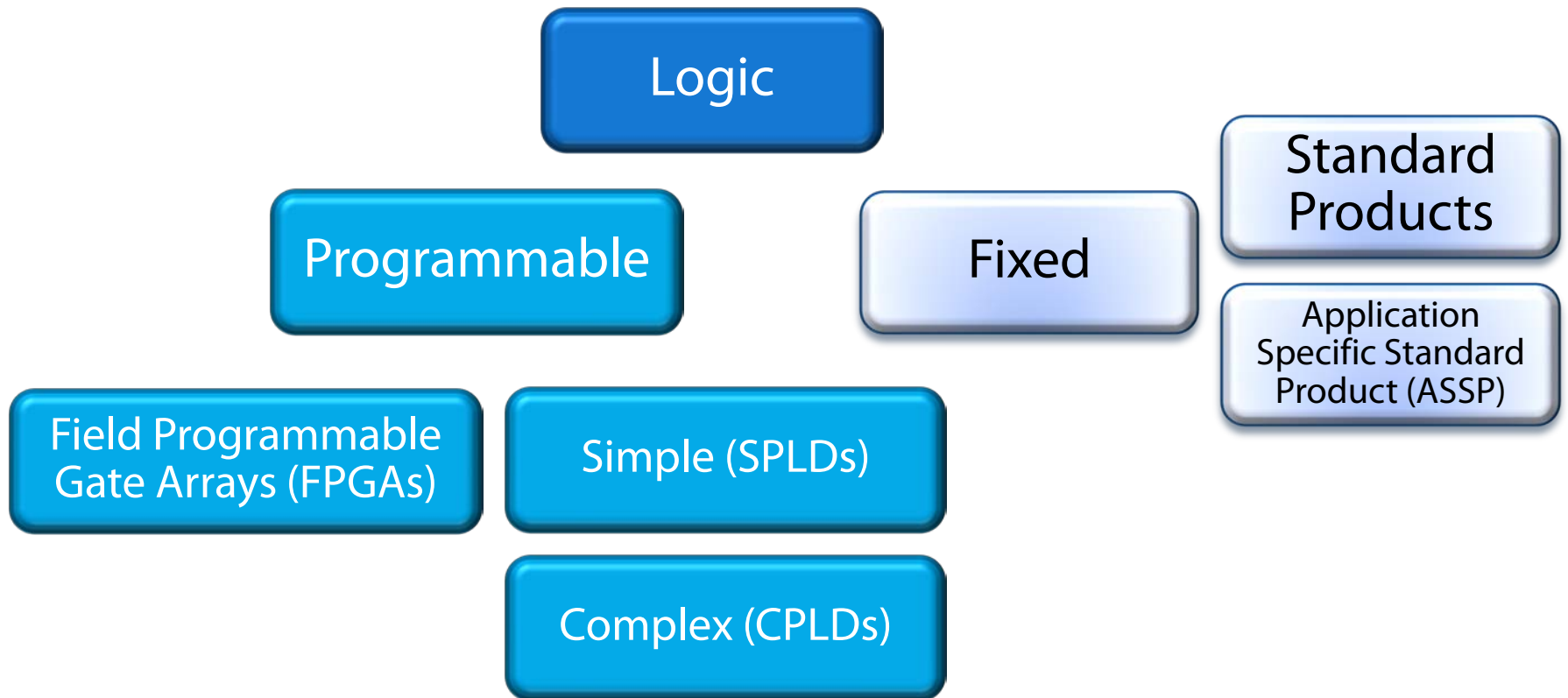
- **Fixed functionality**

- How to you make a change?

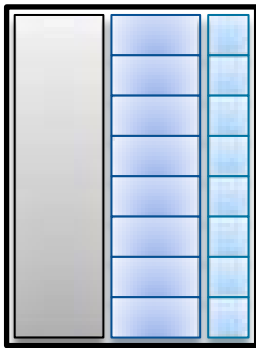
Standard Products



Logic Products



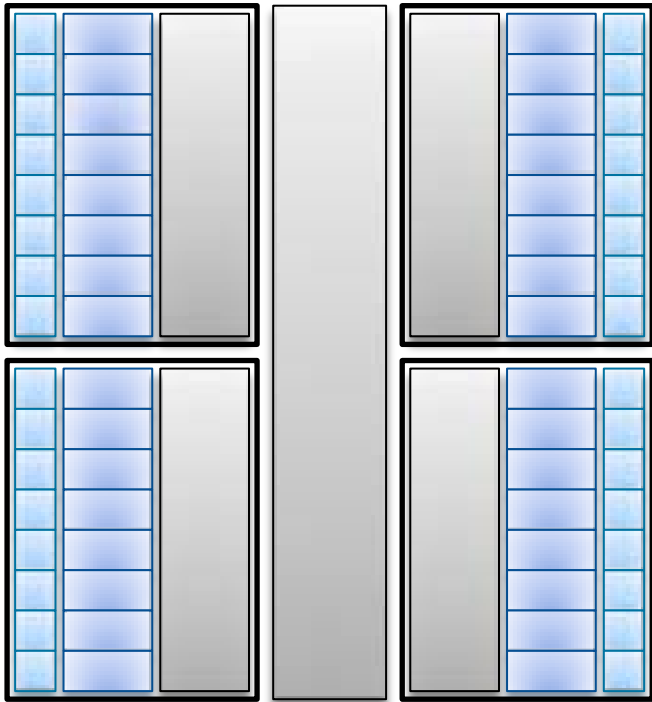
Simple PLD



PAL
GAL
PLD
PLA

- **Mostly small-density parts**
- **Small number of logic blocks**
 - Sum-of-product architecture
- **Inputs/Outputs (I/Os) blocks**
- **Programmable interconnect allows the blocks to communicate**
- **Underlying “configuration” cells to define the operation**
 - Usually in-system programmable Flash

Complex PLD



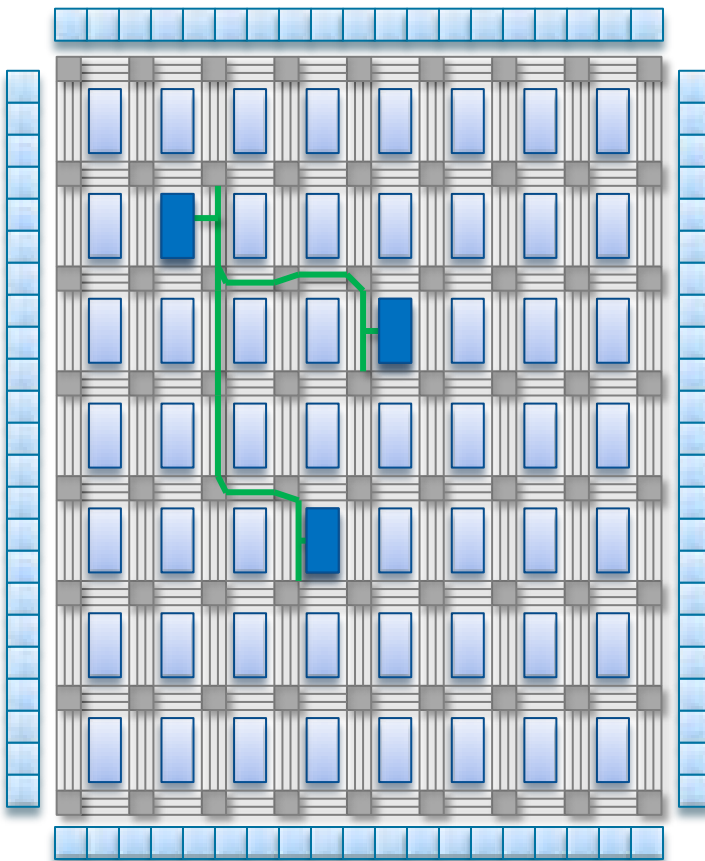
- Builds on simple PLD concept
- Multiple PLD blocks
- Secondary interconnect matrix allows communication between PLD blocks
- Underlying “configuration” cells to define the operation

What Does FPGA Mean?

- **Field-Programmable Gate Array**

- Field-programmable
 - Programmable in the “field”, without requiring a separate manufacturing facility
- Gate Array
 - The underlying architecture mimic “gate array” style architecture

Basic FPGA Architecture



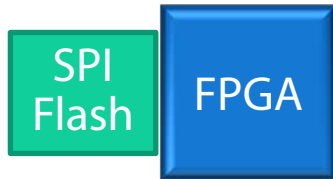
- **Ring of Inputs/Outputs (I/Os) blocks**
- **An array of Logic Blocks**
- **Programmable interconnect that allows a block to communicate to one or more other blocks**
- **Underlying “configuration” cells to define the operation**



FPGA Configuration Methods



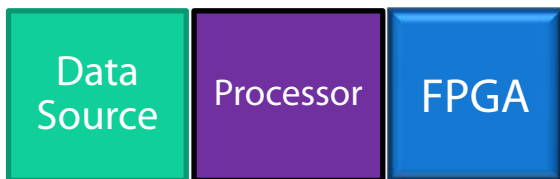
From internal Flash, anti-fuse, or NVCM memory



Self-loading, like a processor, from an external serial Flash



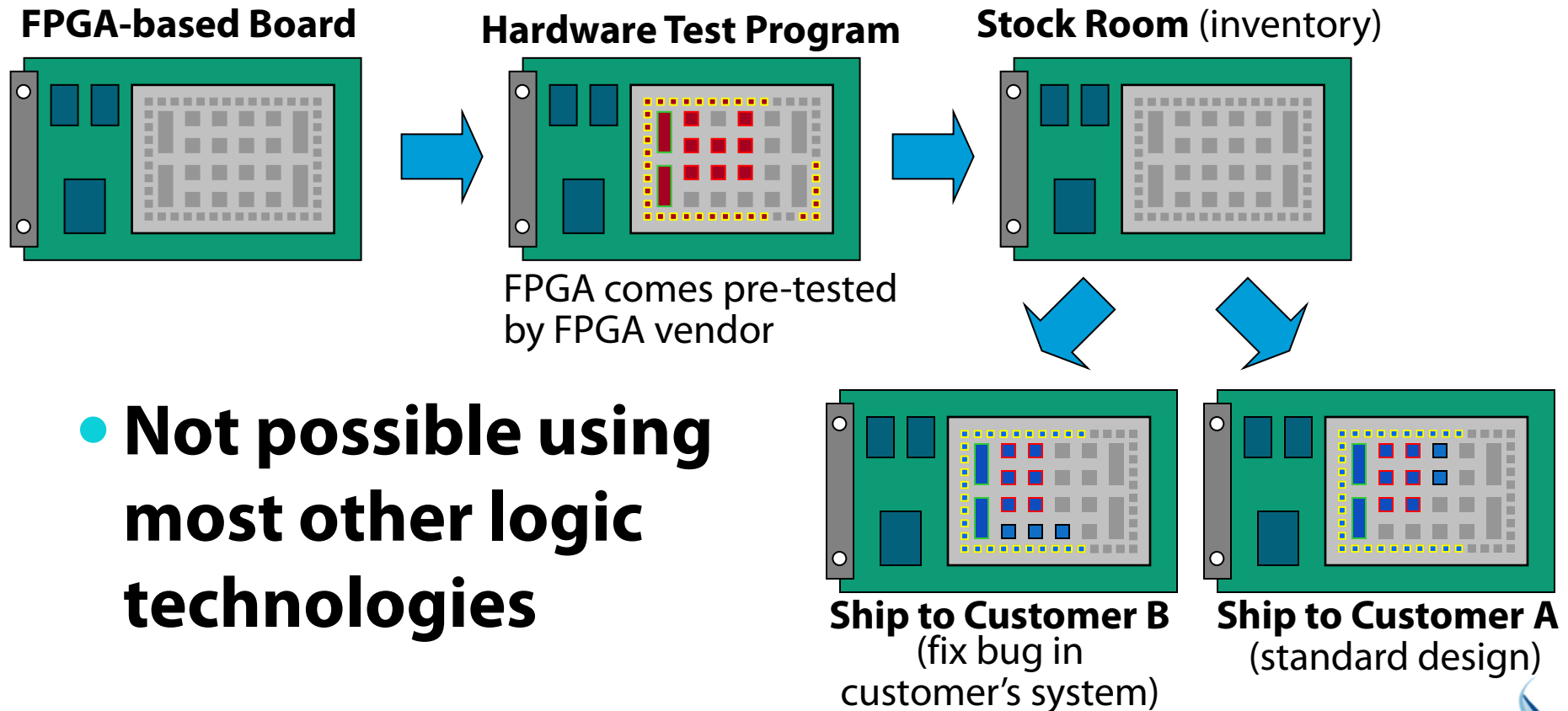
Self-loading, like a processor, from an external parallel NOR Flash



Downloaded from a data source by a processor, much like a processor peripheral. The data width can be x1, x8, or sometimes wider. The memory source can be Flash, hard disk, a network connection, etc.

Easiest system upgrades

Exploiting Programmability

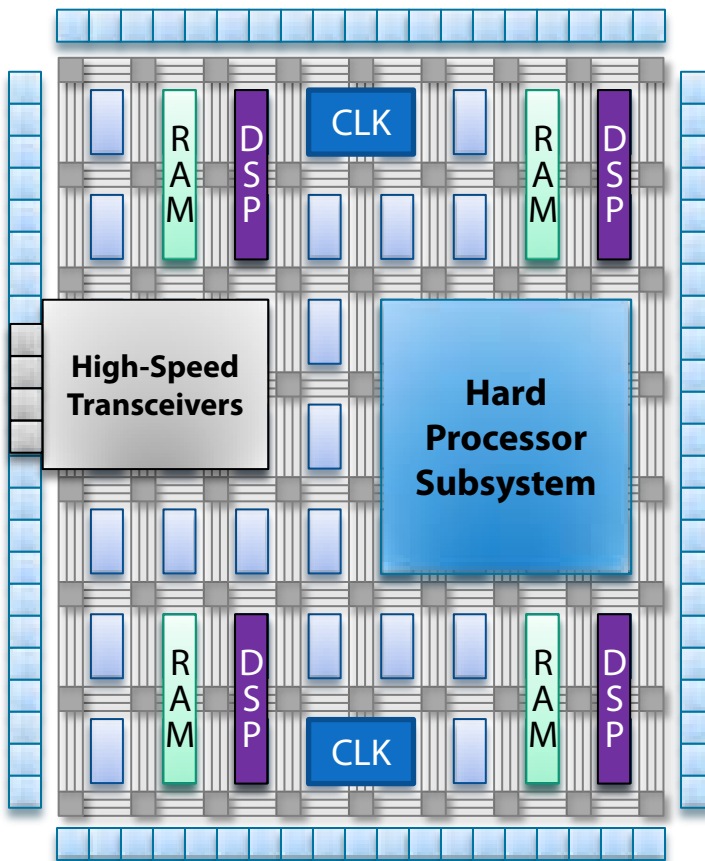


- **Not possible using most other logic technologies**

Bitstream Design Security

- **PROBLEM:** Unscrupulous competitor can sometimes directly and exactly copy your FPGA design
 - It's extremely difficult to reverse-engineer an FPGA bitstream
- **SOLUTIONS:**
 - Bitstream encryption (available on some devices)
 - Bitstream authentication

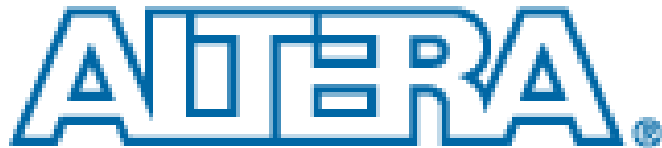
Advanced FPGA Architecture



- **Clock and Phase-Locked Loops**
- **On-Chip RAM memory blocks**
- **Multiplier or Digital Signal Processing (DSP) Blocks**
- **High-speed transceivers**
- **Dedicated Processors**

FPGA Manufacturers

The Big Players



Smaller Suppliers



Up-and-comers (growing from a niche)



Clash of the Titans

	Altera	Xilinx
High-End Family	Stratix	Virtex
Mid-Range Family	Arria	Kintex
Low-Cost Family (CIGARs)	Cyclone	Artix, Spartan
High-Speed Transceiver Family	Arria Family 'GS', 'GX', 'GT' Families	'T' Devices
CPLD	MAX	CoolRunner-II
ARM Cortex-A9 Family	SoC FPGA	Zynq-7000
Soft Processor Family	Nios II	MicroBlaze
In-System Debugging Tool	SignalTap	ChipScope Pro

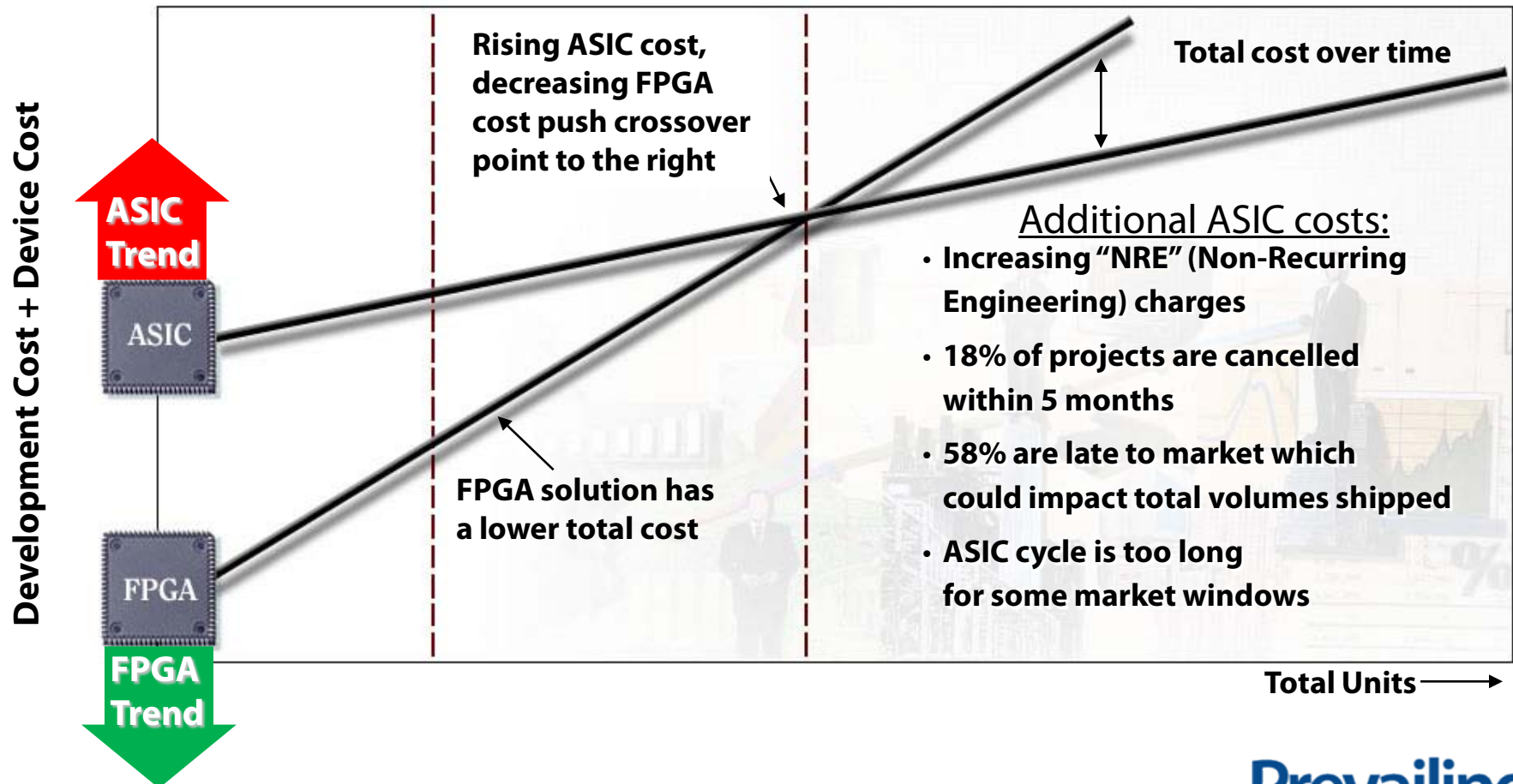
Programmable Logic Buzzwords

- **FPGA:** Field-Programmable Gate Array
- **PLD:** Programmable Logic Device
- **SPLD:** Simple Programmable Logic Device
- **CPLD:** Complex Programmable Logic Device
- **EPLD:** Erasable Programmable Logic Device
- **PAL:** Programmable Array Logic
- **PLA:** Programmable Logic Array
- **GAL:** Generic Array Logic
- **FPLA:** Field Programmable Logic Array

ASIC or FPGA?

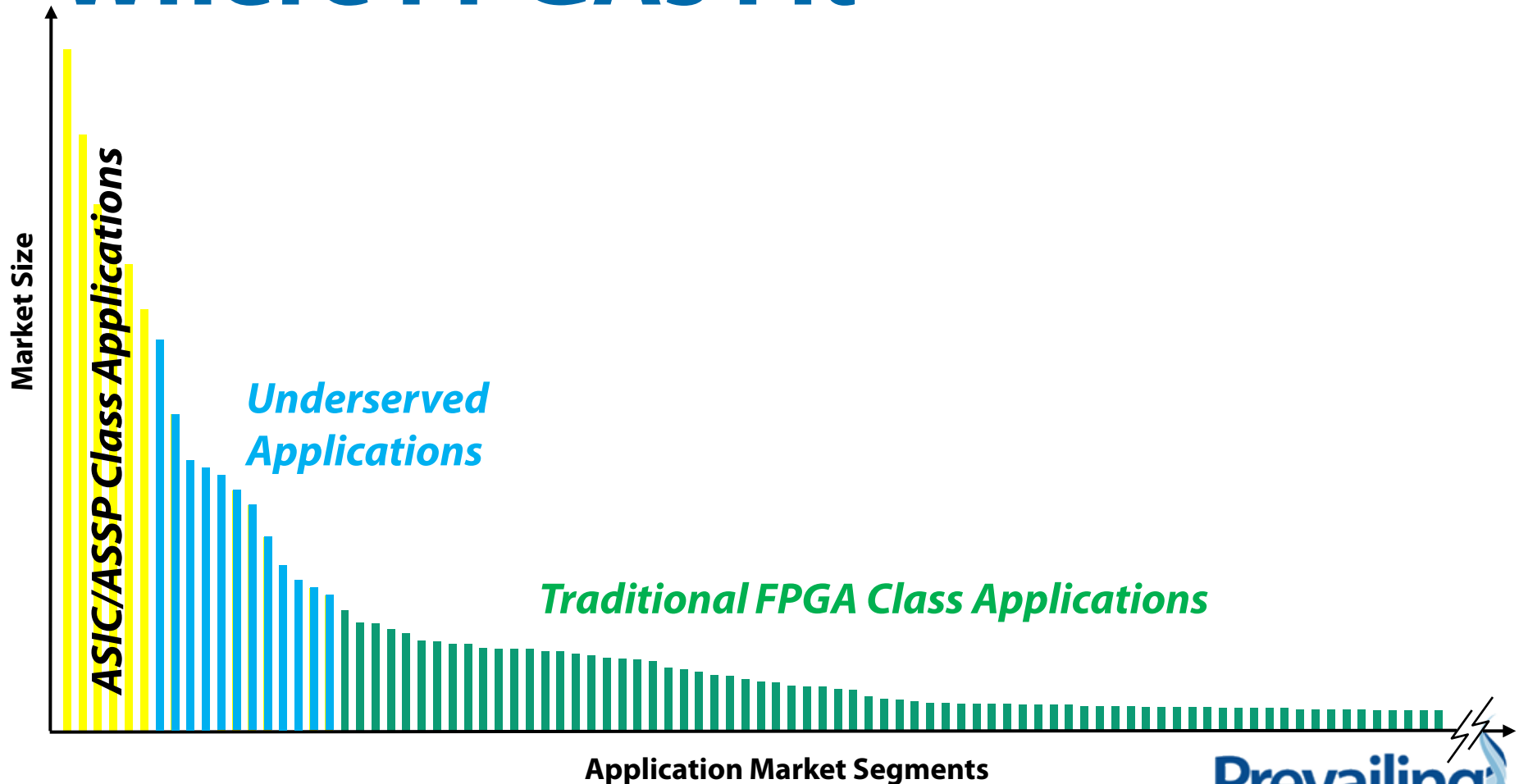
- **ASIC cost: \$100,000 charge plus \$3 per chip**
- **FPGA cost: \$5 per chip**
- **Which is more cost-effective?**
- **When is it more cost-effective to buy at 7-Eleven than at Costco store?**

FPGA/ASIC Crossover Costs

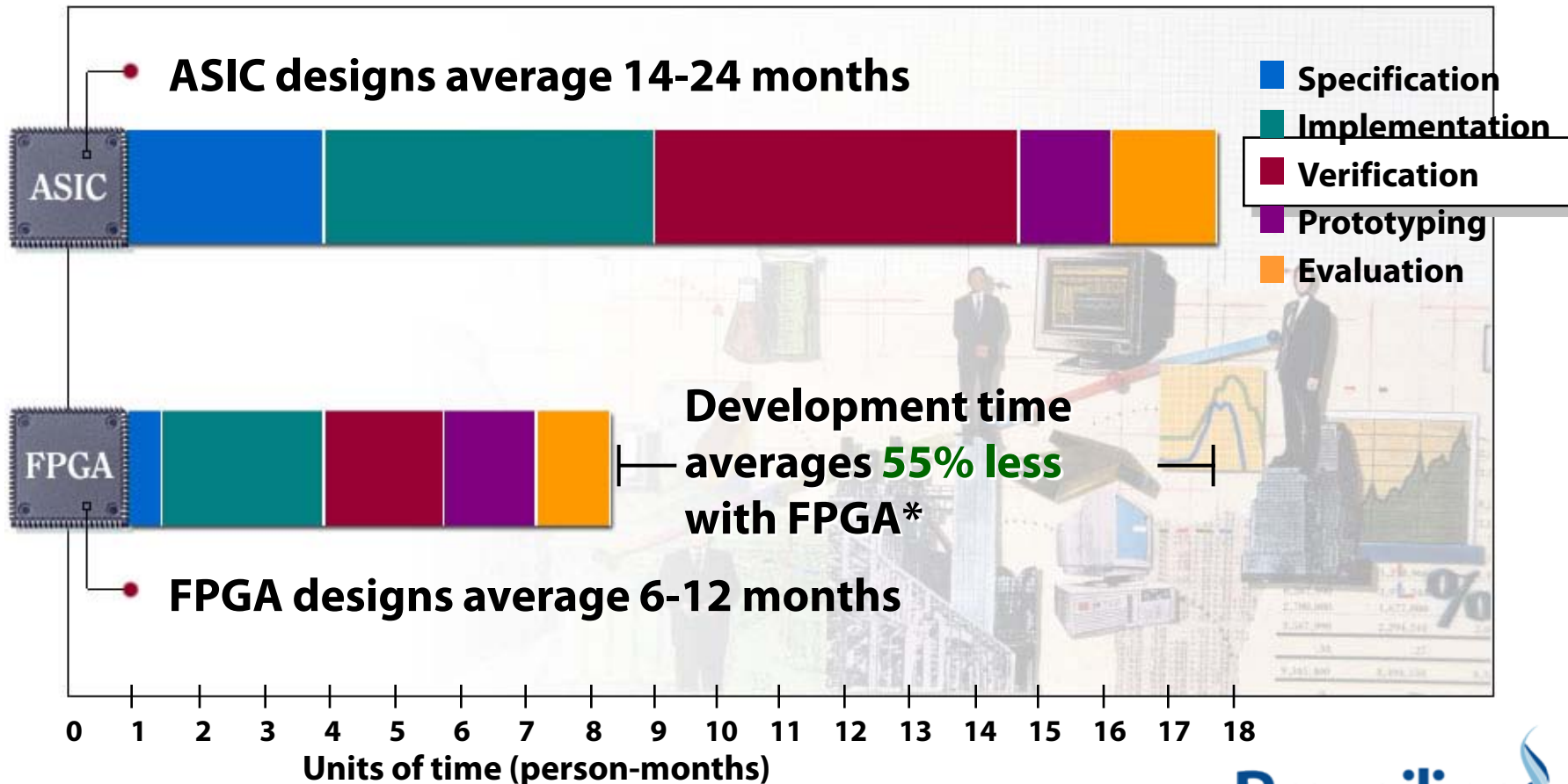


Source: Current and Emerging Embedded Markets and Opportunities – ElectronicMarket Forecasters

Where FPGAs Fit



Shorter Development Cycles Increased Revenue Potential



Source: Harvard Study
* Based on an average of 391 different sized designs

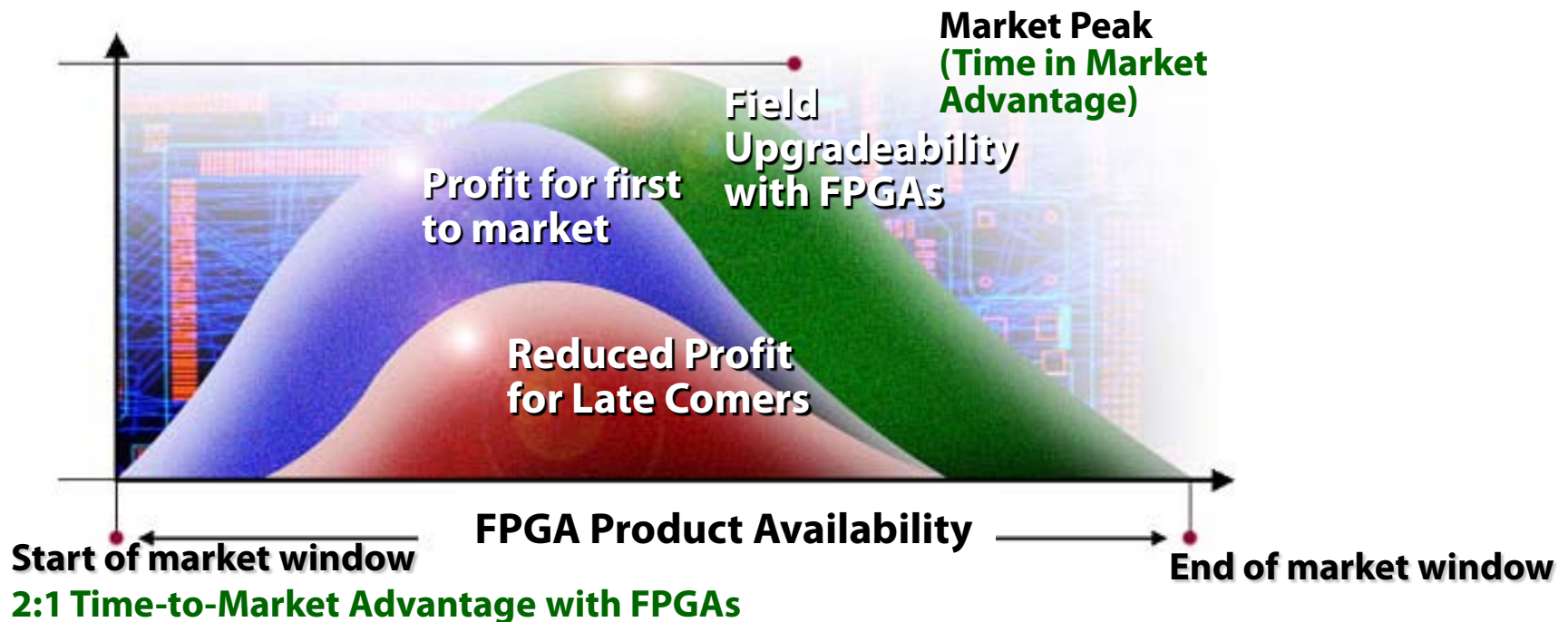
FPGA Maximize Profitability

- **Products that are 6 months late but on budget earn 33% less profit over 5 years***
 - Every 4 week delay equals 14% loss in market share †
- **Upgradeability extends product lifetime**

* SOURCE: CURRENT AND EMERGING EMBEDDED MARKETS AND OPPORTUNITIES – ELECTRONICMARKETFORECASTERS

† SOURCE: MCKINSEY & CO. , # SOURCE: JOHN CHAMBERS WINDRIVER SYSTEMS, INC.t

FPGA Maximize Profitability



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† SOURCE: MCKINSEY & CO. , # SOURCE: JOHN CHAMBERS WINDRIVER SYSTEMS, INC.†

Where FPGAs Live

Communications

- Infrastructure
- Wireless



Automotive

- Infotainment
- Instrumentation



Aerospace and Defense

- Avionics
- Space



Consumer

- Displays
- Handhelds



Industrial Scientific and Medical

- Video Imaging
- Test and Measurement



Why Programmable Logic?

- **Faster time-to-market**
- **Less risk if errors found**
 - Or design changes required
 - “Insurance policy” for design engineers!
- **Easy to do physical test instead of just software simulation**
- **Less risk if product needs to change**
- **Can have multiple versions of one product**
- **Upgrade in the field**
- **Re-program as needed in the application**

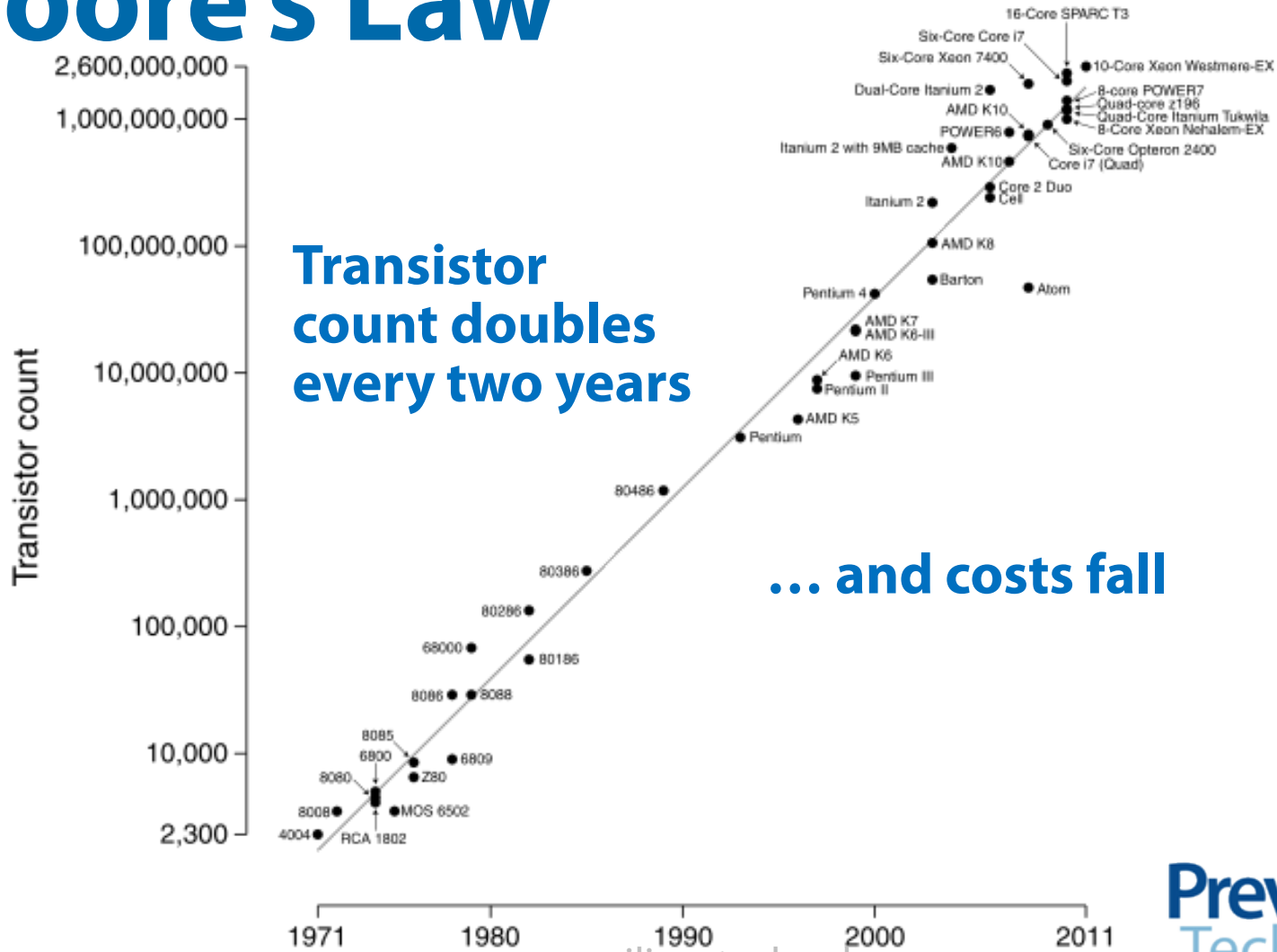
Prototyping

Production

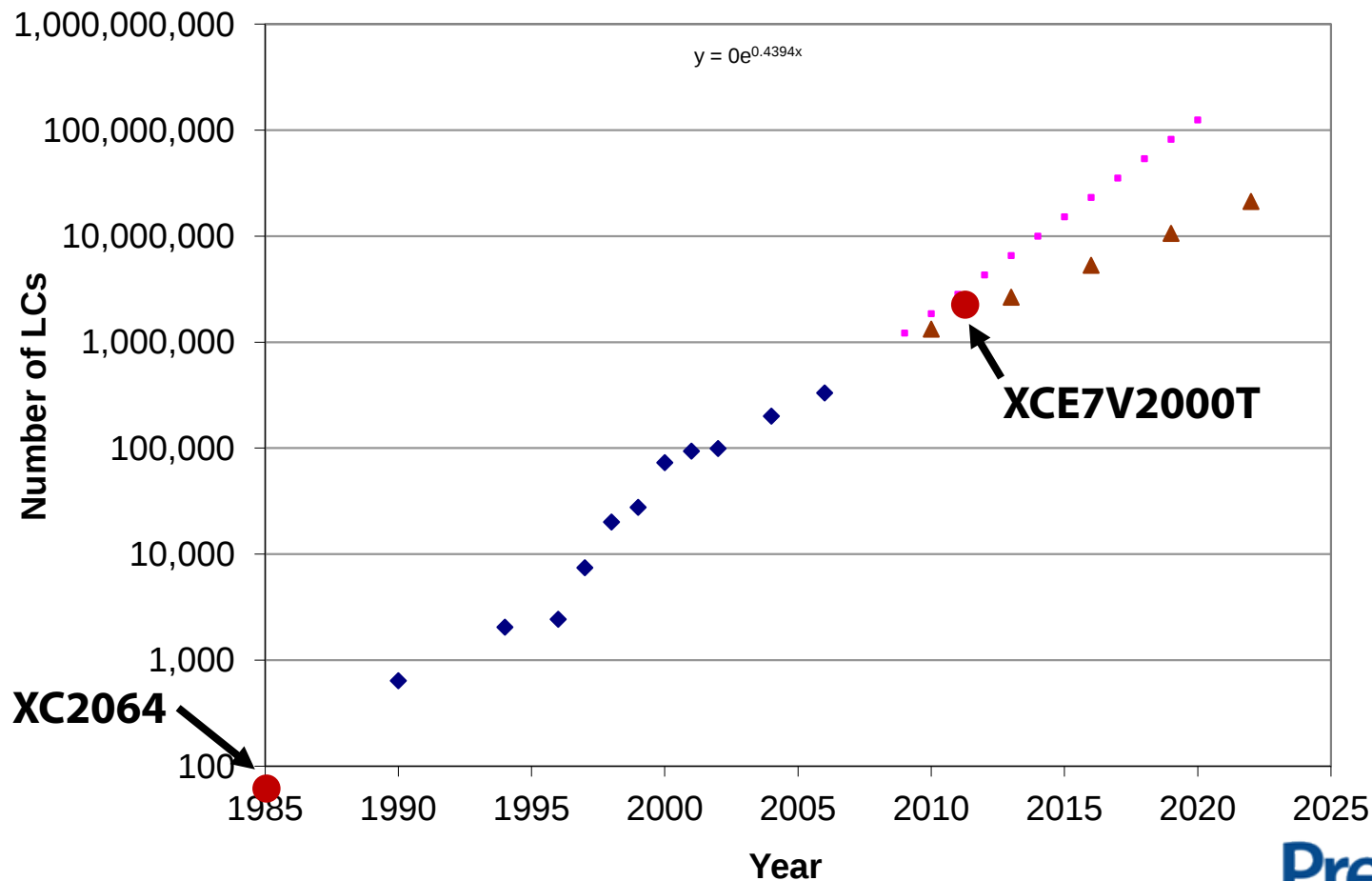
Moore's Law

Transistor count doubles every two years

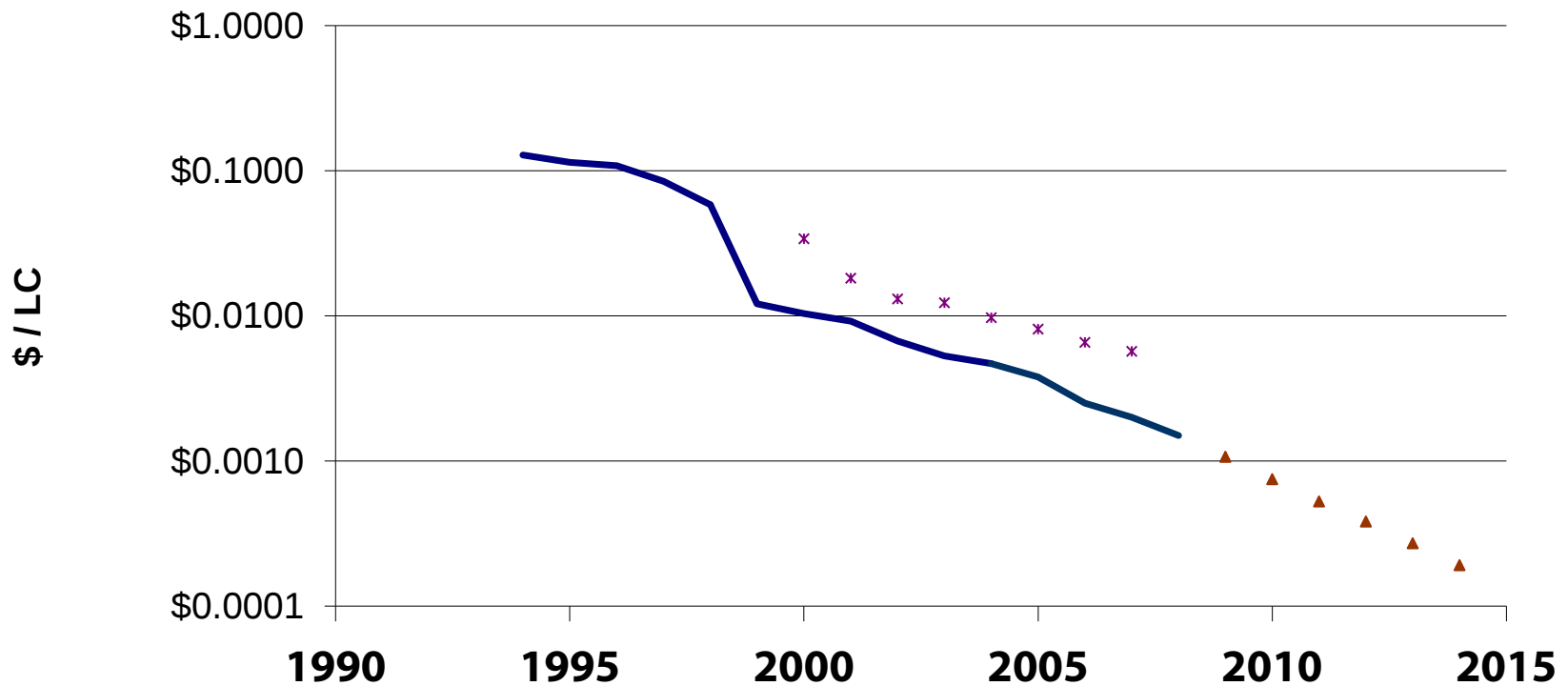
... and costs fall



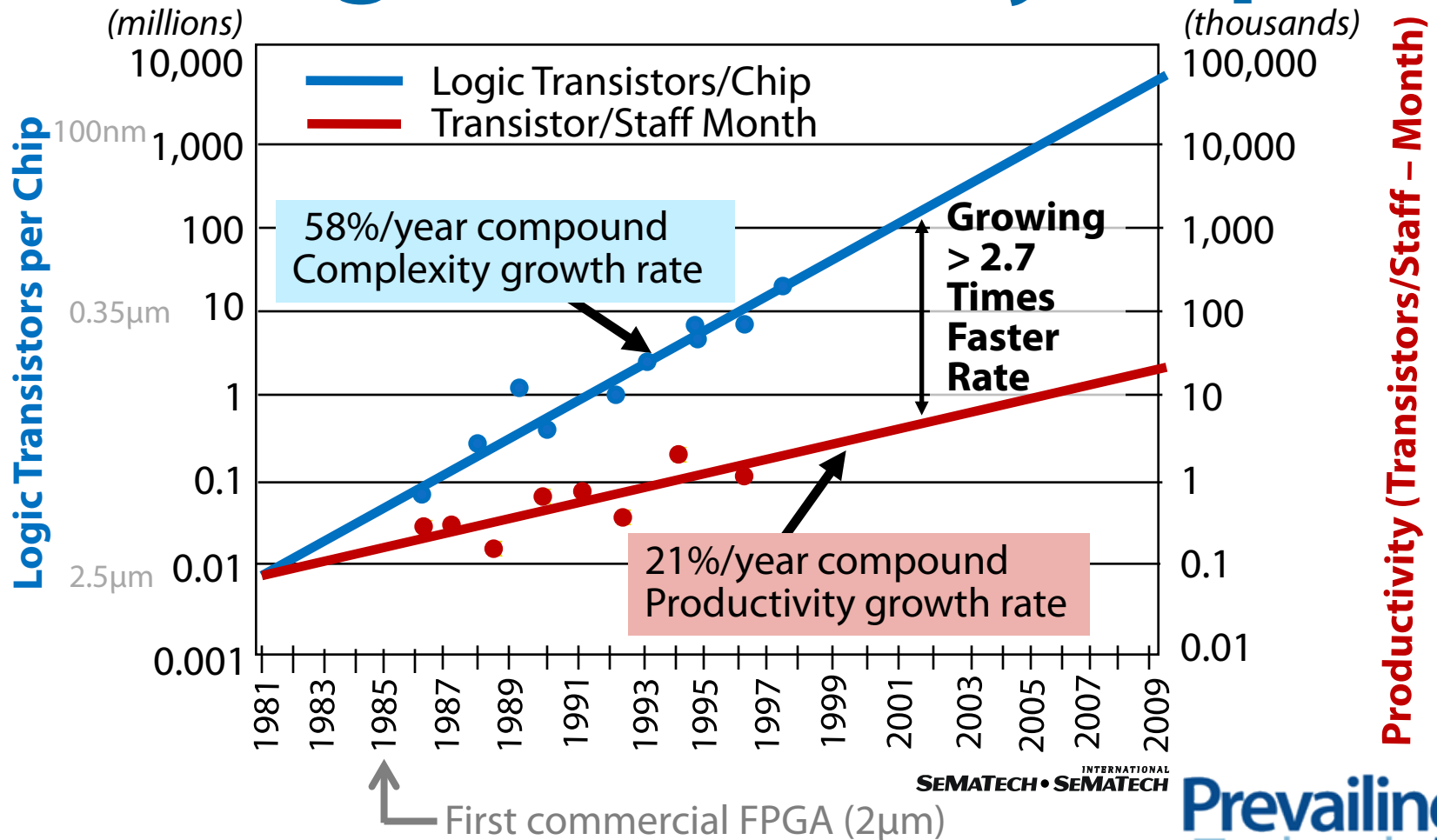
Number of Logic Cells



FPGAs Drop in Price



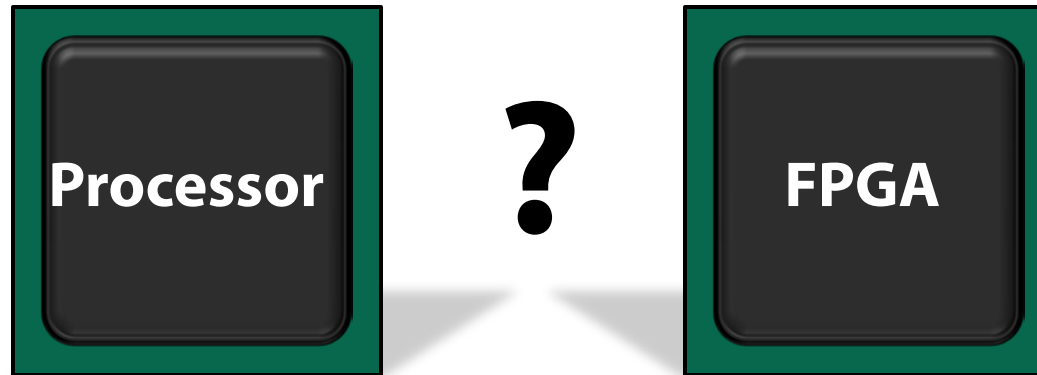
Growing Productivity Gap



Cost Trends Benefiting PLDs

- **Production costs increasing for newest technology: fab costs billions and mask costs millions**
- **Transistor costs decrease for newest technology**
 - Moore's Law: transistor density doubles every 2 years
 - Favors moving quickly to latest generation
 - Seen in consumer electronics
- **Best chips are those built in highest volumes**
 - Amortize production costs over many chips
- **PLDs are low cost because thousands of other people are also buying the same chip, but for their own custom functions!**

Which “Desktop Logic” is Best?



- **An FPGA can perform any digital function that a processor can—and *vice versa***
 - FPGA designs simulated on a processor
 - Processors prototyped with FPGAs
 - Processors built within FPGAs

Shand's Law

“If an application can be done in a processor, it will be done in a processor.”

- **Processors are easier to program and to use**
 - May not be fast enough for the application
 - May not have enough inputs and outputs

Processor Architecture



Memory



**Processing
Unit**



Clock



Instructions

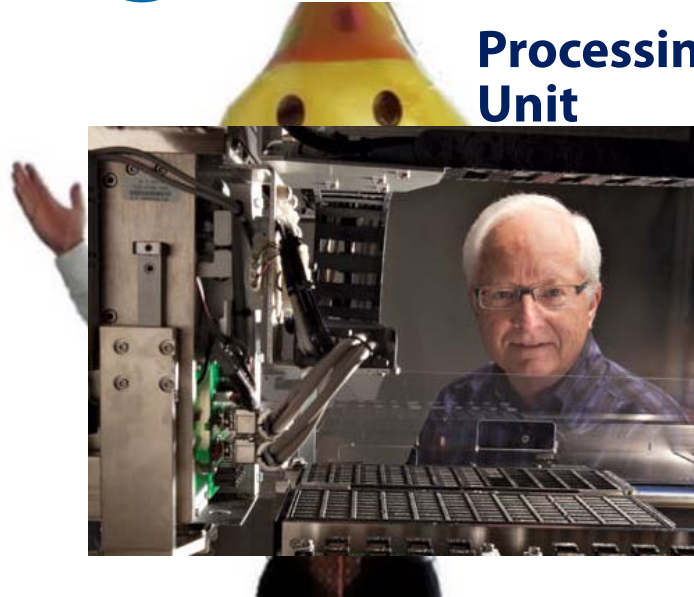


**Input/
Output**

Upgrading the Processor



Memory



**Processing
Unit**



Clock



Instructions

Interrupts

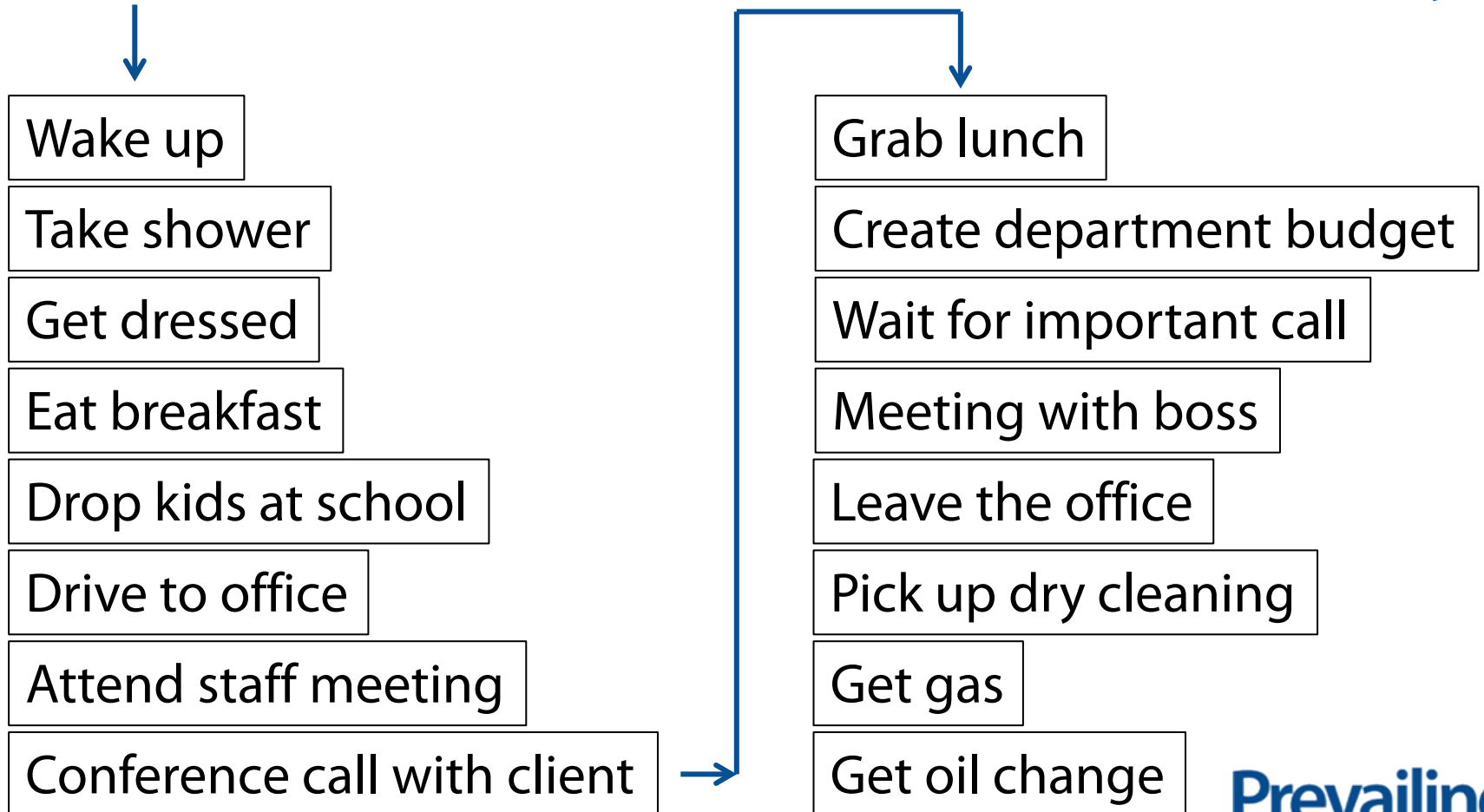


**Input/
Output**

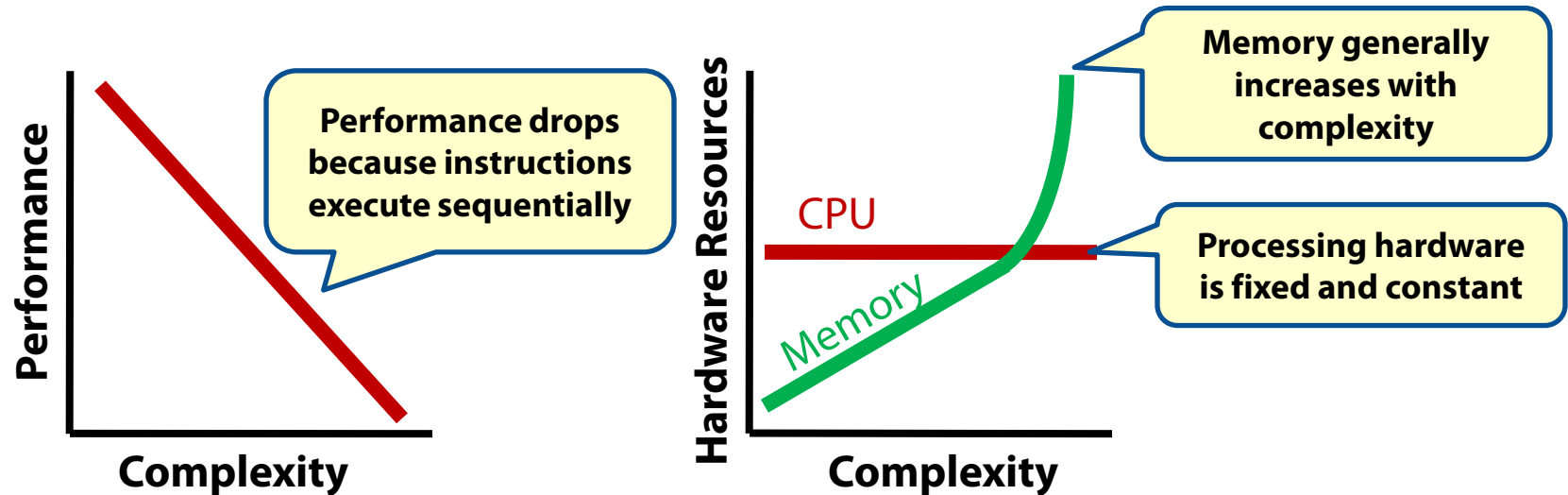


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Processors Process Sequentially



Traditional Processors



- **Complexity issues**

- Subtasks may interfere with one another
- Indeterminate response times

The FPGA Approach

Processing
Unit



Clock



**Do this one
thing!**

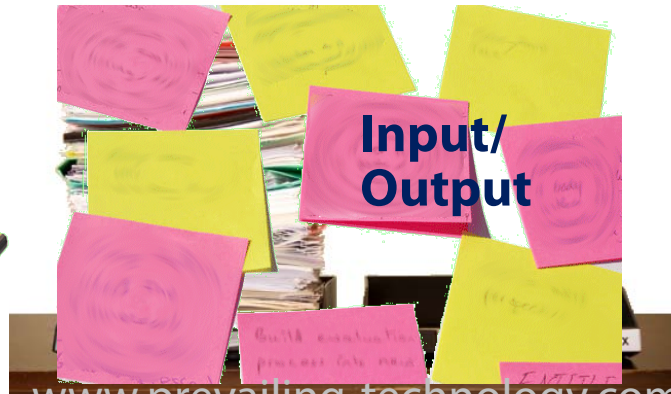
Instructions



Memory



Input/
Output



Interrupts

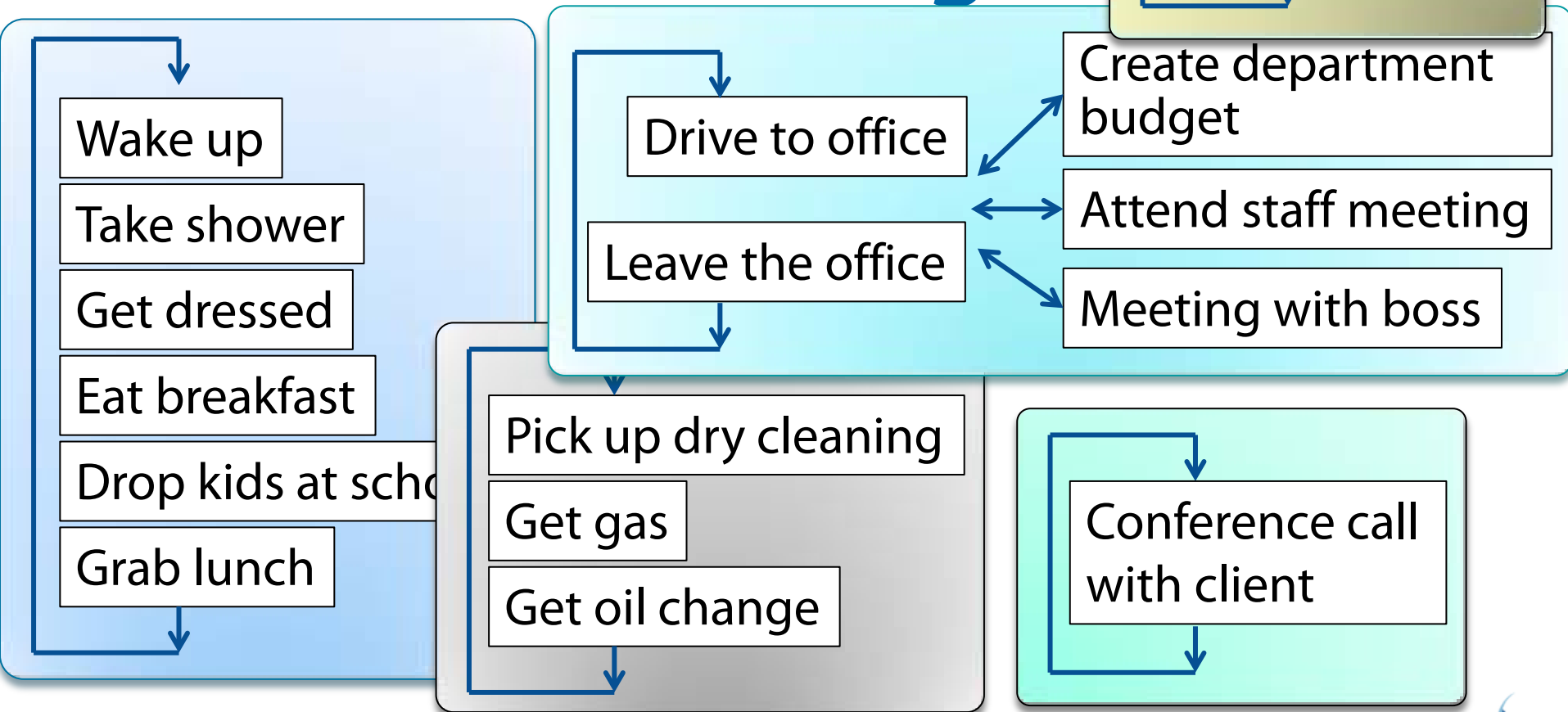


The FPGA Approach

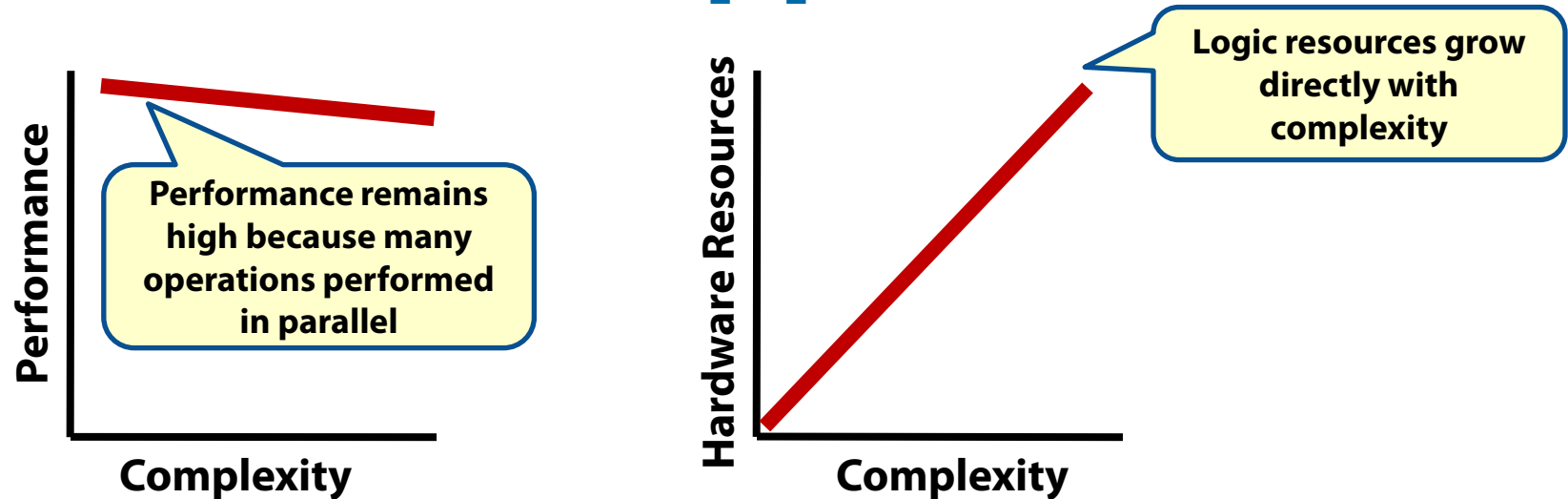
Logic Element



Parallel Processing



FPGA-based Applications



- **Complexity issues**

- FPGA size and cost generally increase with increasing application complexity

FPGA-based Processors

- **Building the processor on an FPGA provides more flexibility, higher performance, smaller (and sometimes cheaper) system**
- **Requires extensive software support**
- **“Soft” processors**
 - Xilinx MicroBlaze, Altera Nios, Lattice Mico32
 - Pre-defined using general FPGA gates
- **“Hard” processors**
 - ARM Cortex-A9 dual-core CPU
 - Xilinx Zynq-7000
 - Altera SoC FPGAs
 - PowerPC in some Xilinx Virtex FPGA families
 - Operates independent of programmable FPGA logic

Designing Programmable Chips

Specify the
Application

Compile the
Application

Download or
Program the
Device

Processor

C, C++, Java

Compiler,
Assembler

PLD/FPGA

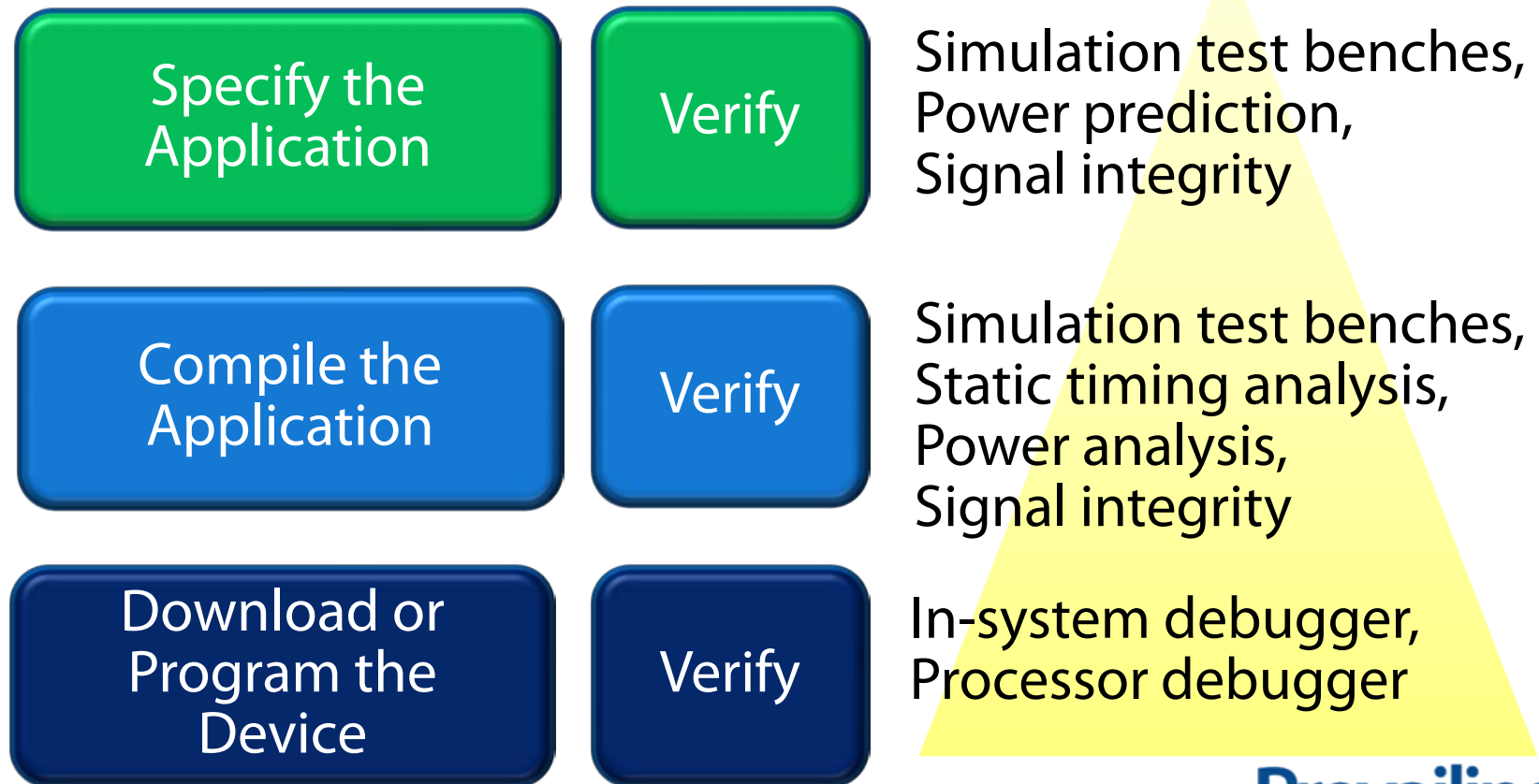
VHDL, Verilog,
(Azido, Matlab, Labview)
(C, C++, Java)

Constraints

Logic Synthesis,
Partition, Place,
Route

Trust but Verify, Verify, Verify

Cost of finding bug



FPGA Development Advantages

- **Most FPGAs are reprogrammable**
- **Supports iterative design**
 - Bring up portions of the design independently
- **Perform integration testing in the real system, with real components and software**
- **If system includes upgrade ability, the FPGA design can be upgraded in the field**

Build or Buy Design?

- **Most applications require some amount of custom design**
- **Major building blocks may use Intellectual Property (IP) blocks**
 - From the FPGA vendor (free or \$\$\$)
 - From an IP vendor (almost never free)
- **If done correctly, can greatly speed development and lower costs**

FPGAs in a Nutshell

- **FPGAs bring “desktop publishing” benefits to system design**
 - Fast time to market
 - Easy customization
 - Low risk
 - Affordable for low to all but the highest production volumes

Questions?





Thank You!

Prevailing Technology

- **Define:** critical features, target users and markets, user case scenarios, competitive comparisons and benchmarking
- **Design:** digital electronic systems, FPGA, embedded systems, intellectual property (IP) cores, VHDL, Verilog, C
- **Develop:** software prototypes, prototype easy-to-use user interfaces, software alpha and beta user testing, evaluation boards and systems, technical marketing plans, design libraries, software libraries, intellectual property (IP) cores, reference designs, application design examples
- **Document:** data sheets, reference manuals, design handbooks, application notes, user guides, white papers, trade publication articles, conference papers
- **Deploy:** Field training, customer training, self-support web sites, customer affinity web sites, user group meetings, technical seminars