SiliconBlue™

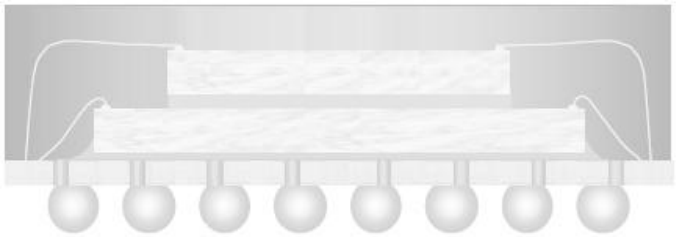
SiliconBlue Technologies
iCE65 Architecture

Programmable Solutions for Consumer Handheld

7-MAY-2008 (v1.1)

Agenda

- iCE65 Architecture
  - Overview
  - Programmable Logic Blocks (PLBs)
  - Programmable Input/Output Blocks (PIOs)
  - RAM4K Blocks
  - Interconnect
  - Powering iCE65 Devices
- iCE65 Configuration
  - Modes and Methods
  - SPI Serial Flash
  - NVCM



iCE Architecture

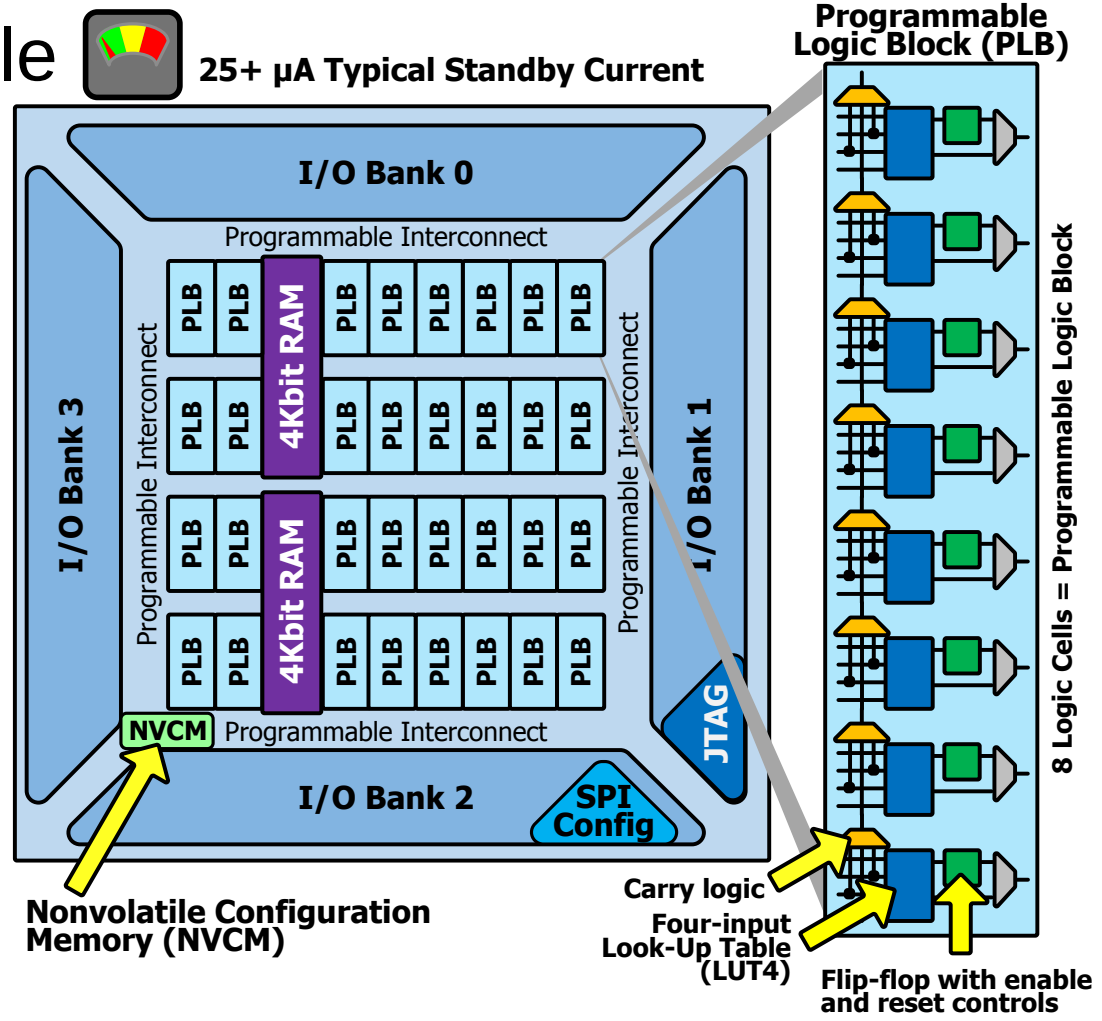
iCE65 Low Power NV FPGAs

	iCE65L02	iCE65L04	iCE65L08	iCE65L16
Logic Cells (LUT4 + FF)	1,792	3,520	7,680	16,896
Programmable I/O (max.)	128	176	222	384
Differential I/O Pairs (max)	16	20	25	54
RAM4K blocks	16	20	32	96
RAM4K bits	64K	80K	128K	384K
Core voltage options	1.2V, 1.0V			
Static current (typical, 1.2V)	25 µA	50 µA	100 µA	250 µA
I/O Banks	4 + SPI mini bank			
Global Buffers	8			
iCEGATE input disables	4			

*2010 Volume Quantities

iCE65 FPGA Architecture

- Ultra-low power
- Array of Programmable Logic Blocks (PLB)
- Surrounded by four I/O Banks
- 4Kbit RAM Blocks
- Programmable interconnect
- Non-Volatile Configuration Memory (NVCM)
- SPI interface

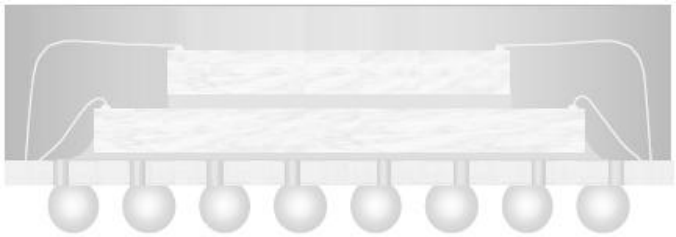


Power Consumption

- Total Power = Static + Dynamic
- Static power is almost entirely controlled by IC design
  - Dominated by leakage current
  - Controlled by IC design techniques, transistor choices, device-level architecture
    - Choose the right device: SiliconBlue iCE65 FPGAs!
  - Only User controls are voltage and temperature
    - Lower core voltage helps
- User has many levers to control dynamic power

Dynamic Power

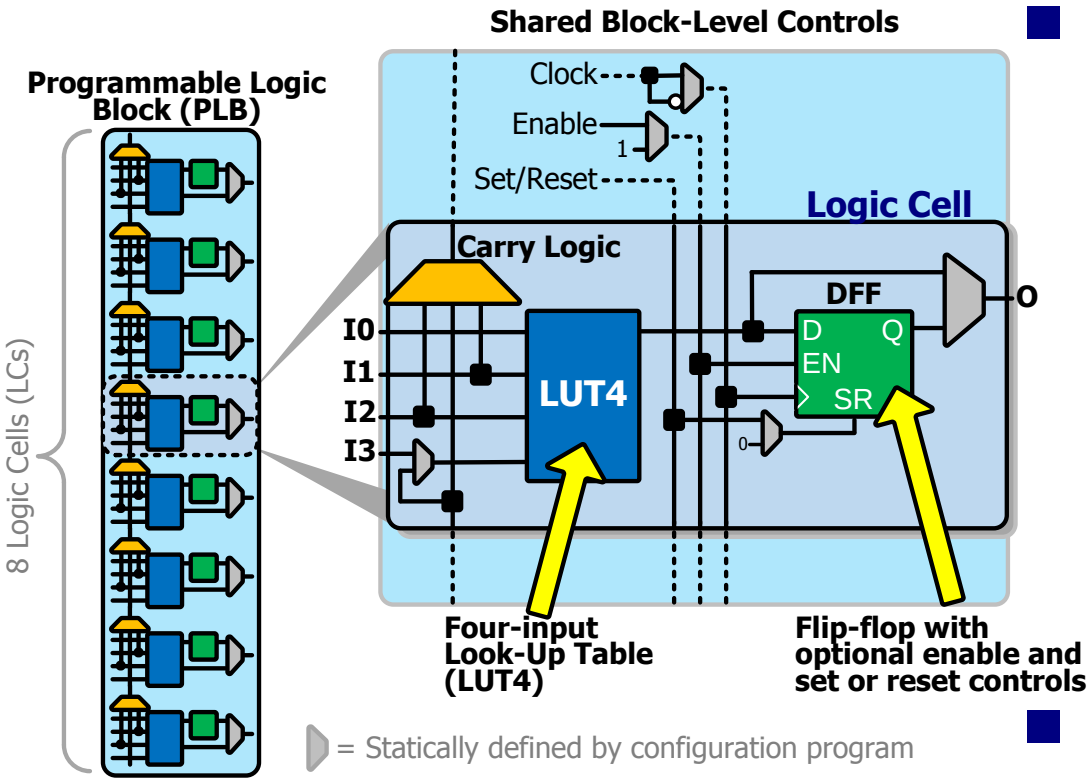
- Dynamic Power = **$AfCV^2$**
- **A** = **Activity:** If it moves, it burns dynamic power. Corollary: If it moves, kill it.
- **f** = **Frequency:** The slower it moves, the less power it uses.
- **C** = **Capacitance:** High fanout routes have more capacitance.
- **V^2** = **Voltage:** Power scales with the square of the voltage. Operate at lowest possible voltage.



Programmable Logic Block

PLB

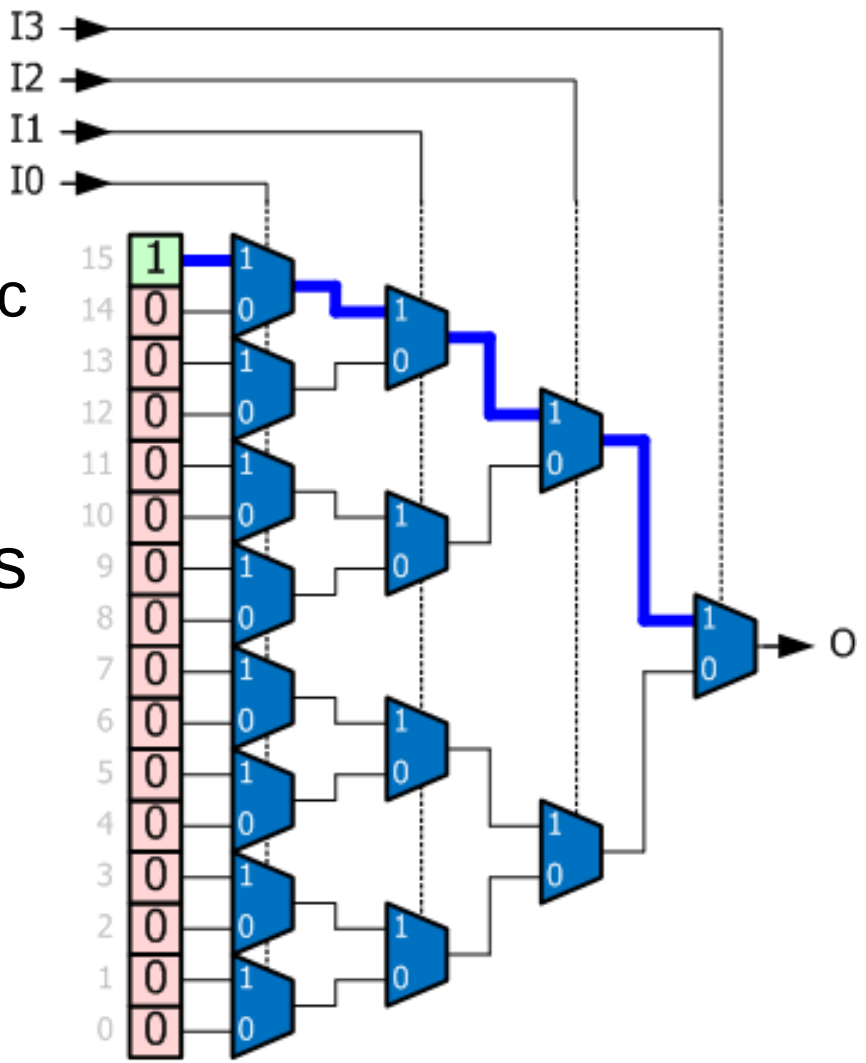
Programmable Logic Block



- Programmable Logic Block (PLB)
  - Eight 4-input Look-up Tables (LUT4)
  - Eight ‘D’ flip-flops with shared clock, clock enable, set/reset control
  - Fast carry logic
- Familiar, well supported by logic synthesis tools

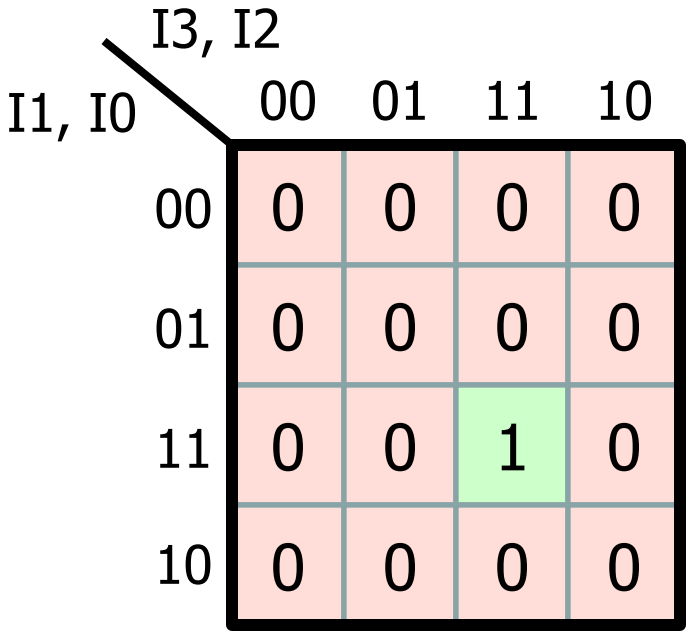
What is a LUT4?

- 4-input Look-Up Table
  - A 16x1 PROM
  - Locations loaded during configuration with desired logic value
- Popular method to create logic in SRAM-based FPGAs
  - Altera, Lattice, Xilinx
  - Widely supported
- Four inputs select 1 of 16 memory locations
  - Any possible function of between 0 to 4 inputs



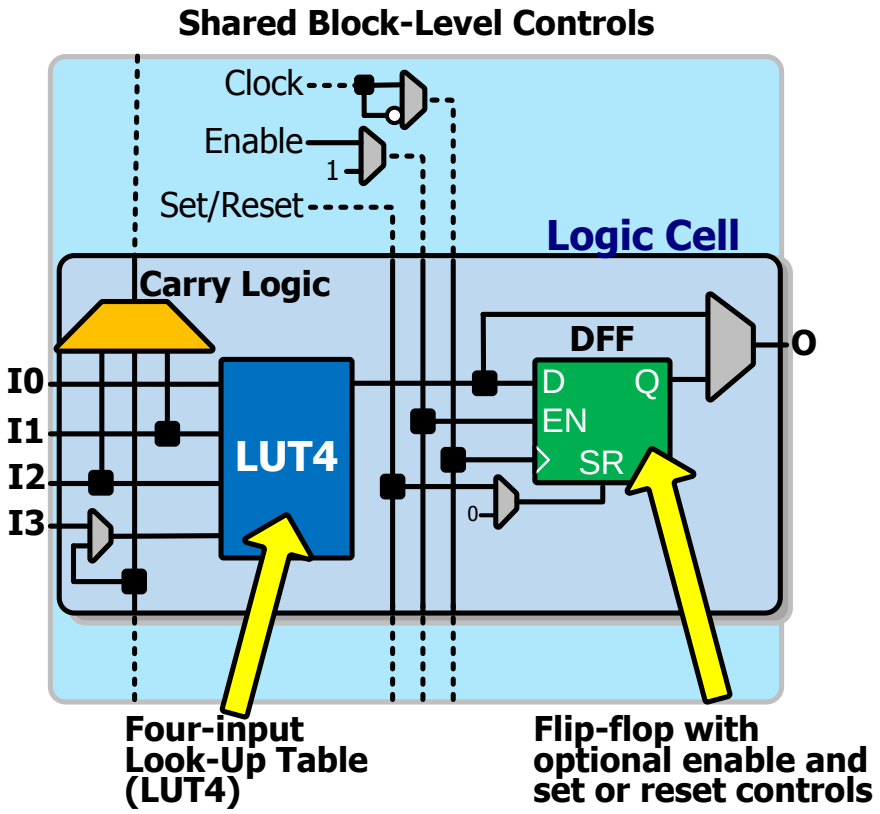
Alternate View: Karnaugh Map

- Karnaugh maps commonly taught in digital design courses
- LUT4 is essentially a four-input Karnaugh map
  - Programmed by configuration bitstream
  - Any possible function of between 0 to 4 inputs



$$O = I3 \bullet I2 \bullet I1 \bullet I0$$

Flip-flop Options



- Select LUT4 or flip-flop as Logic Cell output
- Clock is shared
  - Rising-edge triggered, or
  - Falling-edge triggered
- Enable is shared
  - Always enabled, or
  - Selectively enabled
- Set/Reset is shared
  - None
  - Set or Reset (per Logic Cell)
  - Synchronous or Asynchronous (per Logic Cell)
- Flip-flops reset to '0' after power-on, CRESET_B

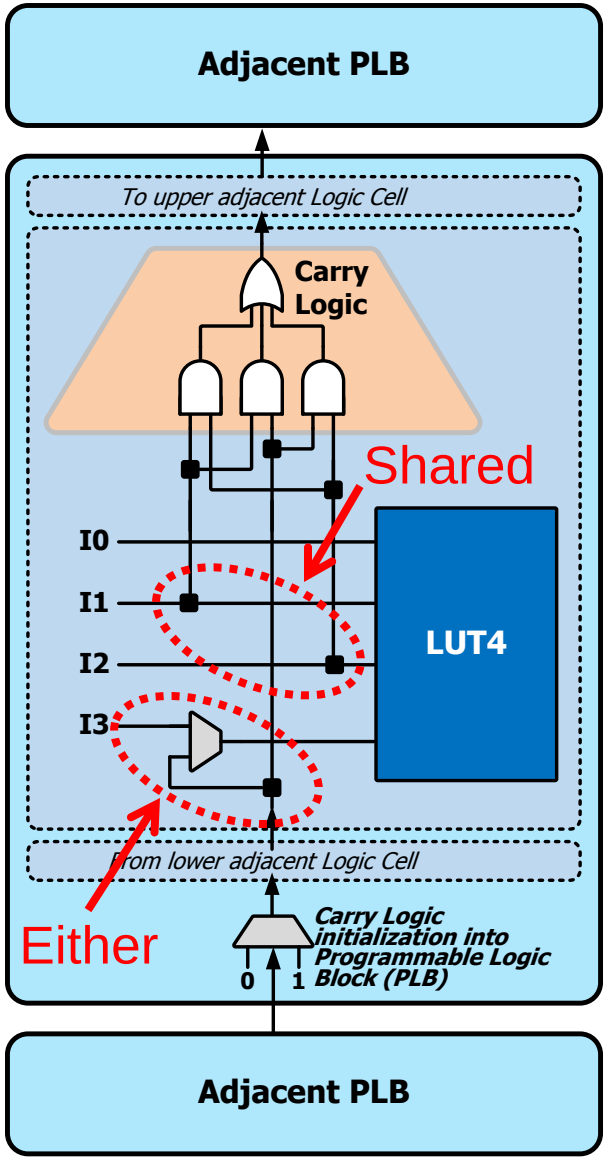
Flip-flop Packing in PLB

- Due to shared controls, only flip-flops sharing common controls pack into a single PLB
- Eight possible groupings

Group	Active Clock Edge	Clock Enable	Set or Reset (Sync. Or Async.)
1	↑	None (always enabled)	None
2	↓		
3	↑		✓
4	↓		
5	↑	Selective (controlled by enable input)	None
6	↓		
7	↑		✓
8	↓		

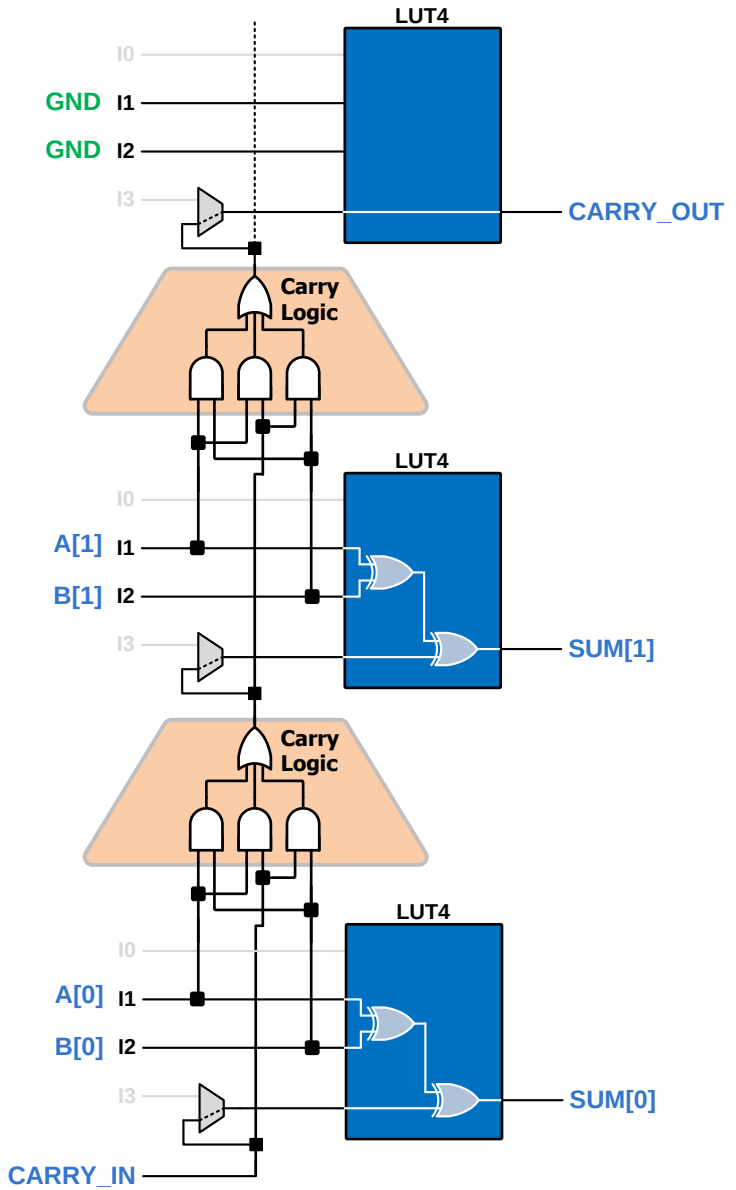
Carry Logic (Adder Ladder)

- Each Logic Cell includes special logic to build arithmetic functions
  - ~ 10X faster than LUT alone
- Carry logic + LUT required to build useful functions
- Carry in, initialization input to each PLB
  - May need a Logic Cell to initialize chain in some cases
  - May need a Logic Cell to exit the chain
- Carry logic cascade through the Logic Cells in a PLB, up a column
- Carry Logic driven High when not used (low power)
- I1, I2, I3 inputs shared/borrowed



Carry Logic Example

- Two-bit Adder with Carry In and Carry Out
  - Each logic cell produces a
    - 1-bit Sum using a LUT4
    - Carry using the Carry Logic
  - The carry propagates up the chain to the next bit
  - Final carry output tapped out of a LUT
- Carry In
  - Initialized within PLB, or
  - Created using a LUT4 to start



Other Arithmetic Functions

- Carry Logic (Adder Ladder) only generates carry for add operations
  - Adder
  - Accumulator
  - Incrementer
  - Binary Up Counter
- What about other functions?
  - Subtracter
  - Decrementer
  - Down Counter

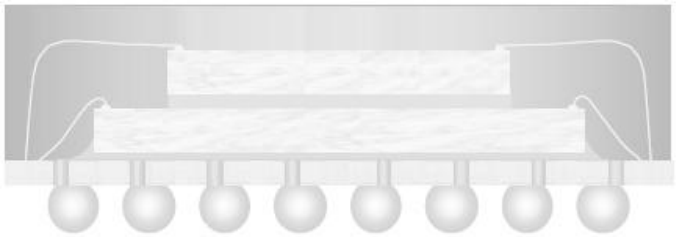
- Using 2s complement arithmetic, invert carry

$$A - B + 0 = A + \overline{B} + 1$$

$$B = 2 = 0010$$

$$A - 0010 + 0 = A + 1101 + 0001$$
$$= A + 1110$$

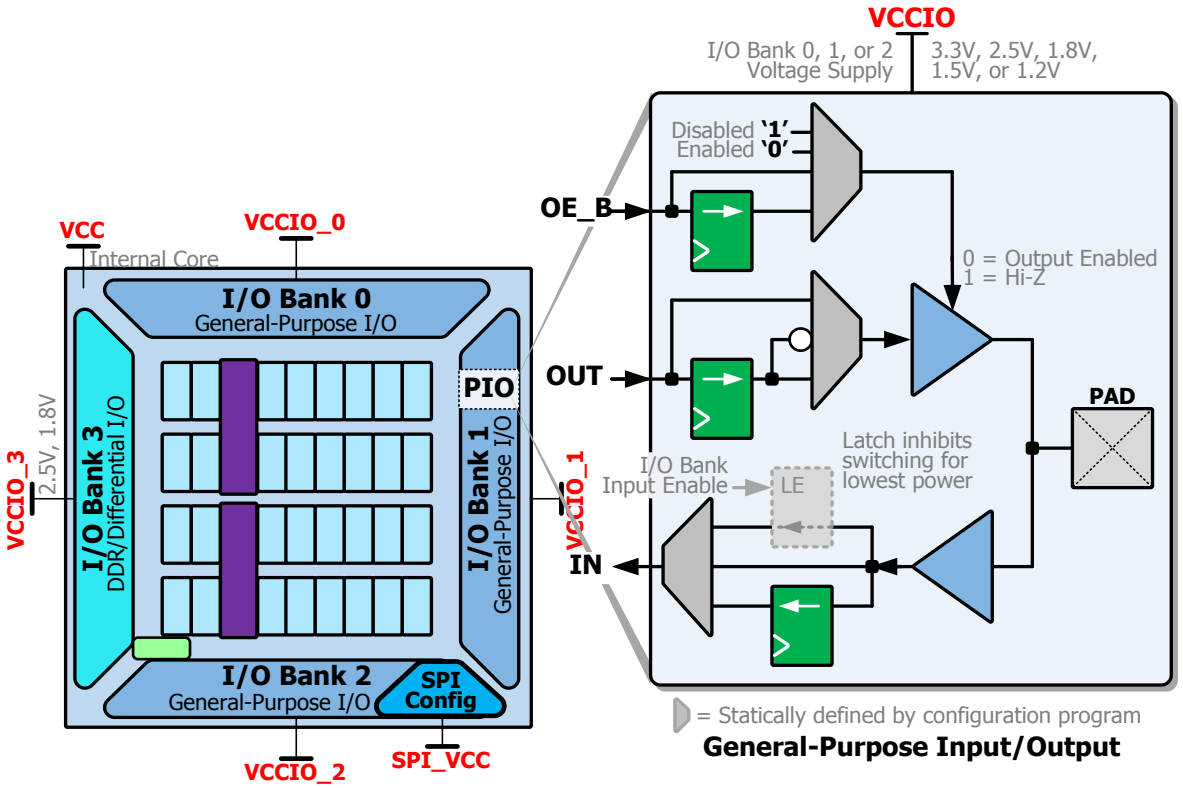
$$A - 2 = A + (-2)$$



Programmable Input/Output

PIO

Programmable I/O



- Four independent I/O banks
  - Independent voltage inputs
  - Multi-standard support

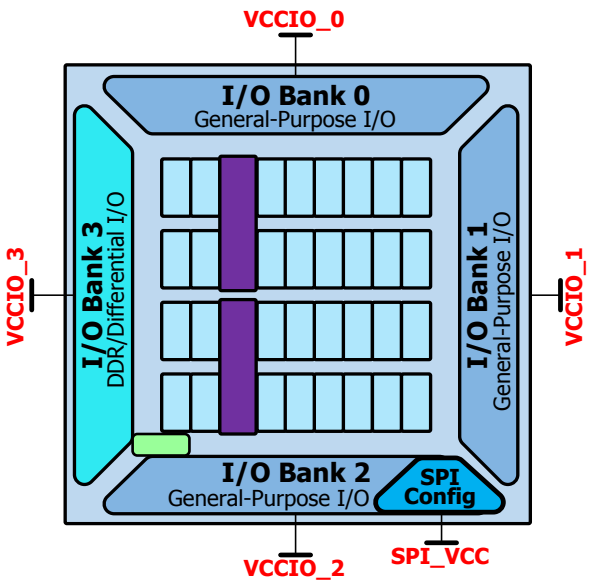
- Input, Output, or Bi-directional
- Flip-flops on all paths
  - DDR option
- Low-power latch option
- JTAG boundary scan

Four+ I/O Banks

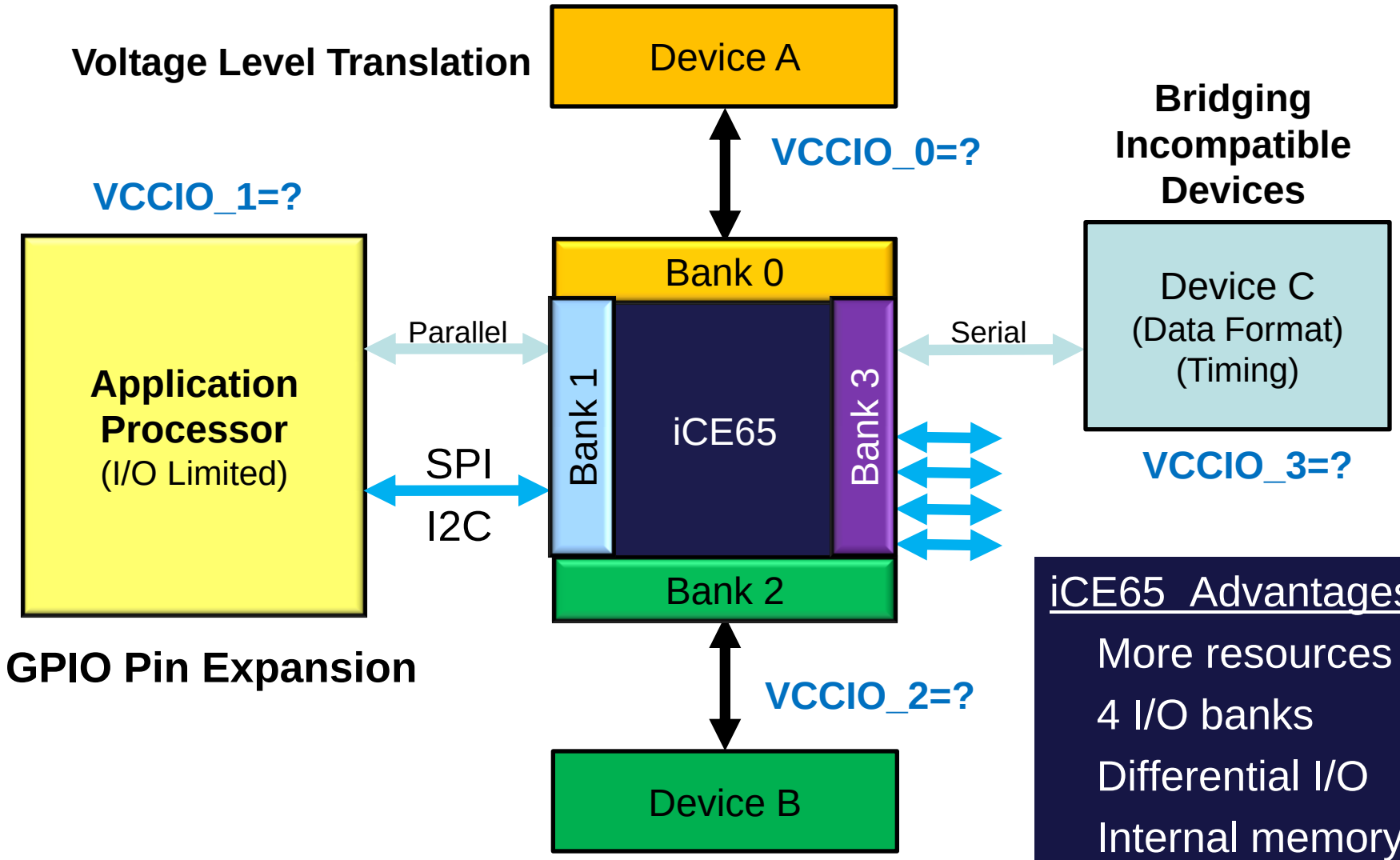
iCE65 I/O Bank Voltage Support

I/O Bank	5V tolerant	3.3V	2.5V	1.8V	1.5V
0 (top)	Yes	Yes	Yes	Yes	—
1 (right)	Yes	Yes	Yes	Yes	—
2 (bottom)	Yes	Yes	Yes	Yes	—
3 (left)	—	—	Yes	Yes	Yes
SPI	Yes	Yes	Yes	Yes	—

- Support up to four different I/O voltages
- Ideal for voltage level translation
  - Almost pay for voltage translation get a free FPGA
- Supported on iCEman65 board



Voltage Level Translation



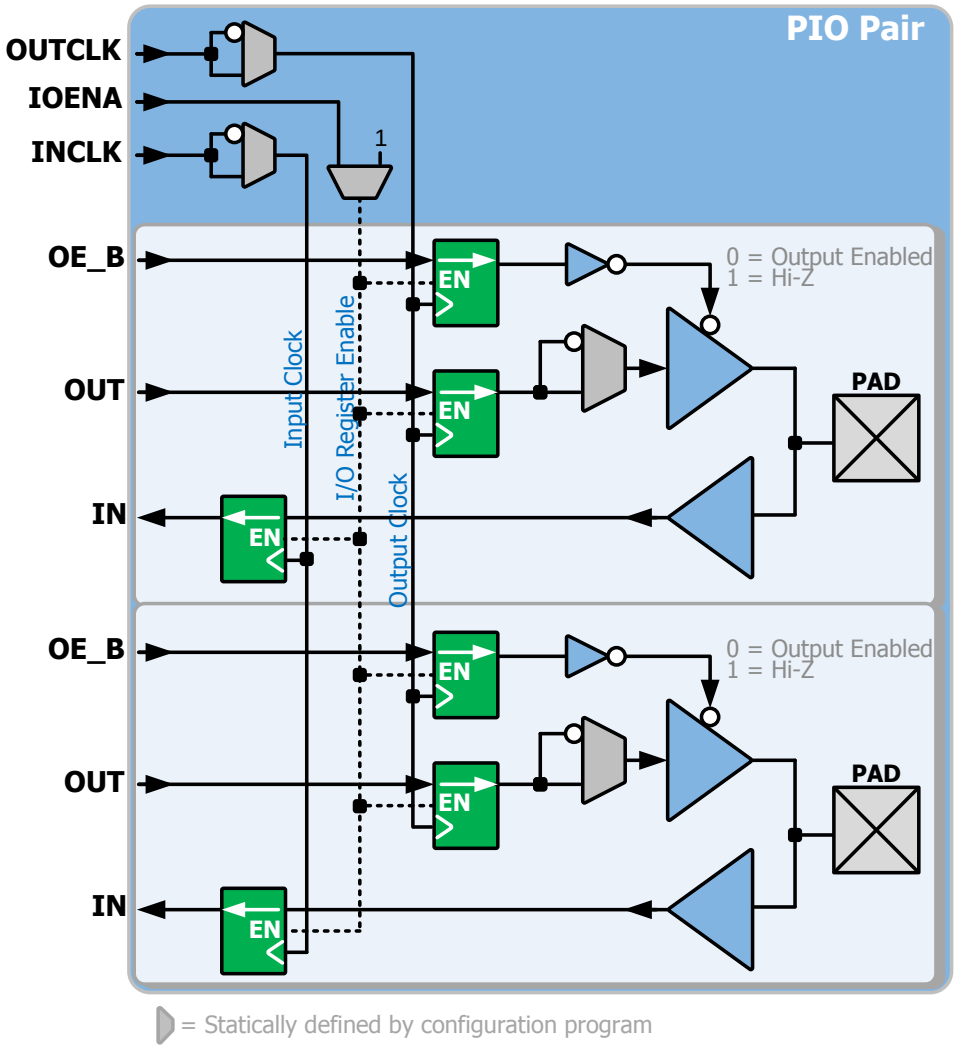
Specialty Standards in Bank 3

Application	I/O Standard	VCCIO_3 Supply Voltage	Drive Current (mA)
DDR1 SDRAM	SSTL2_II	2.5V	± 16.2
	SSTL2_I	2.5V	± 8.1
DDR2 SDRAM	SSTL18_II	1.8V	± 16.2
	SSTL18_I	1.8V	± 8.1
Mobile DDR	MDDR	1.8V	
Differential	LVDS	2.5V	

- All specialty voltage standard support is in I/O Bank 3

Programmable I/O Pair

- I/O pair **shares** control signals
  - Input clock
  - Output clock
  - Enable
- Input and output flip-flops are optionally Double Data Rate (DDR)
  (described later)



Double Data Rate (DDR)

- Basic Idea: Communicate twice as much data over a pin by using both edges of the clock
- Keeps internal frequency more manageable
- Saves power because clock transitions at half the frequency

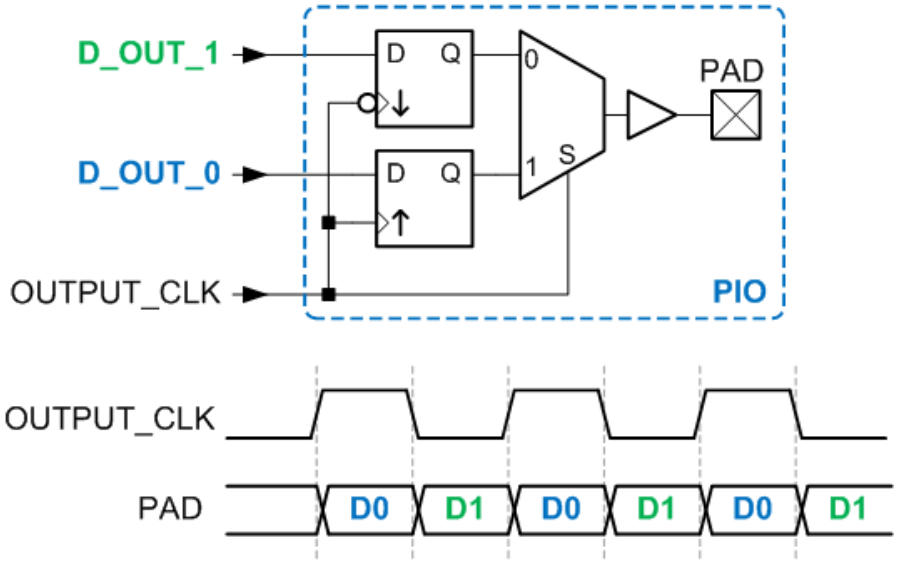
Dynamic Power = Activity ● **Frequency** ● Capacitance ● $(\text{Voltage})^2$

- Commonly used in DDR, DDR2 memories and with LVDS differential signaling

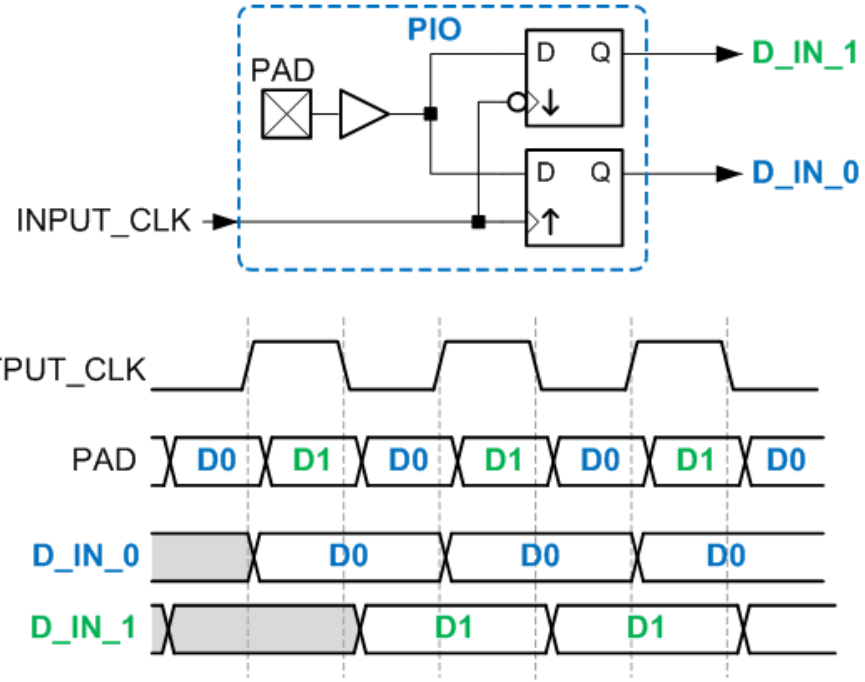
iCE65 DDR Flip-Flops in PIO

- Every PIO has two sets of DDR flip-flops
  - Input pair
  - Output
- Cannot be used when using JTAG boundary scan

Output DDR Pair



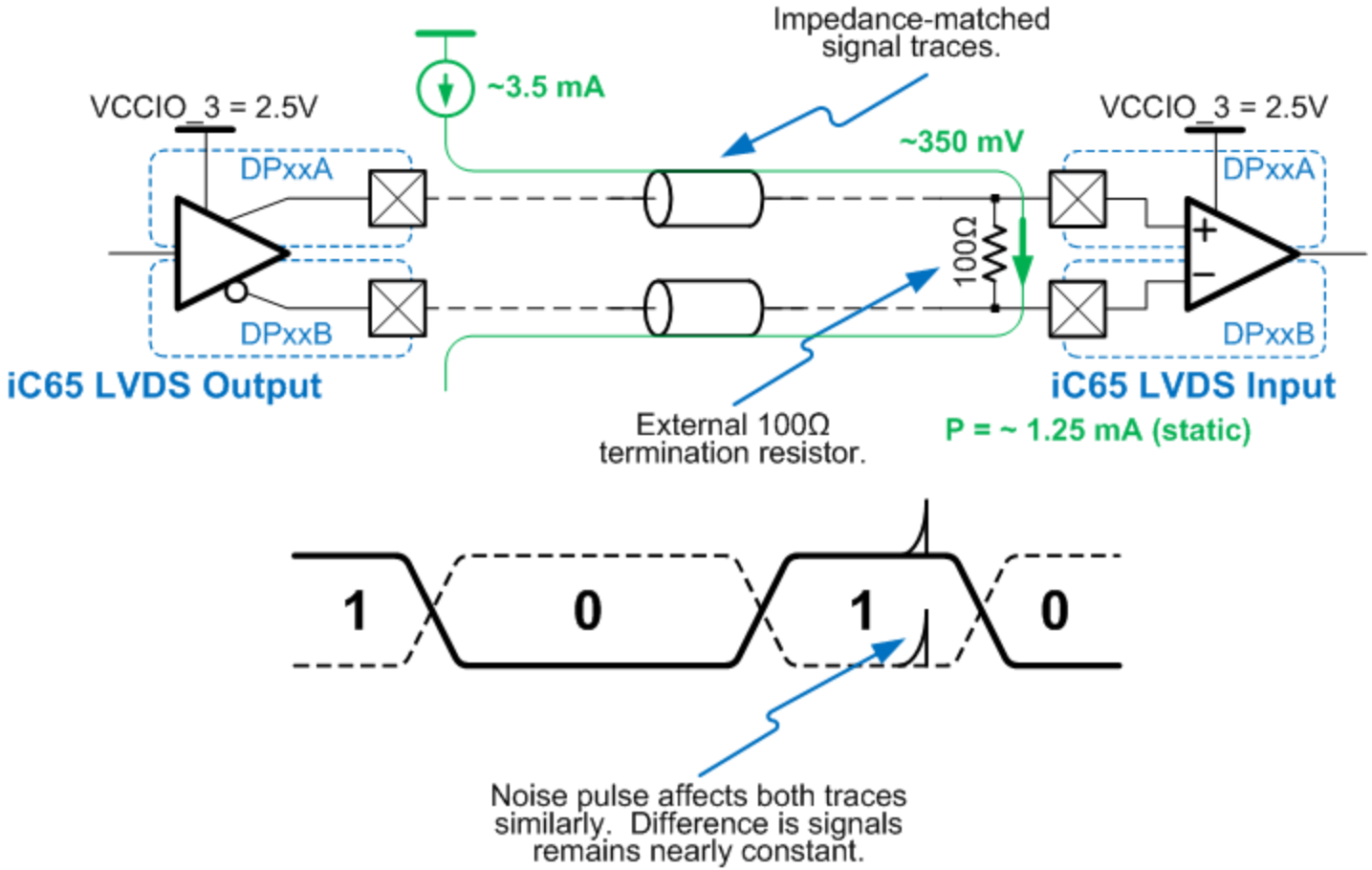
Input DDR Pair



LVDS Differential I/O

- Basic Idea: Send data over a few high-speed, carefully controlled traces than over many, lower-speed traces
- Low-voltage Differential Signaling (LVDS)
  - Low-power, high-speed I/O standard
  - Excellent noise immunity
  - Reduced EMI noise
- Popular for some applications
  - Higher-resolution graphic displays
  - Telecommunications
  - High-speed cameras

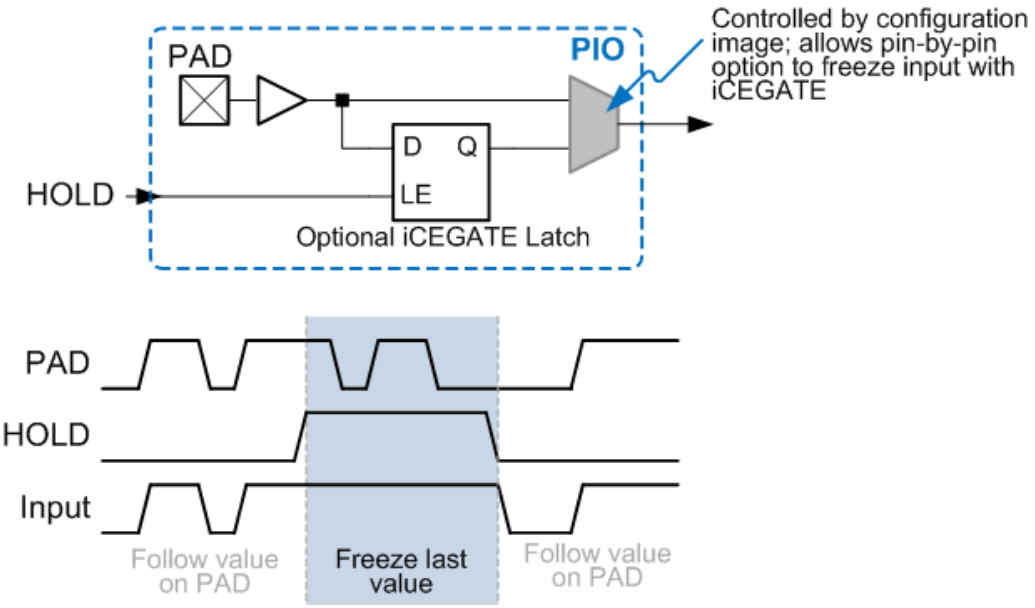
iCE65 LVDS



- Supported in I/O Bank 3, VCCIO_3 = 2.5V
- Receiver requires external 100Ω resistor

iCEGATE Input Latch

- Save power: Selectively freeze input signals
- One HOLD control per I/O Bank
  - Internal routing connection
  - Connect to a PIO, logic, or other HOLD signals

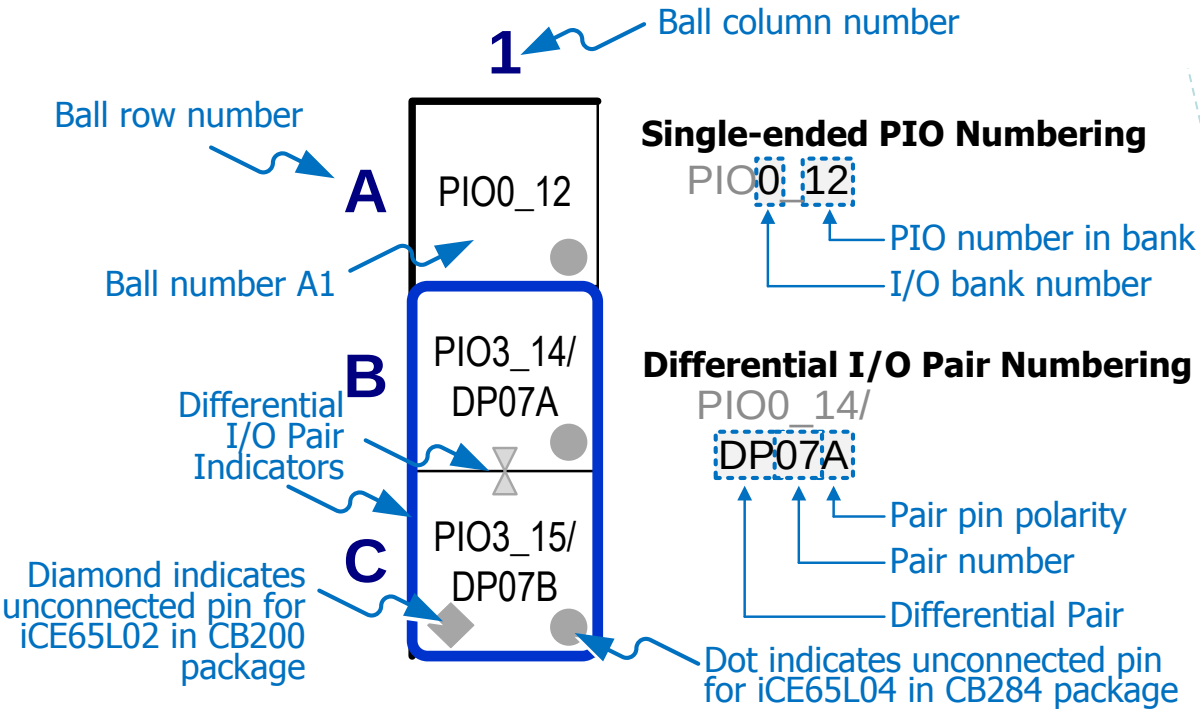


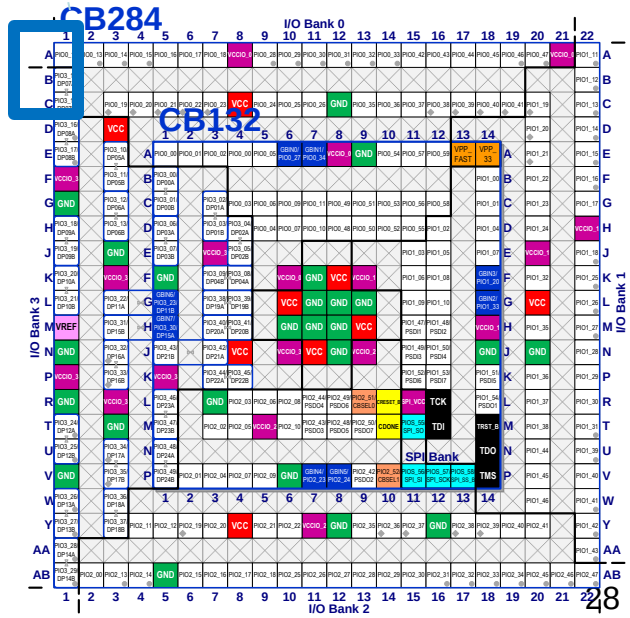
- Configuration image determines whether an input freezes with iCEGATE or not
  - Pin-by-pin control

PAD	HOLD	Input
PAD	0	PAD
X	1	Last value of PAD

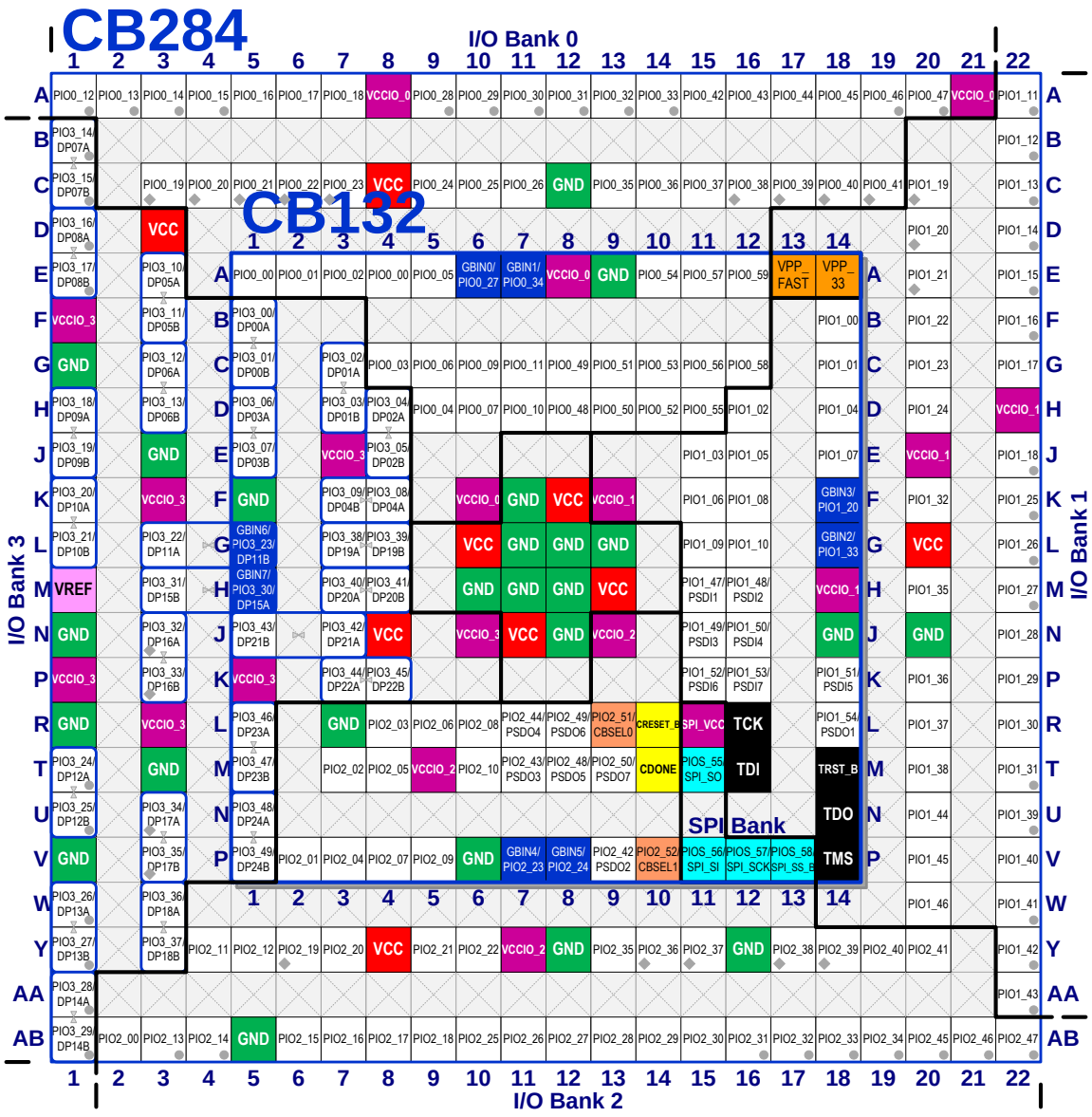
- Really only applicable to asynchronous input signals
  - Clocked inputs are already frozen until the next clock edge

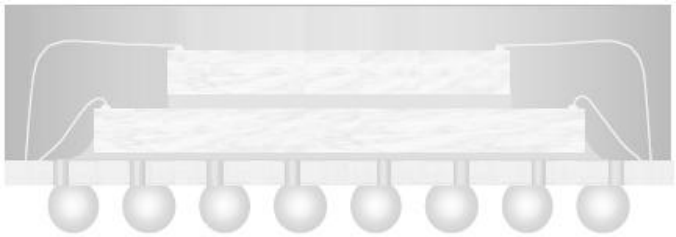
Pin Naming


Ball column number
1
Ball row number
A
Ball number A1
PIO0_12
B
PIO3_14/
DP07A
Differential
I/O Pair
Indicators
C
PIO3_15/
DP07B
Diamond indicates
unconnected pin for
iCE65L02 in CB200
package
Single-ended PIO Numbering
PIO 0 12
PIO number in bank
I/O bank number
Differential I/O Pair Numbering
PIO0_14/
DP07A
Pair pin polarity
Pair number
Differential Pair
Dot indicates unconnected pin
for iCE65L04 in CB284 package


CB284
CB132
I/O Bank 0
I/O Bank 1
I/O Bank 2
I/O Bank 3
SPI Bank

CB132/284 Common Footprint



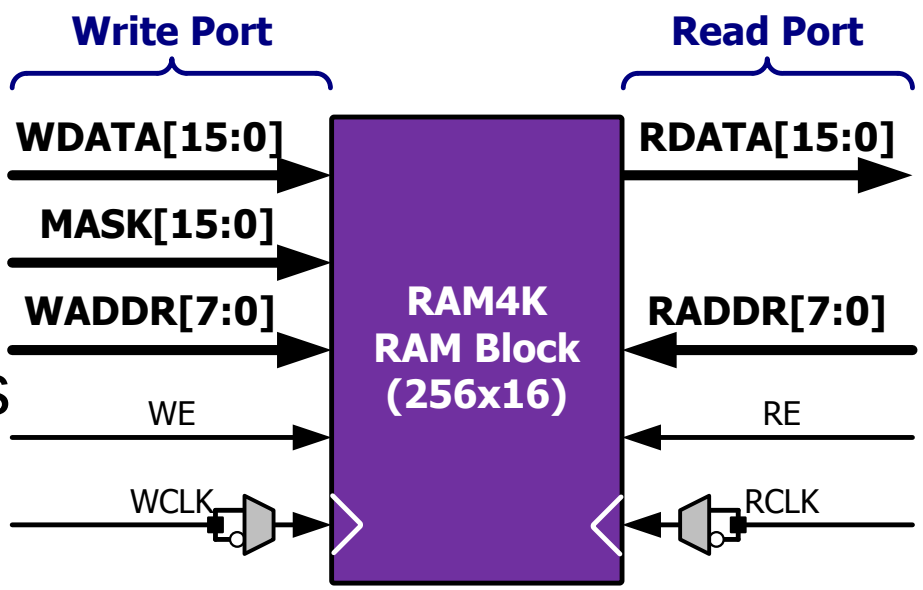


4Kbit Block RAM Memory

RAM4K

On-Chip RAM Blocks

- RAM4K memory blocks
  - 256 by 16-bit
  - Other formats available using programmable logic
- Separate read / write ports
- Optionally pre-initialized during configuration



Device	RAM4K Blocks	Default Configuration	RAM bits per Block	Total RAM Bits
iCE65L02	16	256 locations x 16 bits/location	4K (4,096)	64K
iCE65L04	20			80K
iCE65L08	32			128K
iCE65L16	96			384K

RAM4K Applications

- Data buffering
  - First-in, First-Out (FIFO)
  - Last-in, First-Out (LIFO, stack)
  - Circular buffers
  - Line buffers
- Register files
- Waveform generator
  - 256 x 16 ROM
- Function generator
  - “Super, synchronous PLB”
  - 8-inputs, 16 outputs
- Pattern matcher, correlator
- Counter
- Shift register

RAM Competitive Advantage

	SiliconBlue	Actel	Altera	Xilinx	Lattice
Family	iCE65	Igloo	MAX IIZ	CoolRunner-II	MachXO
Block RAM	Yes	In some parts	None	None	None
Block RAM Size	4Kx1	4Kx1 + parity	—	—	—
Number of RAM blocks	16 to 96	0: AGL015, 030 4 to 32 in larger devices	0	0	0
Block RAM bits	64K to 384K	0: AGL015,030 18K to 144K in larger devices	0	0	0

Write Operations

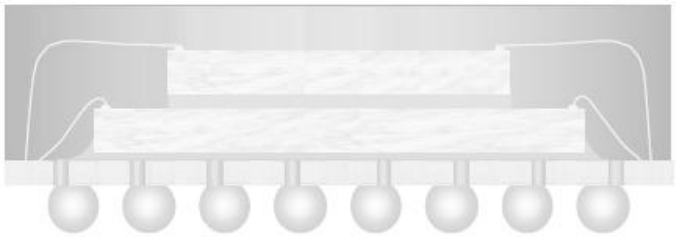
- MASK input masks off specific bits, prevents write to the specific bits in the RAM location
- All write operates are synchronized to clock input
- Write Clock is invertible (rising edge operation shown)

Operation	WDATA Data	MASK Bit Mask	WADDR Address	WE Enable	WCLK Clock	RAM Location
Disabled	X	X	X	X	0	No change
Disabled	X	X	X	0	X	No change
Write Data	WDATA[i]	MASK[i]=0	WADDR	1	↑	RAM[WADDR][i] = WDATA[i]
Masked Write	X	MASK[i]=1	WADDR	1	↑	RAM[WADDR][i] = No Change

Read Operations

- RAM contents optionally loaded during configuration
- RDATA output register not cleared by configuration reset
  - Valid read operation makes RDATA valid
- Write Clock is invertible (rising edge operation shown)

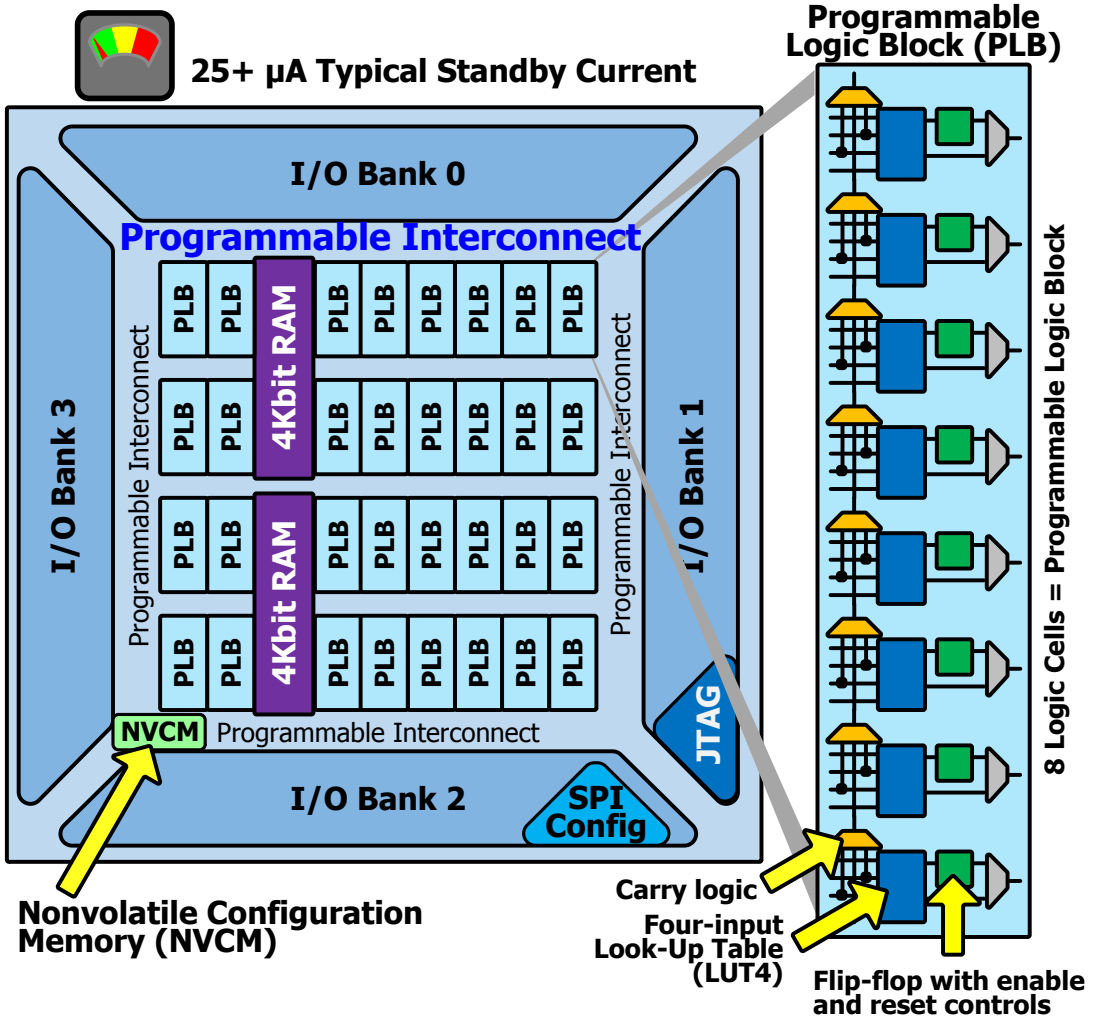
Operation	RADDR Address	RE Enable	RCLK Clock	RDATA
Immediately after configuration, before first Read operation	X	X	X	Undefined. Output register not cleared by configuration reset.
Disabled	X	0	X	No change
Read Data	RADDR	1	↑	RAM[RADDR]



PROGRAMMABLE INTERCONNECT

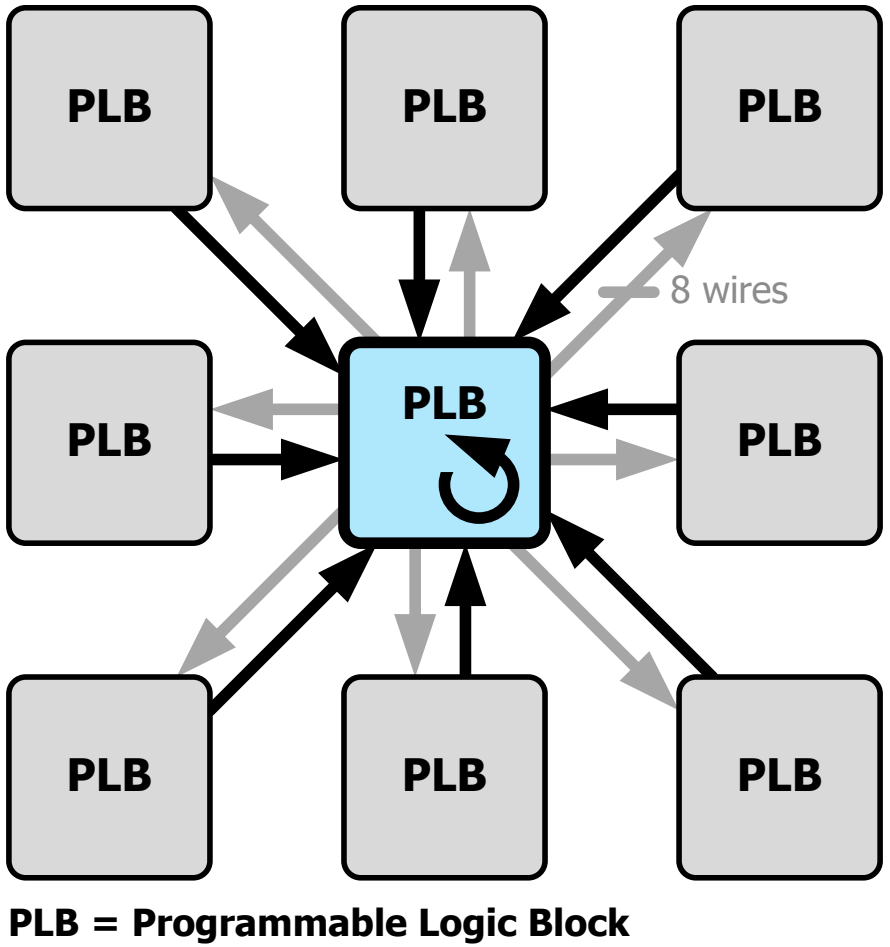
Programmable Interconnect

- Specially designed for ultra-low power
- Connections to Nearest Neighbors
- Connections that span four blocks
- Connections that span 12 blocks
- Global connections

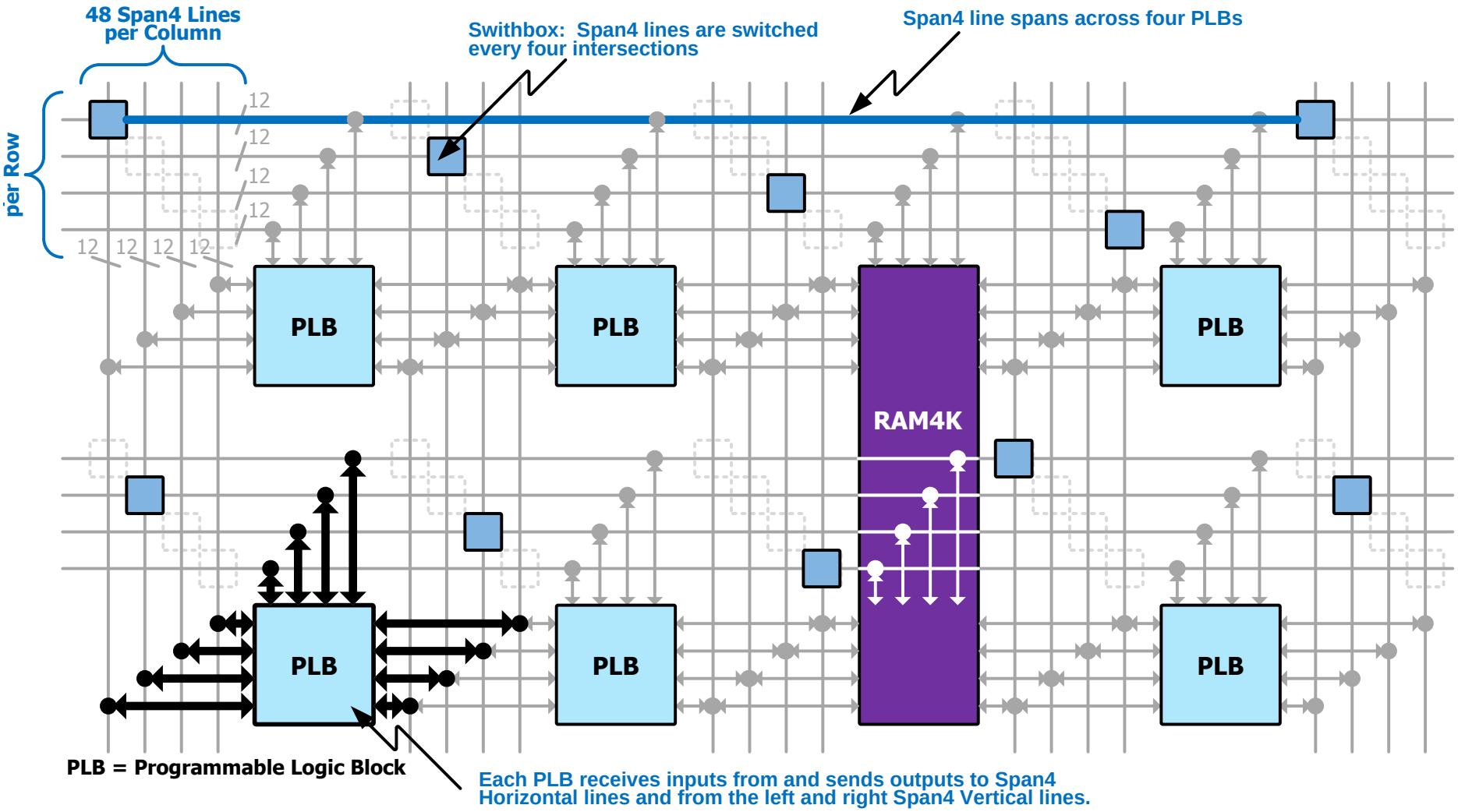


Nearest Neighbor Connections

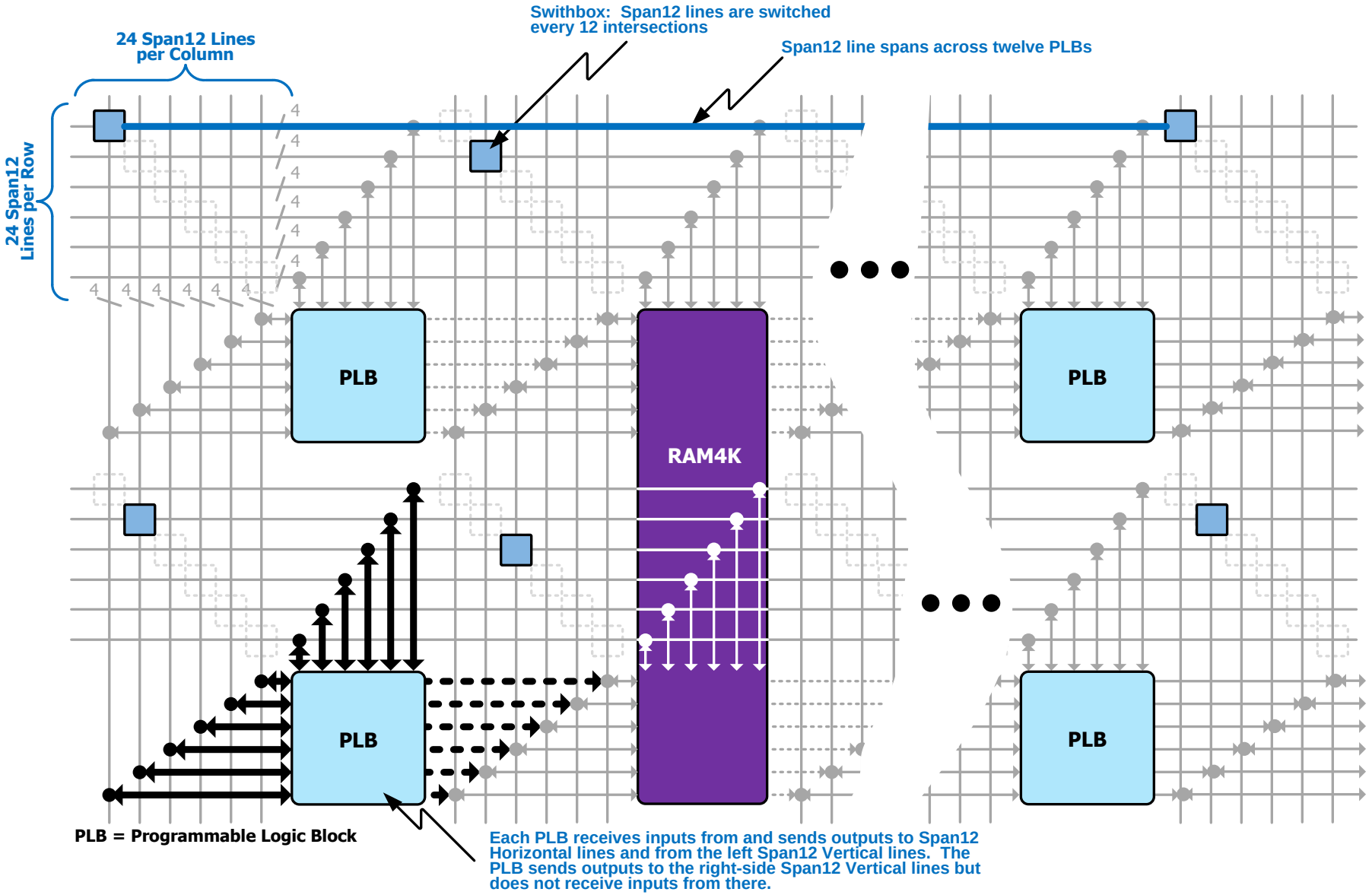
- Each PLB has connections to:
  - Itself
  - Eight nearest neighbors
- Fastest connections



Span4 Connections

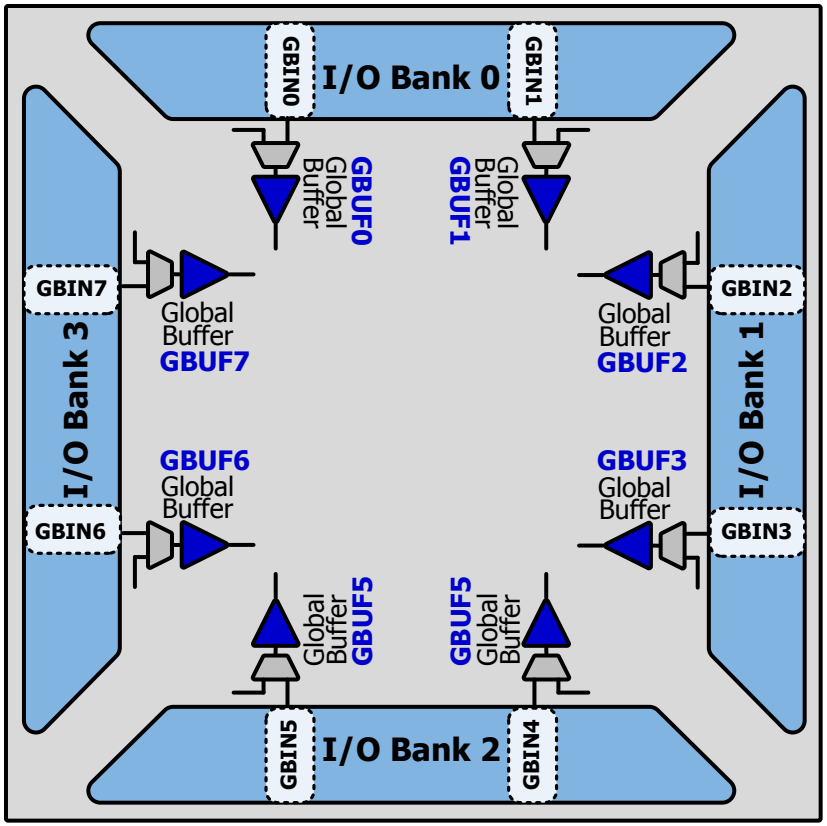


Span12 Connections

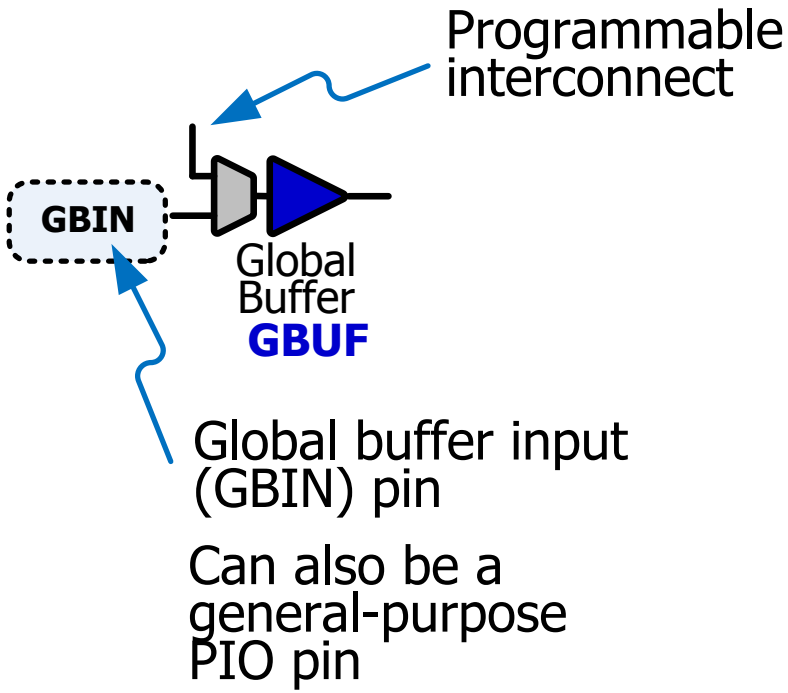


iCE65 Global Resources

- Eight high-drive, low-skew buffers
  - Potentially connect to all PLB, RAM4K, and PIO blocks
  - Clock drivers
  - High-fanout signals
- Global set/reset
  - Automatic at power-up
  - Resets all flip-flops to a known state



Global Buffer Inputs (GBIN)



- Global buffers (GBUFs) have two potential input sources
  - Special Global Buffer Input (GBIN) associated with a GBUF
  - From programmable interconnect
- Special GBIN pins also available for general-purpose I/O

Global Buffer to PLB

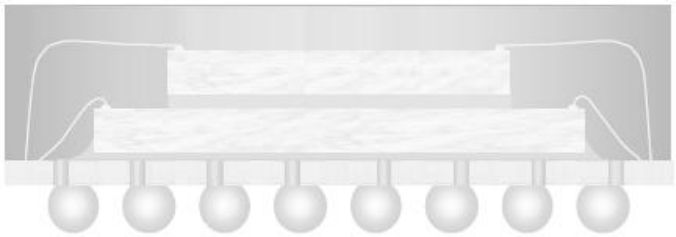
- GBUFs available as LUT4 inputs
- GBUFs available to all clock inputs
- Even-numbered GBUFs available to Set/Reset
- Odd-numbered GBUFs available to Enable

Global Buffer	LUT4 Inputs	PLB Clock	PLB Enable	PLB Set/Reset
GBUF0	Yes, any 4 of the 8 global buffers	■	N/A	■
GBUF1		■	■	N/A
GBUF2		■	N/A	■
GBUF3		■	■	N/A
GBUF4		■	N/A	■
GBUF5		■	■	N/A
GBUF6		■	N/A	■
GBUF7		■	■	N/A

Global Buffer to PIO

- GBUFs cannot directly connect to PIO output
  - Must connect through Logic Cell first
- GBUFs available to all input and output clocks
- Even-numbered GBUFs available to Clock Enable

Global Buffer	PIO Output	Input Clock	Output Clock	Clock Enable
GBUF0	Not available (connect through Logic Cell first)	■	■	■
GBUF1		■	■	N/A
GBUF2		■	■	■
GBUF3		■	■	N/A
GBUF4		■	■	■
GBUF5		■	■	N/A
GBUF6		■	■	■
GBUF7		■	■	N/A



SPI and NVCM

CONFIGURATION

iCE65 Device Configuration

- iCE65 FPGAs offer multiple configuration options to meet your application requirements
  - Secure, on-chip Non-Volatile Configuration Memory (NVCM)
  - Self-loading from an external, commodity SPI serial Flash PROM
  - Downloaded from external processor using SPI-like serial interface
  - SPI interface has separate voltage supply to simplify system interface
  - Internal oscillator and power-on reset

iCE65 Configuration Models

Self-Contained Model (ASIC, Microcontroller)

- Lowest-cost
- Single-chip, secure; loads from internal NVCM memory
- Permanently programmed (with reprogrammable options)

Processor Model

- Boot at power-up from external SPI serial Flash
- Optionally store additional application data in Flash
- Changeable program

Peripheral Model

- Download to iCE65 using a controller/processor
- Simple SPI interface
- iCE65 bitstream stored in any form of memory
  - Internal Flash, Disk drive
  - Over network, RF link
- Changeable program

How Many Bits to Program?

- Regardless of design complexity, configuration image size is the same per device

iCE65 Configuration Image Size

Device	Kbits	Mbits	Kbytes
iCE65L02	314 Kb	0.31 Mb	39.3 KB
iCE65L04	533 Kb	0.52 Mb	62.7 KB
iCE65L08	1,057 Kb	1.03 Mb	132.2 KB
iCE65L16	2,404 Kb	2.35 Mb	300.5 KB

Internal Oscillator

- Clock source for self-loading modes
  - NVCM
  - SPI serial Flash
- Mode determines operating frequency, but wide variance
  - Maximum frequency determines which PROM is required
  - Minimum frequency determines how fast configuration completes
- Turned off after configuration to save power

Mode	Minimum	Maximum	Description
Default	3.3 MHz	10 MHz	Works with any SPI PROM
Low	11 MHz	33 MHz	Works with most SPI PROMs
High	17 MHz	50 MHz	Supported by some high-speed SPI PROMs

How Long to Configure?

- Speed depends on internal oscillator setting or external clock frequency
- Maximum configuration time depends on
  - Configuration image size
  - Lowest frequency for configuration clock

iCE65 Maximum Configuration Time

Device	Internal Oscillator			Download Clock	
	Default	Low Frequency	High Frequency	25 MHz	40 MHz
iCE65L02	98 ms	30 ms	19 ms	13 ms	9 ms
iCE65L04	166 ms	50 ms	33 ms	22 ms	14 ms
iCE65L08	328 ms	99 ms	64 ms	44 ms	28 ms
iCE65L16	746 ms	224 ms	145 ms	99 ms	62 ms

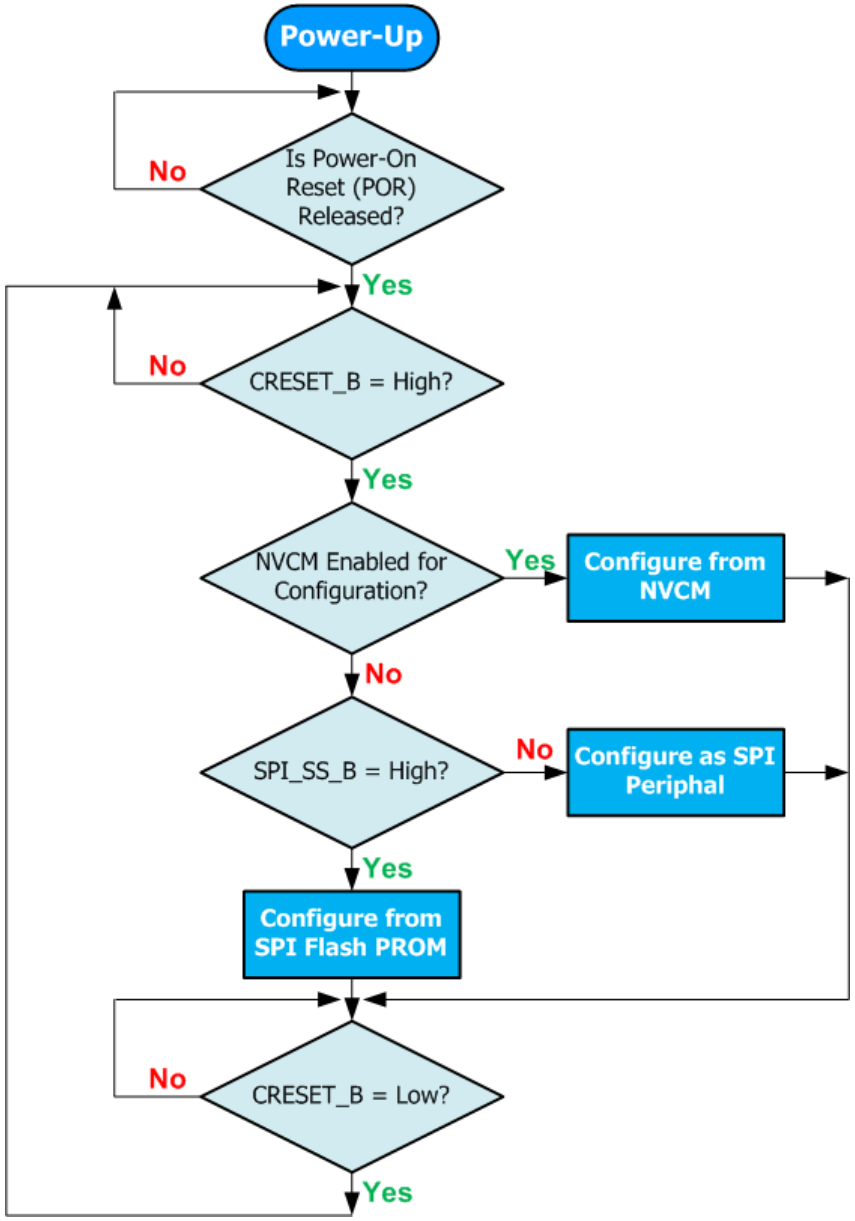
NVCM Programming

- NVCM memory is large enough to completely program device plus initialize on-chip RAM
  - Low cost; permanently programmed
  - Completely internal, secure
- Programming interface similar to 25-series SPI PROM
- External programming support
- In-system programming (ISP) also available
  - 2.5V-only with on-chip programming circuitry
  - Faster programming using separate 6.5V supply

Pin	Voltage	Description
VDDP_2V5	2.5V	Charge pumped programming voltage supply.
VPP_6V5	6.5V	Direct, faster programming voltage supply.

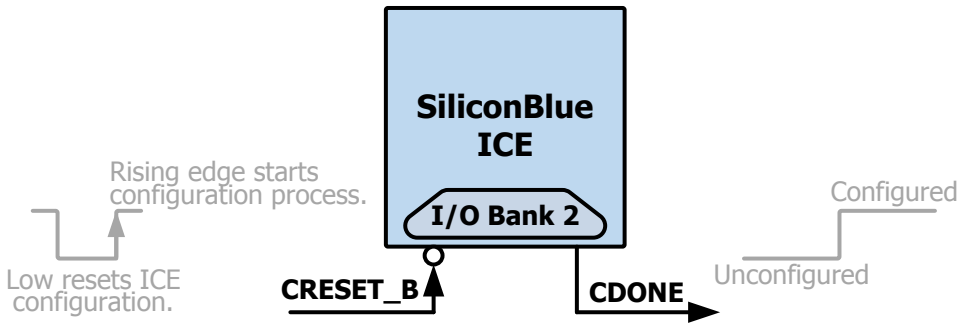
Selecting Mode

- Configuration mode decided by a few variables
  - Is NVCM enabled for configuration?
  - What is the logic value on the SPI_SS_B pin?
    - Low: Peripheral mode
    - High: SPI Flash PROM



Configuration Control

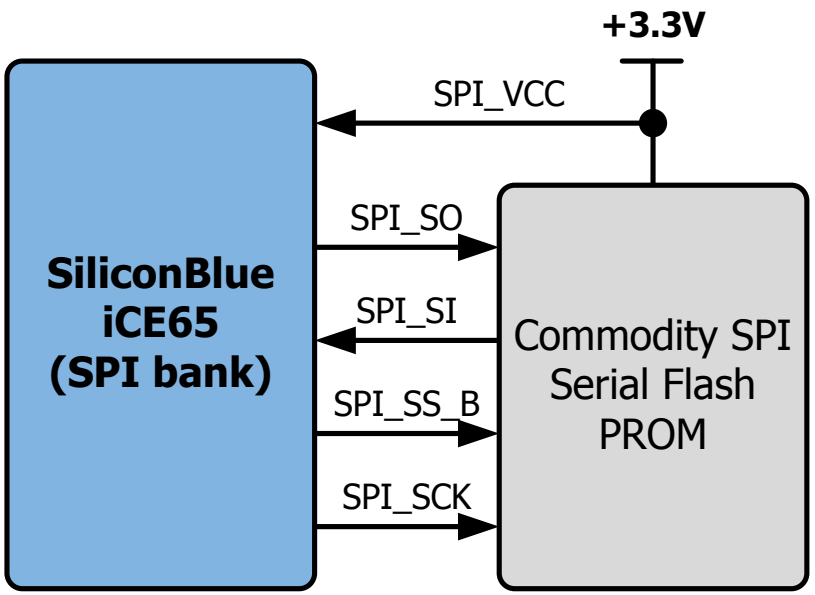
- Built-in Power-On Reset (POR)
- Internal oscillator for self-loading mode
  - Three frequency ranges
- CRESET_B: Asynchronous, active-Low reset
  - Keep Low to postpone start of configuration
  - Configuration starts when CRESET_B returns High



- CDONE: Low during configuration, High when configuration complete
  - Low-current output

SPI Serial PROM Interface

- Separate I/O bank to simplify system design
- Supports multiple commodity SPI Flash vendors
  - Competitive pricing
  - Multi-sourcing security

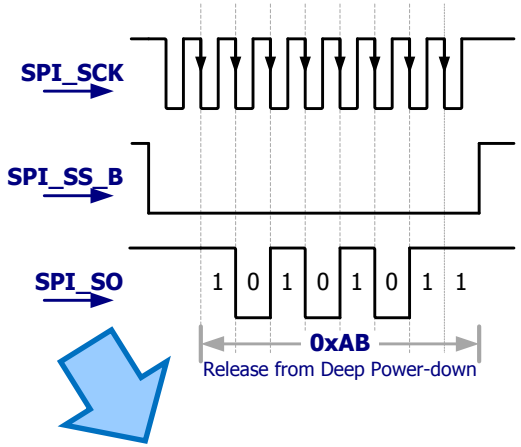


- Same SPI interface for peripheral mode configuration

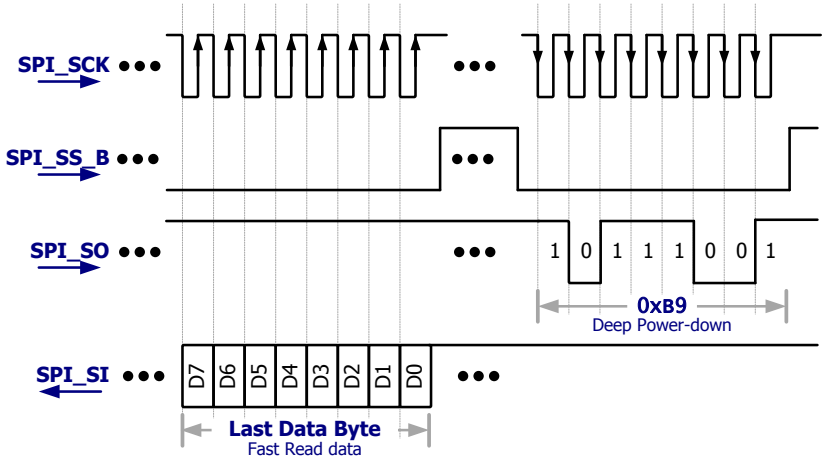
Signal Name	Flash Mode	Peripheral Mode	After Configuration	Configuration Function
SPI_SO	Output	Output	User-defined PIO	Serial Output
SPI_SI	Input	Input	User-defined PIO	Serial Input
SPI_SS_B	Output	Input	User-defined PIO	Slave Select, active Low
SPI_SCK	Output	Input	User-defined PIO	Slave Clock

Low-Power SPI Configuration

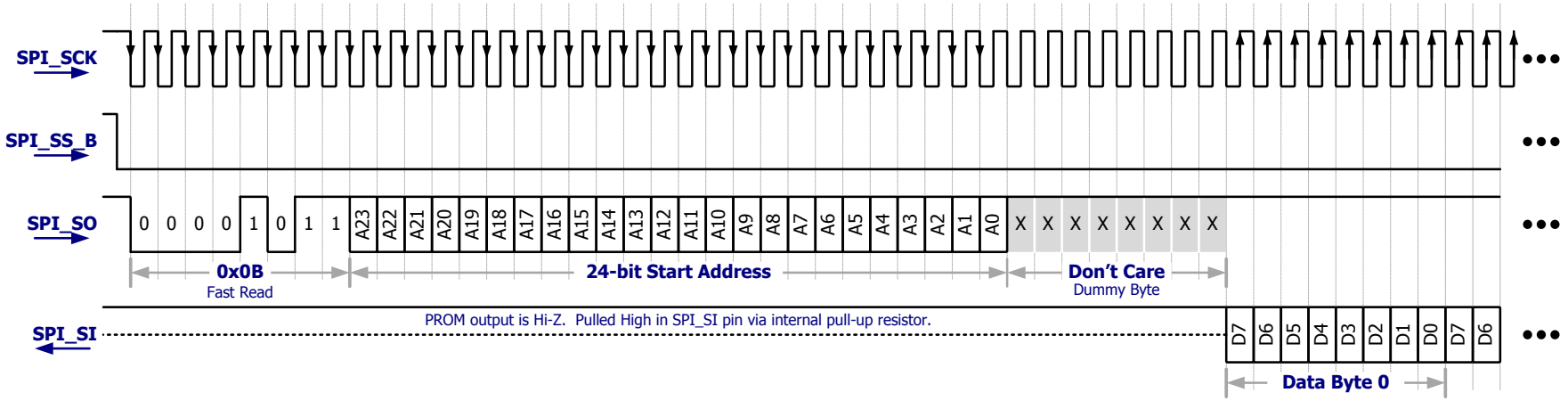
1 Wake up PROM from low-power mode



3 Return PROM to low-power mode (default, optional)



2 Send 0x0B Fast Read Command, 24-bit Start Address, Read Required Configuration Data

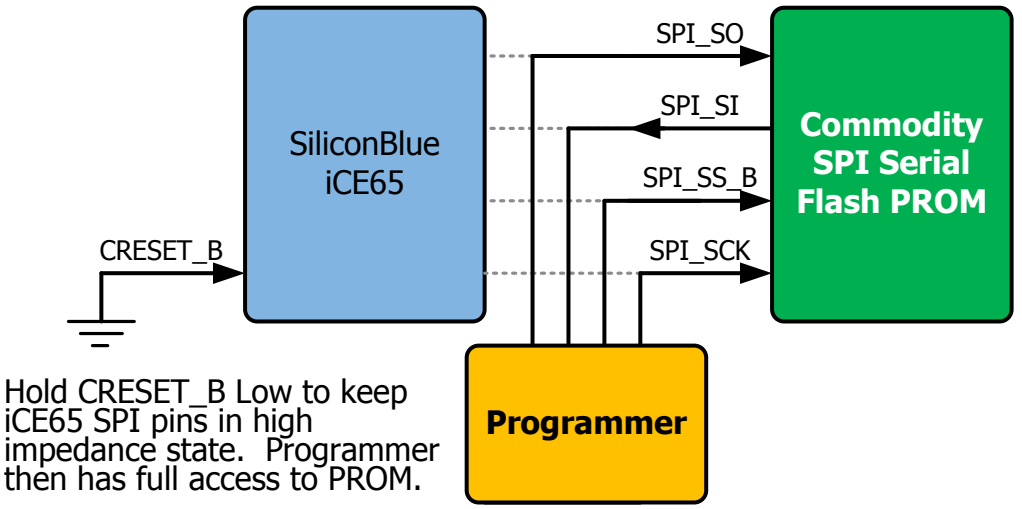


SPI PROM Requirements

- iCE65 optional loads from commodity SPI serial Flash
  - Multiple vendors with compatible devices
  - Lowest pricing; supply security
  - Innovative features and packaging
- Requirements
  - 25- or 45-series SPI PROM
  - Large enough to hold a bitstream (512K to 4M)
  - Supports the Fast Read command (0x0B)
  - Fast enough power-up to ready time

Programming SPI Flash

- Hold CRESET_B Low
  - Tri-states all pins
  - Allows external programmer access to SPI Flash
- Built into iCEman65 board
- TotalPhase
  - Aardvark (lower-speed) www.totalphase.com/products/aardvark_i2cspi
  - Cheetah (high-speed) www.totalphase.com/products/cheetah_spi
  - Free Flash Center software www.totalphase.com/products/flash_center
- Digilent
  - JTAG-USB Cable www.digilentinc.com/Products/Detail.cfm?Prod=JTAG-USB&Nav1=Products&Nav2=Cables
  - Works with Adept/ICEUTIL



SPI Serial PROM Vendors

Tested

- Numonyx
  - Formerly STMicro/Intel
  - M25P40, M25P80
- Atmel
  - AT45DB081D

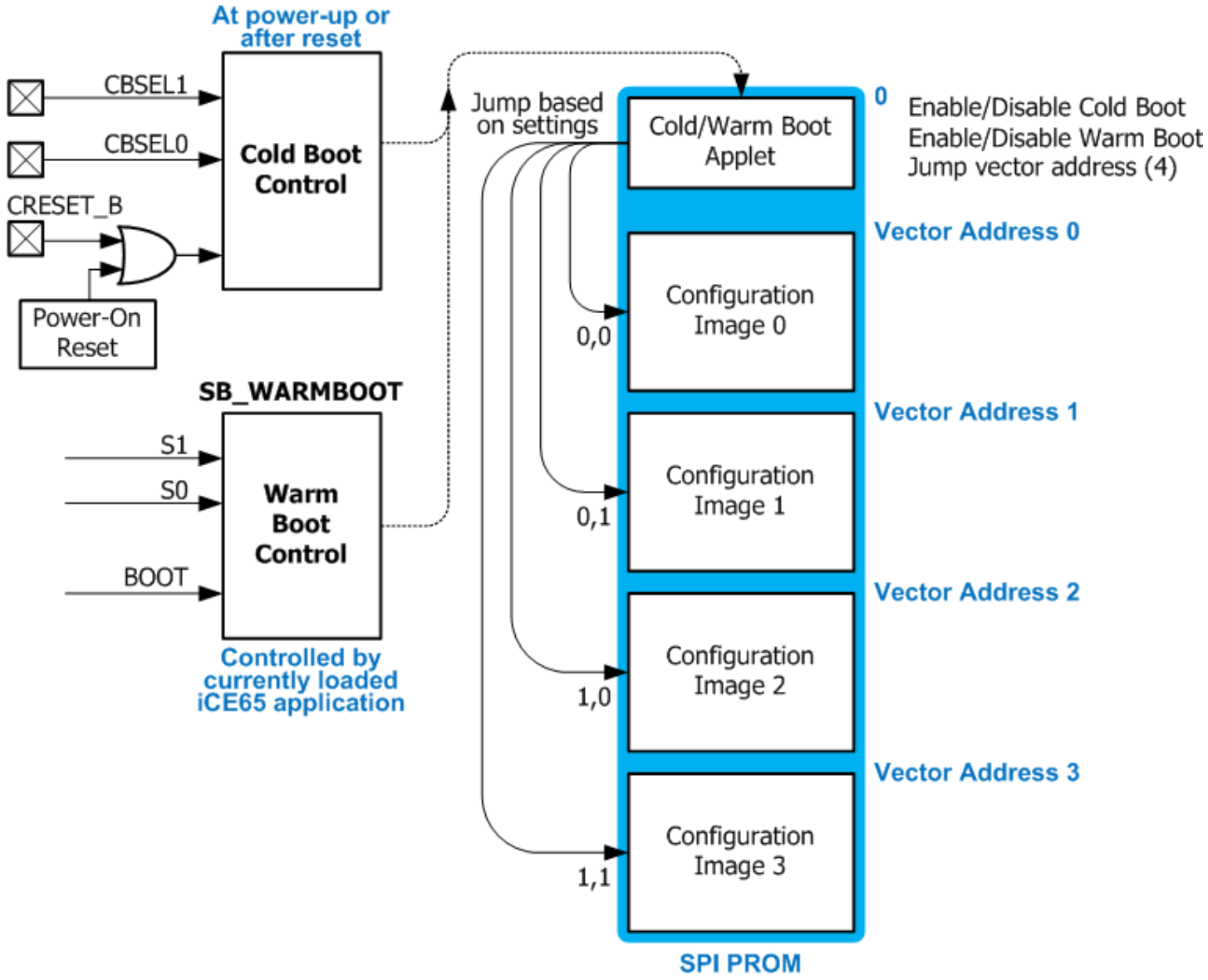
Not Yet Tested

- Spansion
  - Formerly AMD/Fujitsu
- Winbond
  - NexFlash
- Silicon Storage Technology (SST)
- Chingis
- Macronix
- Eon Silicon Solution
- AMIC Technology

Cold/Warm Boot

- Usually, iCE65 device programmed using a single configuration image
- Optionally select one of up to four iCE65 configuration images
  - **ColdBoot:** At power-on or after CRESET_B returns High, read value on CBSEL[1:0] pins to select four possible configuration bitstreams
  - **WarmBoot:** FPGA application selects one of four possible bitstreams, controls when to jump to next bitstream using SB_WARMBOOT primitive

Cold/Warm Boot Procedure

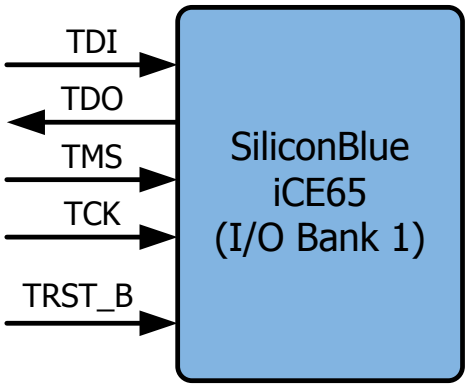


Cold/Warm Boot Examples

- Single hardware design has multiple functions
  - Board loads self-test design, then jumps to user application if test passes
  - Based on a card slot ID, the iCE65 FPGA is loaded with required hardware design
  - Time-share hardware, saves costs
- NVCM with Field Upgrade/Expansion Path
  - Load from NVCM
  - Optionally jump to SPI configuration image if available

JTAG/Boundary Scan

- Primarily used during PCB assembly
  - Open/short test
  - Especially useful with aggressive packaging
- Optional configuration interface (though many details are yet to be determined)
- Powered by VCCIO_1



TRST_B must be Low during normal operation.

Signal Name	Description
TDI	Test Data Input
TDO	Test Data Output
TMS	Test Mode Select
TCK	Test Clock
TRST_B	Test Reset (active Low)

Powering iCE65 FPGAs

- Core Voltage
  - 1.2 V: Standard
  - 1.0 V: Ultra-low power

Dynamic Power = Activity ● Frequency ● Capacitance ● **(Voltage)^2**

- Up to five different I/O voltages
  - Four I/O bank voltages
    - Banks 0, 1, 2 can be 3.3V, 2.5V, 1.8V
    - Bank 3 can be 2.5V, 1.8V, or 1.5V
  - SPI “mini-bank” voltage
    - 3.3V when configuring from SPI Flash
    - 2.5V and 1.8V options when configuring from NVCM or peripheral mode