iCE DiCE™: iCE65L08 Ultra Low-Power FPGA Known Good Die

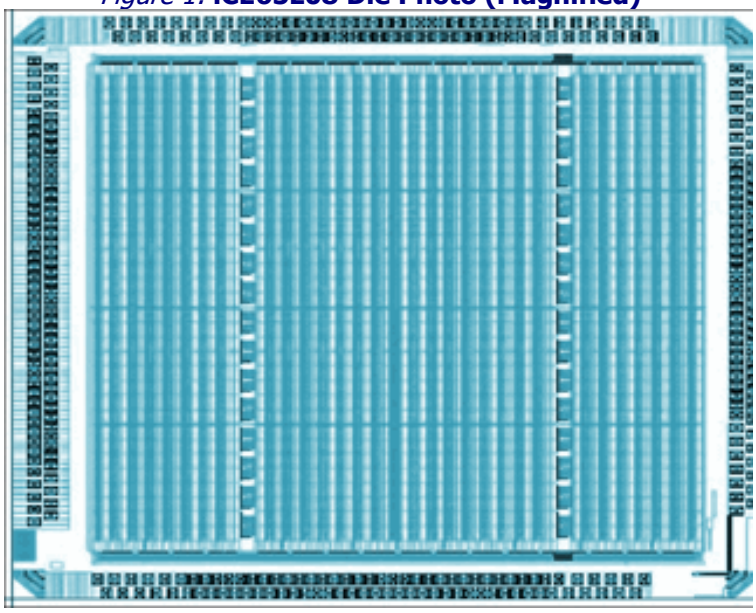
SiliconBlue®

January 25, 2009 (1.0) **Advance Information (SUBJECT TO CHANGE)**

Features

- **First ultra low-power programmable logic family specifically designed for hand-held applications and long battery life**
  - Less than 100 µA typical standby current; no special power down modes required
  - Lowest active power consumption of any comparable programmable logic family
  - Lowest heat dissipation on power-sensitive applications
- **Known Good Die (KGD)**
  - Ideal for System-in-Package (SiP), stacked-die, or multi-chip module applications
  - Ideal for Chip on Board (COB) mounting in low-cost consumer products
  - Various temperature range, thickness, and delivery method options
- **Reprogrammable from a variety of sources**
  - Self-loading from secure, internal Nonvolatile Configuration Memory (NVCM)
    - Superior design and intellectual property (IP) protection; no exposed configuration data
    - Single-chip programmable solution
    - Low-cost, high-volume configuration source
  - Self-loading from external, commodity SPI serial Flash PROM
  - Downloaded by processor using SPI-like serial interface
- **Built on proven, high-volume 65 nm, low-power CMOS technology delivering lowest possible power and cost**

Figure 1: **iCE65L08 Die Photo (Magnified)**



- **Up to 200+ MHz internal performance**
- **Flexible programmable logic and programmable interconnect fabric**
  - Over 7,600 four-input look-up tables (LUT4) and flip-flops
  - Low-power logic and interconnect
- **On-chip, 4Kbit RAM blocks; 32 per device**
- **Flexible I/O blocks to simplify system interfaces**
  - 222 programmable I/O pads
  - Four independently-powered I/O banks support 3.3V, 2.5V, or 1.8V voltage standards
  - Differential LVDS I/O pairs

Table 1: **iCE65 Ultra Low-Power Programmable Logic Family Summary**

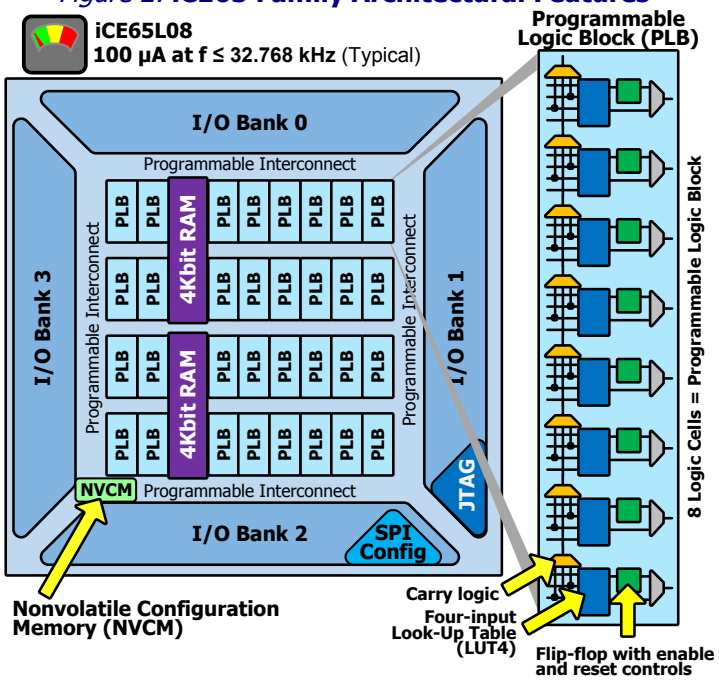
	iCE65L02	iCE65L04	iCE65L08	iCE65L16
Logic Cells (LUT + Flip-Flop)	1,792	3,520	7,680	16,896
Approximate System Gate Count	100K	200K	400K	800K
Typical Equivalent Macrocells	1,400	2,700	6,000	13,000
RAM4K Memory Blocks	16	20	32	96
RAM4K RAM bits	64K	80K	128K	384K
Configuration bits (Kbits maximum)	314 Kb	533 Kb	1,057 Kb	2,404 Kb
Typical Current at ≤ 32.768 kHz (-L)	**25 µA**	**50 µA**	**100 µA**	**250 µA**
Maximum Programmable I/O Pins	128	176	222	384
Maximum Differential I/O Pairs	16	20	25	54

Overview

The SiliconBlue Technologies iCE65 programmable logic family is specifically designed to deliver the lowest standby and dynamic power consumption of any comparable CPLD or FPGA device. iCE65 components are available in two versions. The standard product, designed for cost-sensitive, single-program, high-volume applications, provides on-chip, nonvolatile configuration memory (NVCM) to customize the iCE device for a specific application. Both the standard version with NVCM memory and the optional development version without NVCM memory can be self-configured from a program saved in an external commodity SPI serial Flash PROM or downloaded from an external processor over an SPI-like serial port.

The four iCE components, highlighted in Table 1 deliver from approximately 2K to nearly 17K logic cells and flip-flops while consuming a fraction of the power of comparable programmable logic devices. Each iCE device includes between 16 to 96 RAM blocks, each with 4Kbits of storage, for on-chip data storage and data buffering.

Figure 2: **iCE65 Family Architectural Features**



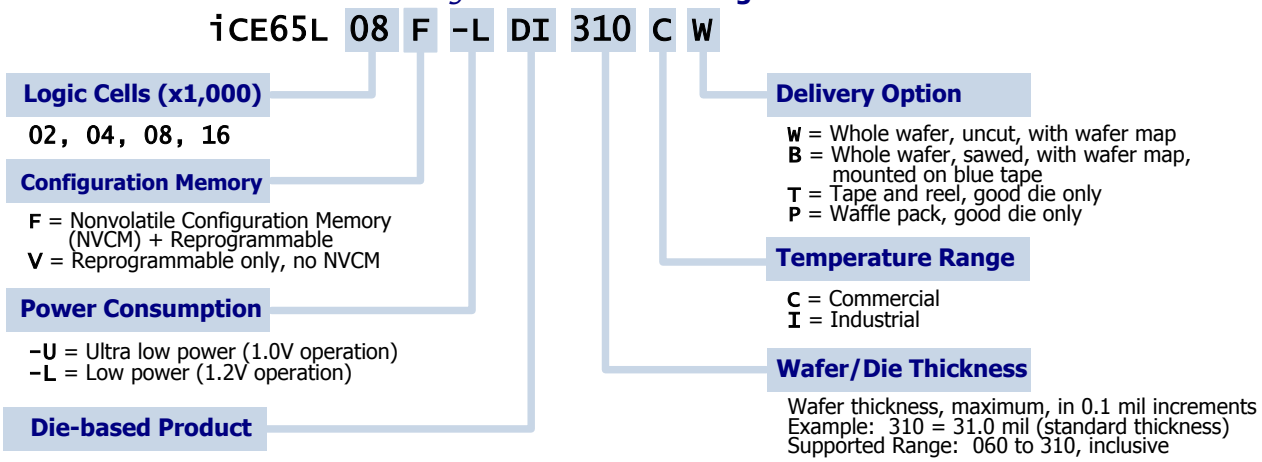
As pictured in Figure 2, each iCE device consists of four primary architectural elements.

- An array of Programmable Logic Blocks (PLBs)
  - Each PLB contains eight Logic Cells (LCs); each Logic Cell consists of ...
    - A fast, four-input look-up table (LUT4) capable of implement any combinational logic function of up to four inputs, regardless of complexity
    - A 'D'-type flip-flop with an optional clock-enable and set/reset control
    - Fast carry logic to accelerate arithmetic functions such as adders, subtracters, comparators, and counters.
  - Common clock input, clock-enabled input, and optional set/reset control input to PLB shared among all eight Logic Cells
- Two-port, 4Kbit RAM blocks (RAM4K)
  - 256x16 default configuration; selectable data width using programmable logic resources
  - Simultaneous read and write access; ideal for FIFO memory and data buffering applications
  - RAM contents pre-loadable during configuration
- Four I/O banks with independent supply voltage, each with multiple Programmable Input/Output (PIO) blocks
- Programmable interconnections between the blocks
  - Flexible connections between all programmable logic functions
  - Eight dedicated low-skew, high-fanout clock distribution networks

Ordering Information

Figure 3 describes the iCE65 die-based product ordering codes.

Figure 3: **iCE65 Ordering Codes**



iCE65 FPGA devices are available with two power consumption options. Standard products ("-L" ordering code) have low standby and dynamic power consumption. The "-U" option specifies the ultra low power version.

Please consult the die distributor or SiliconBlue Technologies Corporation before ordering to verify long-term availability of these die products.

Specifications discussed herein are subject to change without notice. This product is sold "as is" and is delivered with no guarantees or warranties, expressed or implied.

Die Samples

Die samples are available through an authorized SiliconBlue sales representative. Samples are provided untested, but with expected high yield (about 90%). Samples are delivered in waffle pack with 4 mil die thickness.

Functional Specifications

Please refer to the packaged product data sheet found on the SiliconBlue Technologies web site (www.siliconbluetech.com) for functional and parametric specifications. The specifications are provided for reference only.

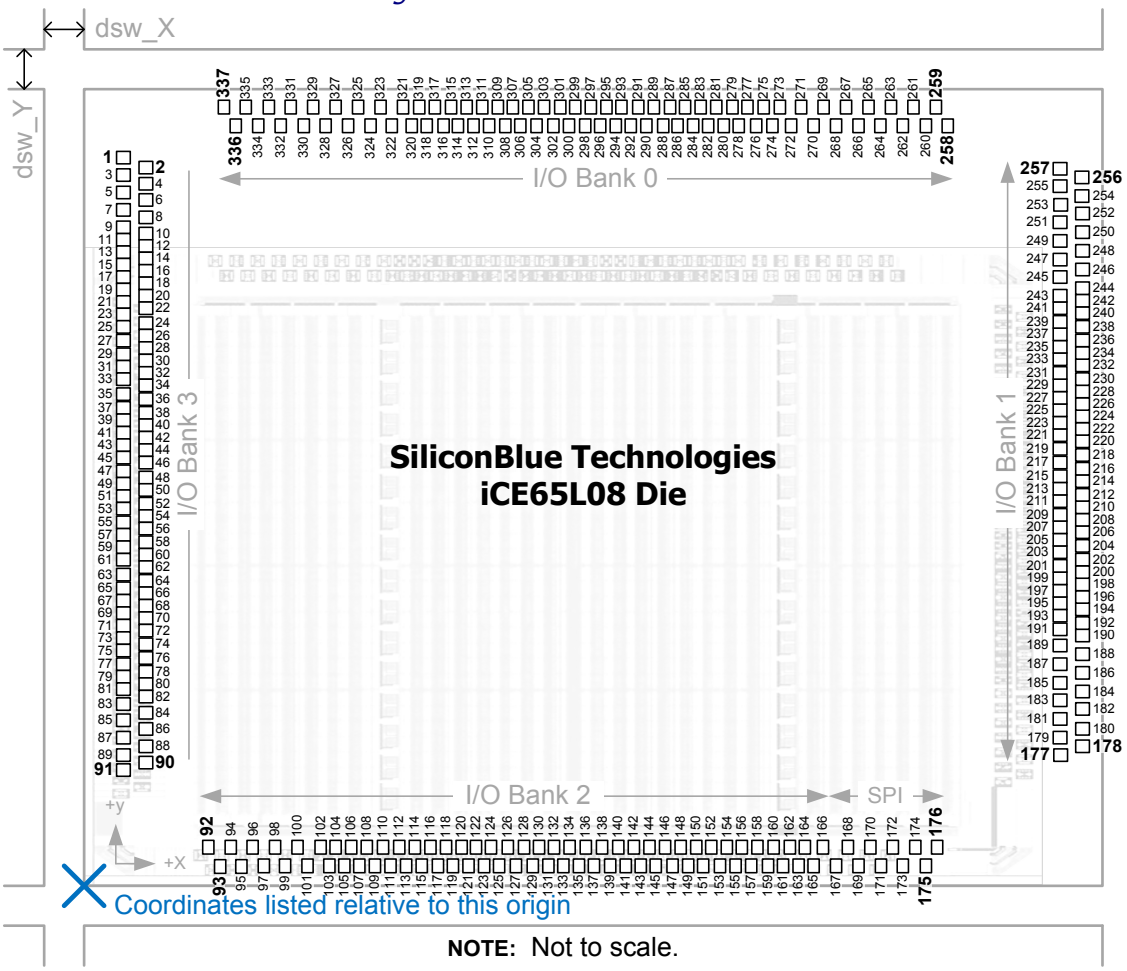
Physical Specifications

Figure 4 shows the physical outlines of iCE65L08 die on a wafer, including pad orientation and physical origin. The bond pad identification and coordinates are provided in Table 3. Table 2 lists key physical characteristics of each iCE65L08 die.

Table 2: **iCEL08 DiCE Physical Specifications**

Feature	Dimension
Wafer Diameter	300 mm (12 inches)
Wafer Thickness	6.0 to 31.0 mil, specified in ordering code, Figure 3.
Die Size (stepping interval)	4,810 µm x 4,394 µm
Scribe Width Along X-Axis (dsw_X)	160 µm
Scribe Width Along Y-Axis (dsw_Y)	160 µm
Bond Pad Size (min)	61 µm x 75 µm
Passivation Openings (min)	58 µm x 72 µm
Minimum Bond Pad Pitch (staggered)	35 µm

Figure 4: **iCE65L08 Die Outline**



NOTE: Not to scale.

Bond Pad Listing and Coordinates

Table 3 lists each of the 337 bonding pads on an iCE65L08 device. The pad number begins in the upper left corner of the die, as shown in Figure 4, and increments in a counter-clockwise direction around the perimeter of the die. Each bonding pad is identified. Signal names are color-coded by function. I/O pairs are grouped together with a thick surrounding box. These pairs in I/O Bank 3 represent an optional differential input or output. In all other banks, these pairs represent an optional differential output. The pad coordinates are measured relative to the origin, in the lower left corner of the die.

Table 3: **iCE65L08 Bond Pad Listing and Coordinates (Relative to Origin)**

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
1	PIO3_00/DP00A	129.735	3,882.665
2	PIO3_01/DP00B	231.735	3,837.665
3	PIO3_02/DP01A	129.735	3,792.665
4	PIO3_03/DP01B	231.735	3,747.665
5	GND	129.735	3,702.665
6	GND	231.735	3,657.665
7	VCCIO_3	129.735	3,612.665
8	VCCIO_3	231.735	3,567.665
9	PIO3_04/DP02A	129.735	3,512.665
10	PIO3_05/DP02B	231.735	3,477.665
11	PIO3_06/DP03A	129.735	3,442.665
12	PIO3_07/DP03B	231.735	3,407.665
13	VCC	129.735	3,372.665
14	VCC	231.735	3,337.665
15	PIO3_08/DP04A	129.735	3,302.665
16	PIO3_09/DP04B	231.735	3,267.665
17	PIO3_10/DP05A	129.735	3,232.665
18	PIO3_11/DP05B	231.735	3,197.665
19	GND	129.735	3,162.665
20	GND	231.735	3,127.665
21	PIO3_12/DP06A	129.735	3,092.665
22	PIO3_13/DP06B	231.735	3,057.665
23	GND	129.735	3,022.665
24	GND	231.735	2,987.665

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
25	PIO3_14/DP07A	129.735	2,952.665
26	PIO3_15/DP07B	231.735	2,917.665
27	VCCIO_3	129.735	2,882.665
28	VCCIO_3	231.735	2,847.665
29	VCC	129.735	2,812.665
30	VCC	231.735	2,777.665
31	PIO3_16/DP08A	129.735	2,742.665
32	PIO3_17/DP08B	231.735	2,707.665
33	VCCIO_3	129.735	2,672.665
34	VCCIO_3	231.735	2,637.665
35	GND	129.735	2,602.665
36	GND	231.735	2,567.665
37	PIO3_18/DP09A	129.735	2,532.665
38	PIO3_19/DP09B	231.735	2,497.665
39	PIO3_20/DP10A	129.735	2,462.665
40	PIO3_21/DP10B	231.735	2,427.665
41	PIO3_22/DP11A	129.735	2,392.665
42	PIO3_23/DP11B	231.735	2,357.665
43	VCCIO_3	129.735	2,322.665
44	VCCIO_3	231.735	2,287.665
45	VREF	129.735	2,252.665
46	VREF	231.735	2,217.665
47	GND	129.735	2,182.665
48	GND	231.735	2,147.665
49	VCCIO_3	129.735	2,112.665
50	VCCIO_3	231.735	2,077.665
51	GND	129.735	2,042.665
52	GND	231.735	2,007.665
53	PIO3_24/DP12A	129.735	1,972.665
54	GBIN7/ PIO3_25/DP12B	231.735	1,937.665
55	GND	129.735	1,902.665
56	GBIN6/ PIO3_26/DP13A	231.735	1,867.665
57	PIO3_27/DP13B	129.735	1,832.665
58	PIO3_28/DP14A	231.735	1,798.665
59	PIO3_29/DP14B	129.735	1,762.665
60	PIO3_30/DP15A	231.735	1,727.665
61	PIO3_31/DP15B	129.735	1,692.665
62	GND	231.735	1,657.665
63	GND	129.735	1,622.665
64	PIO3_32/DP16A	231.735	1,587.665
65	PIO3_33/DP16B	129.735	1,552.665
66	VCCIO_3	231.735	1,517.665
67	VCCIO_3	129.735	1,482.665
68	GND	231.735	1,447.665
69	GND	129.735	1,412.665

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
70	PIO3_34/DP17A	231.735	1,377.665
71	PIO3_35/DP17B	129.735	1,342.665
72	PIO3_36/DP18A	231.735	1,307.665
73	PIO3_37/DP18B	129.735	1,272.665
74	PIO3_38/DP19A	231.735	1,237.665
75	PIO3_39/DP19B	129.735	1,202.665
76	PIO3_40/DP20A	231.735	1,167.665
77	PIO3_41/DP20B	129.735	1,132.665
78	VCC	231.735	1,097.665
79	VCC	129.735	1,062.665
80	PIO3_42/DP21A	231.735	1,027.665
81	PIO3_43/DP21B	129.735	992.665
82	VCCIO_3	231.735	957.665
83	VCCIO_3	129.735	912.665
84	GND	231.735	867.665
85	GND	129.735	822.67
86	PIO3_44/DP22A	231.735	777.67
87	PIO3_45/DP22B	129.735	732.67
88	PIO3_46/DP23A	231.735	687.67
89	PIO3_47/DP23B	129.735	642.67
90	PIO3_48/DP24A	231.735	597.67
91	PIO3_49/DP24B	129.735	552.665
92	PIO2_00	510.0	139.5
93	PIO2_01	560.0	37.5
94	PIO2_02	610.0	139.5
95	GND	660.0	37.5
96	GND	710.0	139.5
97	PIO2_03	760.0	37.5
98	PIO2_04	810.0	139.5
99	PIO2_05	859.3	37.5
100	PIO2_06	910.0	139.5
101	PIO2_07	960.0	37.5
102	PIO2_08	1,012.5	139.5
103	VCCIO_2	1,047.5	37.5
104	VCCIO_2	1,082.5	139.5
105	PIO2_09	1,117.5	37.5
106	PIO2_10	1,152.5	139.5
107	GND	1,187.5	37.5
108	GND	1,222.5	139.5
109	PIO2_11	1,257.5	37.5
110	PIO2_12	1,292.5	139.5
111	PIO2_13	1,327.5	37.5
112	PIO2_14	1,362.5	139.5
113	PIO2_15	1,397.5	37.5
114	PIO2_16	1,432.5	139.5
115	PIO2_17	1,467.5	37.5

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
116	PIO2_18	1,502.3	139.5
117	GND	1,537.3	37.5
118	GND	1,572.5	139.5
119	PIO2_19	1,607.5	37.5
120	PIO2_20	1,642.5	139.5
121	VCC	1,677.5	37.5
122	VCC	1,712.5	139.5
123	PIO2_21	1,747.5	37.5
124	PIO2_22	1,782.5	139.5
125	PIO2_23	1,817.5	37.5
126	PIO2_24	1,852.5	139.5
127	PIO2_25	1,887.5	37.5
128	PIO2_26	1,922.5	139.5
129	PIO2_27	1,957.5	37.5
130	VCCIO_2	1,992.5	139.5
131	VCCIO_2	2,027.5	37.5
132	PIO2_28	2,062.5	139.5
133	GBIN5/PIO2_29	2,097.5	37.5
134	GBIN4/PIO2_30	2,132.5	139.5
135	GND	2,167.5	37.5
136	GND	2,202.5	139.5
137	PIO2_31	2,237.5	37.5
138	PIO2_32	2,272.5	139.5
139	PIO2_33	2,307.5	37.5
140	PIO2_34	2,342.5	139.5
141	PIO2_35	2,377.5	37.5
142	PIO2_36	2,412.5	139.5
143	PIO2_37	2,447.5	37.5
144	PIO2_38	2,482.5	139.5
145	PIO2_39	2,517.5	37.5
146	PIO2_40	2,552.5	139.5
147	PIO2_41	2,587.5	37.5
148	PIO2_42	2,622.5	139.5
149	PIO2_43	2,657.5	37.5
150	PIO2_44	2,692.5	139.5
151	VCC	2,727.5	37.5
152	VCC	2,762.5	139.5
153	PIO2_45	2,797.5	37.5
154	PIO2_46	2,832.5	139.5
155	VCCIO_2	2,867.5	37.5
156	VCCIO_2	2,902.5	139.5
157	PIO2_47	2,937.5	37.5
158	GND	2,972.5	139.5
159	GND	3,007.5	37.5
160	PIO2_48	3,042.5	139.5
161	PIO2_49	3,077.5	37.5
162	PIO2_50	3,112.5	139.5
163	PIO2_51/CBSEL0	3,147.5	37.5
164	PIO2_52/CBSEL1	3,182.5	139.5
165	CDONE	3,217.5	37.5
166	CRESET_B	3,260.0	139.5
167	PIOS_00/SPI_SO	3,320.0	37.5
168	PIOS_01/SPI_SI	3,370.0	139.5
169	GND	3,420.0	37.5
170	GND	3,470.0	139.5
171	PIOS_02/SPI_SCK	3,520.0	37.5
172	PIOS_03/SPI_SS_B	3,570.0	139.5
173	VCC	3,620.0	37.5
174	VCC	3,670.0	139.5
175	SPI_VCC	3,720.0	37.5
176	SPI_VCC	3,770.0	139.5
177	TDI	4,470.5	634.615
178	TMS	4,572.5	684.615
179	TCK	4,470.5	734.615
180	TDO	4,572.5	784.615
181	TRST_B	4,470.5	834.615
182	PIO1_00	4,572.5	884.615
183	PIO1_01	4,470.5	934.615
184	PIO1_02	4,572.5	984.615
185	PIO1_03	4,470.5	1,034.615
186	GND	4,572.5	1,084.615
187	GND	4,470.5	1,134.615
188	PIO1_04	4,572.5	1,184.615
189	PIO1_05	4,470.5	1,234.62
190	VCCIO_1	4,572.5	1,287.115
191	VCCIO_1	4,470.5	1,322.115
192	PIO1_06	4,572.5	1,357.115
193	PIO1_07	4,470.5	1,392.115
194	PIO1_08	4,572.5	1,427.115
195	PIO1_09	4,470.5	1,462.115
196	PIO1_10	4,572.5	1,497.115
197	VCC	4,470.5	1,532.115
198	VCC	4,572.5	1,567.115
199	PIO1_11	4,470.5	1,602.115
200	PIO1_12	4,572.5	1,637.115
201	PIO1_13	4,470.5	1,672.115
202	PIO1_14	4,572.5	1,707.115
203	PIO1_15	4,470.5	1,742.115
204	PIO1_16	4,572.5	1,777.115
205	PIO1_17	4,470.5	1,812.115
206	PIO1_18	4,572.5	1,847.115
207	GND	4,470.5	1,882.115
208	GND	4,572.5	1,917.110
209	PIO1_19	4,470.5	1,952.115

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
210	PIO1_20	4,572.5	1,987.115
211	PIO1_21	4,470.5	2,022.115
212	PIO1_22	4,572.5	2,057.115
213	VCCIO_1	4,470.5	2,092.115
214	VCCIO_1	4,572.5	2,127.115
215	PIO1_23	4,470.5	2,162.115
216	PIO1_24	4,572.5	2,197.115
217	PIO1_25	4,470.5	2,232.115
218	PIO1_26	4,572.5	2,267.115
219	GBIN3/PIO1_27	4,470.5	2,302.11
220	GBIN2/PIO1_28	4,572.5	2,337.115
221	PIO1_29	4,470.5	2,372.115
222	PIO1_30	4,572.5	2,407.115
223	PIO1_31	4,470.5	2,442.115
224	PIO1_32	4,572.5	2,477.115
225	PIO1_33	4,470.5	2,512.115
226	PIO1_34	4,572.5	2,547.115
227	PIO1_35	4,470.5	2,582.115
228	GND	4,572.5	2,617.115
229	GND	4,470.5	2,652.115
230	PIO1_36	4,572.5	2,687.12
231	VCCIO_1	4,470.5	2,722.12
232	VCCIO_1	4,572.5	2,757.12
233	PIO1_37	4,470.5	2,792.12
234	PIO1_38	4,572.5	2,827.12
235	PIO1_39	4,470.5	2,862.12
236	PIO1_40	4,572.5	2,897.12
237	PIO1_41	4,470.5	2,932.12
238	PIO1_42	4,572.5	2,967.12
239	PIO1_43	4,470.5	3,002.12
240	PIO1_44	4,572.5	3,037.12
241	PIO1_45	4,470.5	3,072.12
242	PIO1_46	4,572.5	3,107.12
243	VCC	4,470.5	3,142.12
244	VCC	4,572.5	3,177.12
245	PIO1_47	4,470.5	3,229.615
246	PIO1_48	4,572.5	3,279.615
247	VCCIO_1	4,470.5	3,329.615
248	VCCIO_1	4,572.5	3,379.615
249	PIO1_49	4,470.5	3,429.62
250	PIO1_50	4,572.5	3,479.615
251	GND	4,470.5	3,529.615
252	GND	4,572.5	3,579.615
253	PIO1_51	4,470.5	3,629.615
254	PIO1_52	4,572.5	3,679.595
255	PIO1_53	4,470.5	3,729.595
256	PIO1_54	4,572.5	3,779.595

Pad	Signal Name	From Origin	
		X (µm)	Y (µm)
257	VPP_2V5	4,470.5	3,879.575
258	VPP_FAST	3,866.975	4,054.5
259	VCC	3,766.98	4,156.5
260	VCC	3,716.98	4,054.5
261	PIO0_00	3,666.98	4,156.5
262	PIO0_01	3,616.98	4,054.5
263	PIO0_02	3,566.98	4,156.5
264	PIO0_03	3,516.98	4,054.5
265	PIO0_04	3,466.98	4,156.5
266	VCCIO_0	3,416.98	4,054.5
267	PIO0_05	3,366.98	4,156.5
268	PIO0_06	3,316.98	4,054.5
269	PIO0_07	3,266.98	4,156.5
270	GND	3,216.98	4,054.5
271	GND	3,166.98	4,156.5
272	PIO0_08	3,116.98	4,054.5
273	PIO0_09	3,064.48	4,156.5
274	PIO0_10	3,029.48	4,054.5
275	PIO0_11	2,994.48	4,156.5
276	PIO0_12	2,959.48	4,054.5
277	PIO0_13	2,924.48	4,156.5
278	PIO0_14	2,889.48	4,054.5
279	PIO0_15	2,854.48	4,156.5
280	VCCIO_0	2,819.48	4,054.5
281	VCCIO_0	2,784.48	4,156.5
282	PIO0_16	2,749.48	4,054.5
283	PIO0_17	2,714.48	4,156.5
284	PIO0_18	2,679.48	4,054.5
285	PIO0_19	2,644.48	4,156.5
286	PIO0_20	2,609.48	4,054.5
287	PIO0_21	2,574.48	4,156.5
288	PIO0_22	2,539.48	4,054.5
289	PIO0_23	2,504.48	4,156.5
290	PIO0_24	2,469.48	4,054.5
291	PIO0_25	2,434.48	4,156.5
292	GND	2,399.48	4,054.5
293	GND	2,364.48	4,156.5
294	PIO0_26	2,329.48	4,054.5
295	PIO0_27	2,294.48	4,156.5
296	PIO0_28	2,259.48	4,054.5
297	GBIN1/PIO0_29	2,224.48	4,156.5
298	GBIN0/PIO0_30	2,189.48	4,054.5
299	PIO0_31	2,154.48	4,156.5
300	VCCIO_0	2,119.48	4,054.5
301	VCCIO_0	2,084.48	4,156.5

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
302	PIO0_32	2,049.48	4,054.5
303	PIO0_33	2,014.48	4,156.5
304	PIO0_34	1,979.48	4,054.5
305	PIO0_35	1,944.48	4,156.5
306	VCC	1,909.48	4,054.5
307	VCC	1,874.48	4,156.5
308	PIO0_36	1,839.48	4,054.5
309	PIO0_37	1,804.48	4,156.5
310	PIO0_38	1,769.48	4,054.5
311	PIO0_39	1,734.48	4,156.5
312	GND	1,699.48	4,054.5
313	GND	1,664.48	4,156.5
314	PIO0_40	1,629.48	4,054.5
315	PIO0_41	1,594.48	4,156.5
316	PIO0_42	1,559.48	4,054.5
317	PIO0_43	1,524.48	4,156.5
318	PIO0_44	1,489.48	4,054.5
319	PIO0_45	1,454.48	4,156.5

Pad	Signal Name	From Origin X (µm)	From Origin Y (µm)
320	PIO0_46	1,419.48	4,054.5
321	PIO0_47	1,384.48	4,156.5
322	PIO0_48	1,331.98	4,054.5
323	VCCIO_0	1,281.98	4,156.5
324	VCCIO_0	1,231.98	4,054.5
325	PIO0_49	1,181.98	4,156.5
326	PIO0_50	1,131.98	4,054.5
327	PIO0_51	1,081.98	4,156.5
328	PIO0_52	1,031.98	4,054.5
329	PIO0_53	981.98	4,156.5
330	PIO0_54	931.98	4,054.5
331	GND	881.98	4,156.5
332	GND	831.98	4,054.5
333	PIO0_55	781.98	4,156.5
334	PIO0_56	731.98	4,054.5
335	PIO0_57	681.98	4,156.5
336	PIO0_58	631.98	4,054.5
337	PIO0_59	581.98	4,156.5

Die Testing Procedures

SiliconBlue Technologies die products are tested to ensure product functionality in our standard package. Each die has gone through wafer probe test of various functional and parametric conditions.

SiliconBlue Technologies retains a wafer map of each wafer as part of the probe records, along with a lot summary of wafer yields for each lot probed. SiliconBlue Technologies reserves the right to change the probe program at any time for continuous product improvement.

Die users may experience differences in performance relative to SiliconBlue Technologies' data sheets. This is due to differences in package capacitance, inductance, resistance, and trace length.

Product Reliability Monitors

Reliability of all packaged products is monitored by ongoing QRA reliability evaluations. From these evaluations, samples are subjected to a battery of tests known as "Accelerated Life and Environmental Stress Tests." During these tests, devices are stressed for many hours under conditions designed to simulate years of normal field use. A summary of these product family evaluations is published on a regular basis.

Storage Requirements

SiliconBlue Technologies' die products are packaged in a cleanroom environment for shipping. Upon receipt, transfer the die or wafers to a similar environment for storage. SiliconBlue Technologies recommends that the die or wafers be maintained in a filtered nitrogen atmosphere until removed for assembly. The moisture content of the storage facility should be maintained at 30% ±10% relative humidity. ESD damage precautions are necessary during handling. The die must be in an ESD-protected environment at all times for inspection and assembly.

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