Triscend E5 Hardware Development Platform User Manual

November 2001 Version 1.0

Contents

Introduction

The Triscend E5 Hardware Development Platform, shown in Figure 1, provides embedded system designer with a convenient environment to quickly create and evaluate applications for a Triscend E5 Configurable System-on-Chip (CSoC) device. The development platform contains a variety of I/O devices and interfaces for testing designs, all supported using the Triscend FastChip development system. This document provides information on how to use, connect, download, and debug applications on the board.

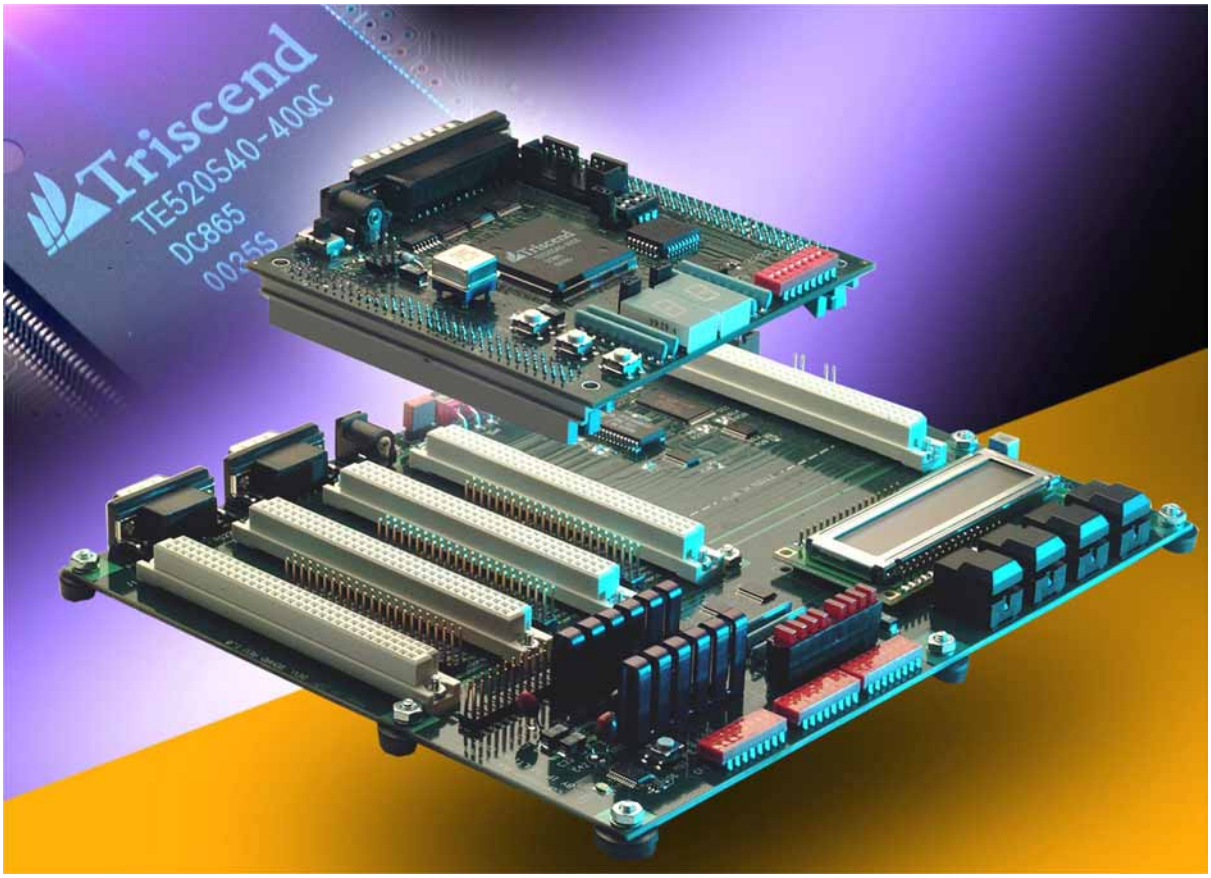


Figure 1. The Triscend E5 Development Platform consists of an E5 Evaluation Board that operates either stand-alone or when mounted on the Triscend Base Board, providing a richer set of capabilities.

The board provides a variety of connectors for attaching serial, parallel, JTAG, and power supply interfaces. Ample probe pins and expansion connectors provide nearly complete access to the pins of the CSoC device, either for a logic analyzer or for other prototype circuitry. Triscend TE520 CSoC applications are downloaded and debugged using a standard PC parallel port. Simply connect the included parallel port cable between your computer and the parallel port connector on the E5 Evaluation Board.

The complete **E5 Hardware Development Platform** consists of two separate pieces, as illustrated in Figure 1.

1. The **E5 Evaluation Board** functions as a stand-alone system for evaluating the Triscend E5 CSoC device. In conjunction with the FastChip Device Link (FDL) software and the included parallel printer cable for downloads, the board runs and tests code and CSL configurations. It includes its own power supply and Flash memory. For I/O, the evaluation board includes two seven-segment LED displays, an eight-position DIP-switch, and two pushbutton switches. All

of the E5's PIO pins are accessible from two 96-pin DIN connectors located along the left and right edges of the board.

2. For a more complete development environment, the E5 Evaluation Board plugs into the Triscend **Development Base Board** via the two 96-pin DIN connectors. The base board also includes its own Flash and SRAM memories, additional LEDs, and an LCD character display. The base board always requires that the evaluation board be installed. It does not function as a stand-alone system.

Triscend E5 Evaluation Board

Board Overview

Figure 2 shows the major functions on the Triscend E5 Evaluation Board. When connected to the included 5-volt regulated supply, the evaluation board functions as a stand-alone application complete with its own configuration Flash memory, pushbuttons, switches, and DIP switches.

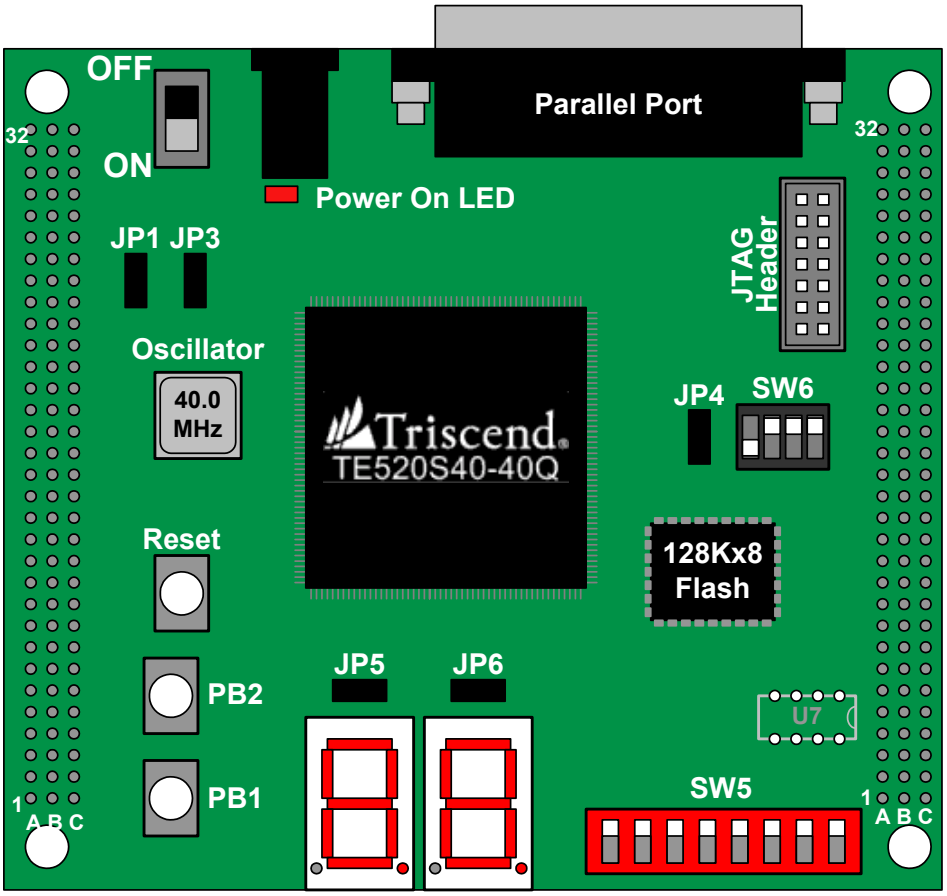


Figure 2. The Triscend E5 Evaluation Board.

Major Components

The Triscend E5 Evaluation Board kit contains the following functions.

- A Triscend TE520S40-40Q Configurable System-on-Chip (CSoC) device with 2,048 Configurable System Logic (CSL) cells and 40K-bytes of internal SRAM.
- An Am29LV001BB- 90JC 1M-bit (128Kx8) Flash memory device.
- A 40.000 MHz socketed oscillator.

- Two 7-segment LED displays.
- An 8-position DIP-switch (SW5).
- Two pushbutton switches (PB1, PB2).
- A pushbutton reset switch.
- A 25-pin 'D'-shell parallel port connector. Ideal for downloading and debugging applications via your PC parallel port.
- A regulated +5VDC, 2.5A wall mount power supply (not shown).
- A parallel printer cable (not shown).
- A Triscend FastChip Development System CD-ROM including a full license (not shown).
- A Keil Software Evaluation Tools CD-ROM that includes a limited 'C'-language compiler, debugger, simulator, and assembler for the E5's embedded, accelerated 8051 microcontroller (not shown).
- An OrCAD Capture Lite Edition CD-ROM including an evaluation version of the OrCAD schematic editor. The schematic libraries are included on the Triscend FastChip CD-ROM (not shown).

Connecting Power

Connect the evaluation board to +5VDC using the included regulated AC power adaptor. An on-board regulator generates the +3.3VDC supply required by the Triscend TE520 device.

When using the E5 Evaluation Board in stand-alone mode without the base board, ensure that jumpers JP1 and JP3 are installed.

When valid power is applied to the board, the Power-On LED indicator—located next to the power switch and below the adaptor connect—will light.

If this is the first time that the board is powered, the E5 boots from the on-board Flash and executes a simple application. The application increments a value displayed on the two 7-segment LEDs about once per second.

7-Segment LED Displays

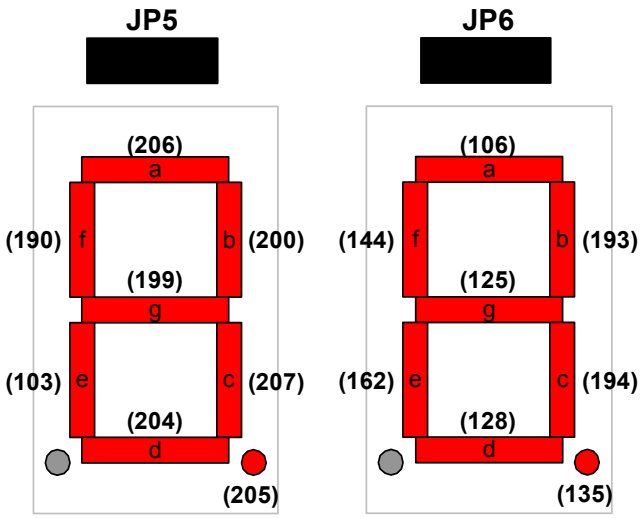
The E5 Evaluation Board has two common-cathode 7-segment LEDs, as shown in Figure 3. The displays are located along the bottom edge of the evaluation board, toward the center. Each display has a separate jumper connecting the display's common-cathode to VCC, optionally allowing each segment to be independently disconnected from the TE520 in order to reclaim PIO pins.

Lighting a Segment

Each segment on the LED displays is active-Low. In order to light a segment, the TE520 must drive the appropriate pin to a logic Low. The TE520 has sufficient drive capability to drive the LED segments directly.

Pin Connections from TE520

Figure 3 shows the pin connections to the two 7-segment LED displays. The number shown in parentheses is the TE520 pin that connects the respective segment. Though it may appear that there is a left decimal point on both displays, neither is connected. The decimal points on the right, however, do connect to TE520 pins.



(xxx) = TE520Q pin number.

Figure 3. Diagram of TE520 Pin Connections to 7-Segment Displays.

Table 1 presents the same connection information, but in tabular form.

Table 1. TE520 Pin Connections to 7-Segment Displays.

Segment	Left Display (TE520 PIO)	Right Display (TE520 PIO)
'a'	206	106
'b'	200	193
'c'	207	194
'd'	204	128
'e'	103	162
'f'	190	144
'g'	199	125
'dp'	205	135
Enable Jumper	JP5	JP6

When the evaluation board is installed on the base board, the left-most display shares connections with LCD character display. The LCD character display has its own enable switch on the base board. There is no signal contention between both functions because both are output devices. You may leave the JP5 jumper installed when using the LCD display. However, you may notice some flickering on the LED display when the application software writes to the LCD character display.

Similarly, the right-most display shares connections with the SW1 8-position DIP-switch on the base board. The SW1 switch has its own enable switch on the base board. There is possible contention if the evaluation board is installed on the base board, switch SW1 is enabled on the base board, one of the SW1 DIP switches is in the DOWN position (on), and the application is writing a '1' to the associated LED segment.

WARNING:	POTENTIAL CONTENTION IF INSTALLED ON BASE BOARD
!	If the evaluation board is installed on base board, and the base board switch SW2.2 is in the DOWN (on) position, then do not drive a PIO connected to the right-most 7-segment display High while the connected switch from switch block SW1 it is the DOWN (on) position! This condition causes contention as the TE520 attempts to drive a logic High while PIO is connected to ground through the switch. This condition will cause excessive power consumption and may damage the TE520 after a long period of time.

Reclaiming PIO Pins

The connections to the two 7-segment displays consume up to 16 PIO pins. Some applications may wish to use these pins for other functions. To reclaim the PIOs connected to a specific 7-segment display, remove its associated jumper. Removing the jumper disconnects the common cathode from VCC.

The jumper for each display is located immediately above the display, as shown in Figure 3. Jumper JP5 controls the left display while JP6 controls the right display, as shown in Table 2.

Table 2. Jumpers JP5 and JP6 Control 7-Segment Displays.

Jumper	JP5 (Left Display)	JP6 (Right Display)
Removed	Disabled (PIOs available to user application)	Disabled (PIOs available to user application)
Installed	Enabled (PIOs connected to 7-segment LED)	Enabled (PIOs connected to 7-segment LED)

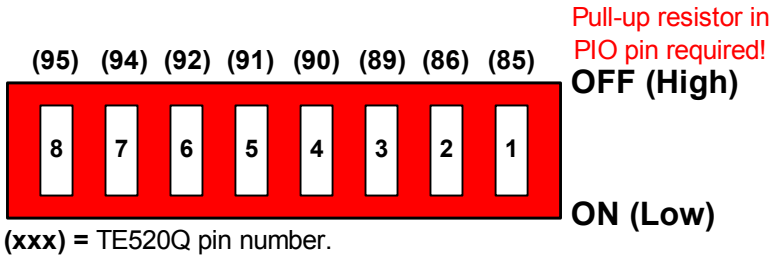
8-Position DIP Switch (SW5)

The Triscend E5 Evaluation Board has an eight-position DIP-switch block located in the lower right corner of the board, labeled SW5.

Pin Connections from TE520

Figure 4 and Table 3 show the pin connections between the TE520 CSoC device and the evaluation board's 8-position DIP-switch.

When an individual switch is switched DOWN (on), the associated TE520 PIO pin connects directly to ground (GND). If the individual switch is switched UP (off), the TE520 PIO pin is completely disconnected, *i.e.* floating.



(xxx) = TE520Q pin number.

Figure 4. Diagram of PIO Connections to the 8-position DIP Switch (SW5).

Consequently, the optional pull-up resistor inside the associated TE520 pin must be used so that the switch indicates a logic High. Switching from Low to High will not be instantaneous as the E5's pull-up resistor has a relatively high resistor value, ranging between 50kΩ and 150kΩ.

The 8-position DIP-switches are not debounced but can be using resources inside the CSoC device.

When the evaluation board is installed on the base board, the evaluation board's SW5 switches are wired in parallel with the base board's SW3 switches, if switch SW2.3 is DOWN (on).

Table 3. PIO Connections to the 8-position DIP Switch (SW5).

Switch Position	TE520 PIO
SW5.1	85
SW5.2	86
SW5.3	89
SW5.4	90
SW5.5	91
SW5.6	92
SW5.7	94
SW5.8	95

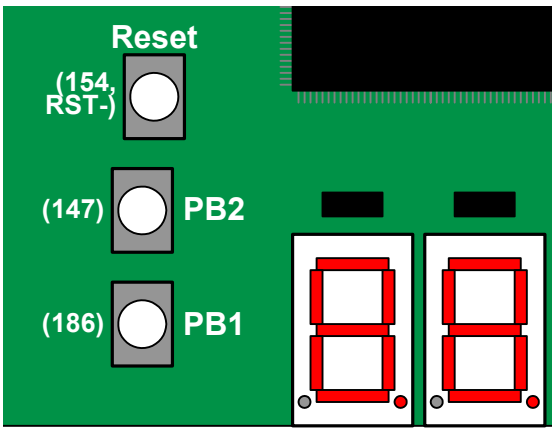
Reclaiming PIO Pins

To reclaim any of the eight PIO pins that connect to the 8-position DIP switch, simply switch the indicated switch position to OFF. While OFF, the PIO is completely disconnected, *i.e.* floating.

WARNING: !	Do not drive a PIO High into a switch while it is the ON position! This condition causes contention as the TE520 attempts to drive a logic High while PIO is connected to ground through the switch. This condition will cause excessive power consumption and may damage the TE520 after a long period of time.

Pushbutton Switches (PB1, PB2)

The E5 Evaluation Board has two normally open, momentary contact pushbutton switches, located to the left of the 7-segment LED displays, as shown in Figure 5.



(xxx) = TE520Q pin number.
Pull-up resistor in TE520 PIO pin required!

Figure 5. Pushbutton Switches.

These switches are normally open. When one of these switches in pressed, the associated TE520 PIO pin is connected to ground (GND). When the switch is released, the connection is again open, *i.e.* floating.

Consequently, the optional pull-up resistor inside the associated TE520 pin must be used so that the switch indicates a logic High Switching from Low to High will not be instantaneous as the E5's pull-up resistor has a relatively high resistor value, ranging between 50kΩ and 150kΩ.

The pushbutton switches are not debounced but can be using resources inside the CSoC device.

Table 4 shows the pushbutton connections to the TE520, including the reset button.

Table 4. Evaluation Board Pushbutton Switches.

Pushbutton	TE520 PIO
PB1	186
PB2	147
Reset	154, RST-

When the evaluation board is installed on the base board, and switch SW2.8 is in the DOWN (on) position, the pushbutton PB1 is wired in parallel with pushbutton SW6 on the base board and pushbutton PB2 is wired in parallel with pushbutton SW7 on the base board. There are no potential contention issues unless one of the pushbuttons is held Low for long periods of time while the associated PIO pin drives High.

Reset Pushbutton (SW2)

When pressed, the Reset pushbutton switch directly resets the TE520 device using the RST- input, pin 154. Holding down the button holds the TE520 in reset. When released, the TE520 begins its boot sequence.

Table 4 shows the pushbutton connections to the TE520, including the reset button.

The Reset button on the evaluation board is wired in parallel with the RST button on the base board.

If the evaluation board's Flash is enabled — jumper JP4 is installed — then the TE520 loads the configuration from Flash, regardless of the previously downloaded configuration. If Flash is disabled or holds invalid configuration data, the E5 attempts to boot itself and then automatically enters power-down mode because the TE520 VSYS pin is pulled to VCC.

Connection Options Settings Switch (SW6)

Figure 6 shows the connection options provided on the E5 Evaluation Board via the SW6 4-position DIP-switch block. Isolation buffers connect or disconnect the TE520 from the parallel port or serial port or connect the TE520's JTAG download/debug port to the parallel port.

The RS-232 drivers on the evaluation board do not attached to any serial connectors, though are available on the auxiliary bus pins.

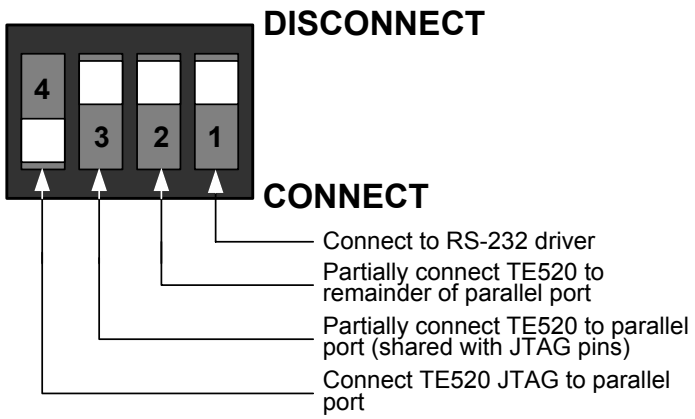


Figure 6. Diagram of the Default Option Switch Settings, SW6.

Table 5 shows how each individual switch controls the configuration of the board. The default switch settings are highlighted in capital letters.

Table 5. Connection Options to Parallel Port, Serial Port. (default switch positions highlighted)

Switch	Switch Position	Function
SW6.1 (RS-232)	**UP**	Disconnects TE520 PIO pins associated with RS-232 driver, reclaims PIO pins
	Down	Connects TE520 PIO pins to the RS-232 driver (U10).
SW6.2 (Remainder Parallel Port)	**UP**	Disconnects TE520 PIO pins associated with part of parallel port, reclaims PIO pins
	Down	Partially connects TE520 PIO pins to the remainder of the parallel port. Additional control provided by SW6.3. See Figure 7.
SW6.3 (Partial Parallel Port)	**UP**	Disconnects TE520 PIO pins associated with part of parallel port, reclaims PIO pins
	Down	Connects TE520 PIO pins, not TE520 JTAG pins, to parallel port signal Data[3:0], Busy. See Figure 7.
SW6.4 (JTAG via Parallel Port)	Up	Disconnects parallel port from TE520 JTAG pins, allows error-free use of 14-pin JTAG header
	DOWN	Connects part of parallel port to the TE520 JTAG pins, not general-purpose PIO pins. See Figure 7.

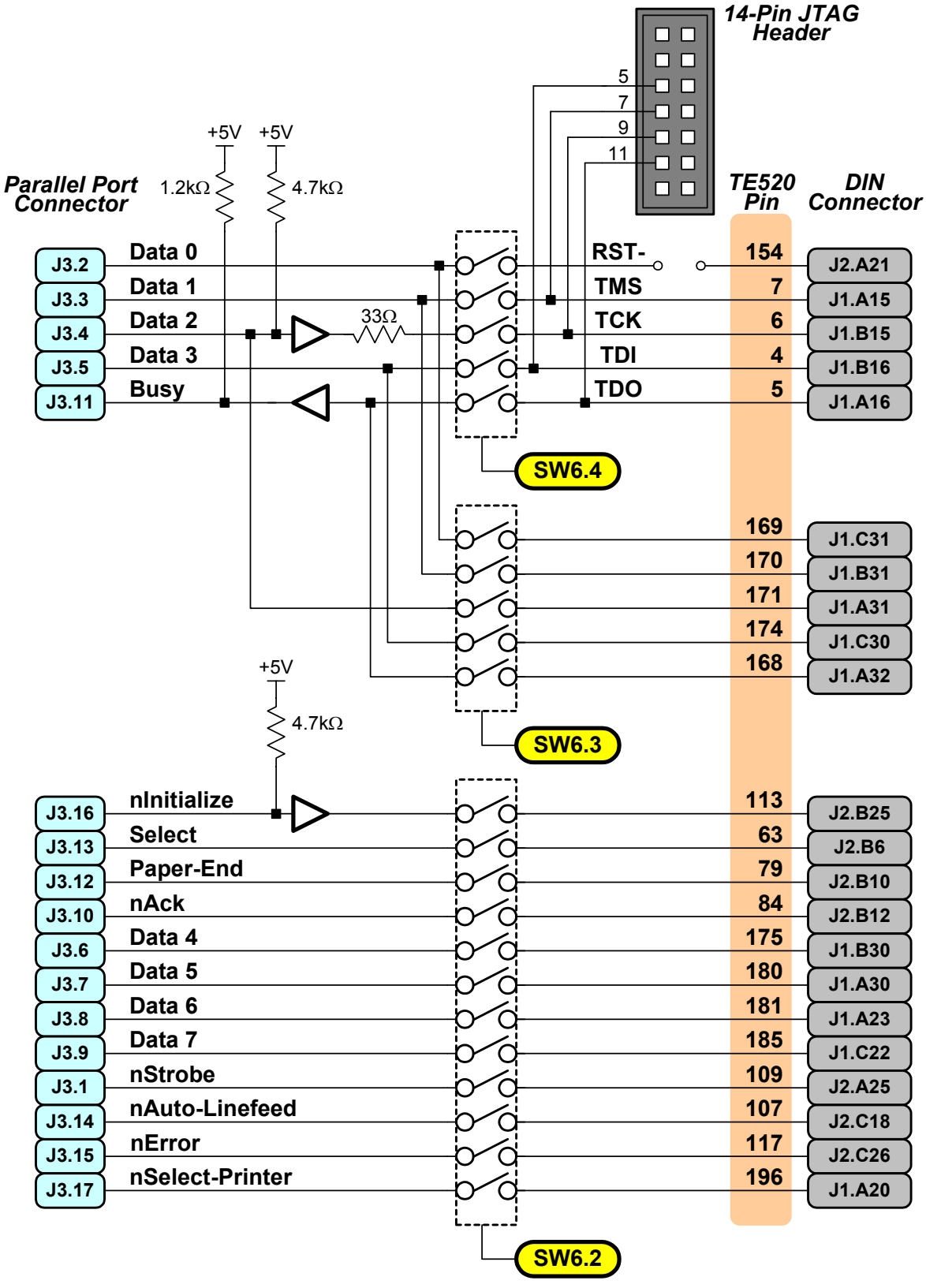


Figure 7. Isolation Switches Connect/Disconnect the TE520 to/from the Parallel Port and JTAG.

Parallel Port

The evaluation board has a 25-pin 'D'-shell male parallel printer port connector. The primary purpose of this connector is for downloading and debugging applications on the TE520 device. However, the parallel port can also be used by the application as an I/O device.

Connection Options

Three switches in switch block SW6 control the TE520 connections to the parallel port, as shown in Table 6. Figure 7 illustrates how the various option switches connect the parallel port signals to the TE520.

Table 6. Parallel Port Options Controlled by Switch Block SW6.

Function	SW6.4	SW6.3	SW6.2
Download/debug TE520 using standard parallel port cable	**DOWN**	**UP**	Don't Care
Download/debug TE520 using JTAG emulator connected to 14-pin JTAG header	Up	Up	Don't Care
Connect TE520 to parallel port so that it can send/receive data	Up	Down	Down
Reclaim all TE520 PIO pins associated with parallel port	Up	Up	Up

Pin Connections

Figure 8 and Table 7 show the connections between the 25-pin parallel port connector and the TE520 device. The specific connectivity also depends on the SW6 switch settings.

In a typical PC application, an IBM-compatible printer port is controlled via three consecutive I/O ports in the processor's I/O space, as shown in Figure 8.

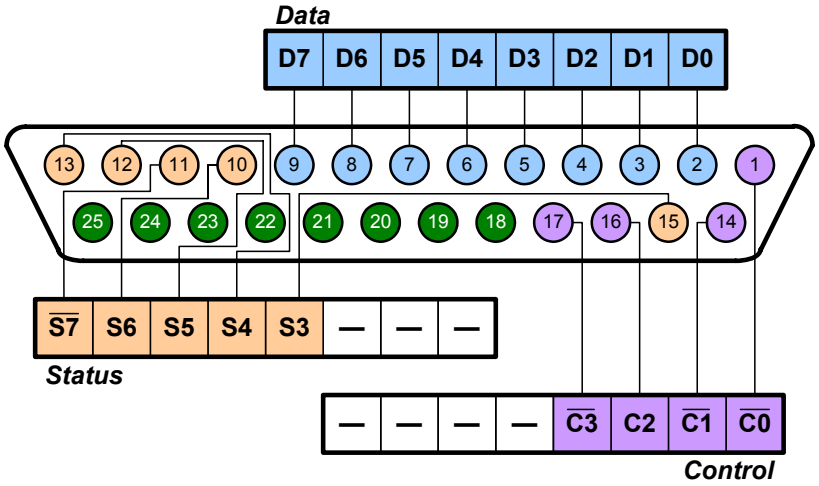


Figure 8. The Signals on a Standard PC Parallel Port Connector are Generally Controlled by Three Byte-Wide I/O Registers (viewed looking into socket from top edge of board)**.**

Table 7. TE520 Connections to the Parallel Port , Depending on SW6 Settings.

DB-25 Pin	Signal Name	Direction from PC	PC Register Bit	JTAG Download SW6.4=DOWN SW6.3=UP	Parallel Port SW6.4=UP SW6.3=DOWN SW6.2=DOWN
1	nStrobe	In/Out	C0	—	109
2	Data 0	Out	D0	RST-, 154	169
3	Data 1	Out	D1	TMS, 7	170
4	Data 2	Out	D2	TCK, 6	171
5	Data 3	Out	D3	TDI, 4	174
6	Data 4	Out	D4	—	175
7	Data 5	Out	D5	—	180
8	Data 6	Out	D6	—	181
9	Data 7	Out	D7	—	185
10	nAck	In	S6	—	84
11	Busy	In	S7	TDO, 5	168
12	Paper-Out/ Paper-End	In	S5	—	79
13	Select	In	S4	—	63
14	nAuto-Linefeed	In/Out	C1	—	107
15	nError/ nFault	In	S3	—	117
16	nInitialize	In/Out	C2	—	113
17	nSelect-Printer/ nSelect-In	In/Out	C3	—	196
18-25	Ground	Ground		—	—

Downloading Application and Using Parallel Port in Application

It is possible to download an application to the TE520 via the parallel port and then use the parallel port as part of the application by modifying the SW6 configuration switches after downloading. However, you will not be able to debug the application via the parallel port in the case.

RS-232 Driver

The E5 Evaluation Board has an RS-232 driver (component U10), located above the red 8-position DIP-switch. The board does not have its own serial connectors. The driver optionally connects to TE520 PIO pins, controlled by switch SW6.1 as shown in Figure 9.

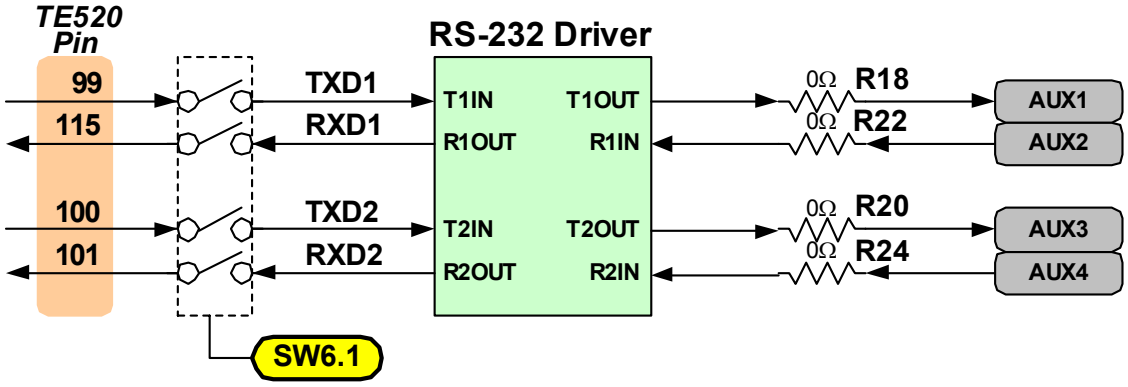


Figure 9. The TE520 Optionally Connects to an On-board RS-232 Driver.

Pin Connections

Table 8 shows the TE520 PIO connection to the evaluation board's RS-232 driver. The associated physical interface connections attach to the auxiliary bus signal AUX1 through AUX4. When the evaluation board is installed on the base board, these auxiliary signals are available on the Auxiliary Connector.

Table 8. Optional RS-232 Connections, Controlled by SW6.1.

RS-232 Signal	TE520 PIO	AUX Bus
Transmit Data 1 (TXD1)	99	AUX1
Receive Data 1 (RXD1)	115	AUX2
Transmit Data 2 (TXD2)	100	AUX3
Receive Data 2 (RXD2)	101	AUX4

Connecting TE520 to RS-232 Driver

The TE520 optionally connects to the RS-232 driver via isolation switches. To connect the TE520, switch SW6.1 to the DOWN position. See Table 5 for more information.

Reclaiming PIO Pins

If not using the RS-232 driver, switch SW6.1 to the UP position. This allows the four PIO pins associated with the RS-232 to be used as PIO pins in the application.

Disconnecting Driver from Bus Connector

The RS-232 driver itself connects to the auxiliary bus signals that connect to the J2 96-pin DIN connector. To disconnect an individual signal from the DIN connector, remove the associated surface-mount 0Ω resistor from the backside of the board. The resistor reference designators are shown in Figure 9.

When the E5 Evaluation Board is plugged into the base board, these RS-232 connections appear on the 26-pin auxiliary connector.

128Kx8 Flash

The E5 Evaluation Board has its own 128Kx8 (1M-bit) boot Flash memory, as shown in Figure 10, that optionally holds the configuration and application code for the TE520 device.

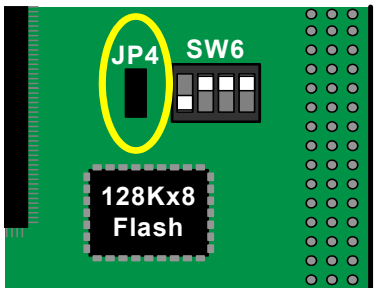


Figure 10. Jumper JP4 on the Evaluation Board Connects the TE520 to Flash Memory.

Jumper JP4 connects the TE520's CE- output pin to chip-enable input on the Flash memory. This jumper must be removed when the evaluation board is installed on the base board.

FastChip Device Link (FDL) can download directly to the TE520's internal SRAM, even if Flash is enabled.

Downloading to the E5 Evaluation Board

The E5 Evaluation Board can be configured and debugged using a standard parallel printer cable connected to your computer's parallel printer port. For future expansion, the evaluation board also has a separate 14-pin JTAG header, JP7.

Using the Parallel Port

To download and debug a design on the E5 Evaluation Board using the parallel port, please follow these steps, as shown in Figure 11.

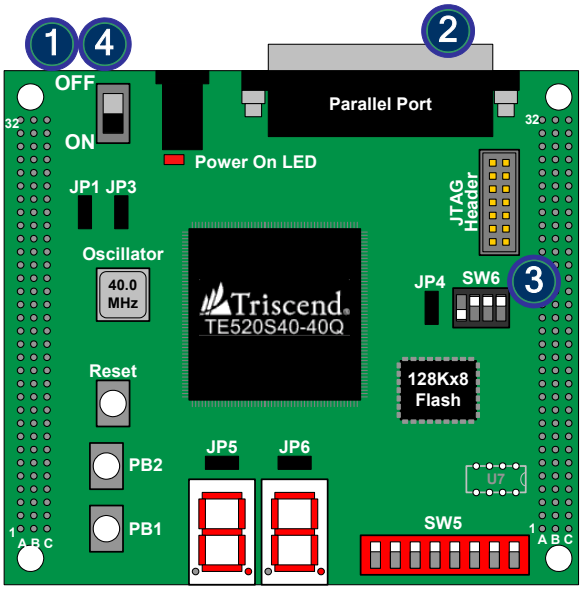
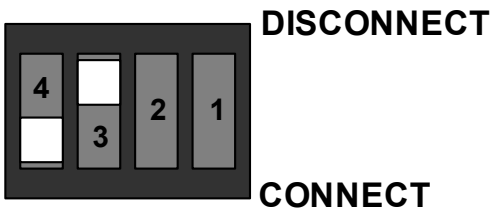


Figure 11. Preparing to Download to the E5 Evaluation Board.

1 Switch the evaluation board's power switch to the OFF position.

2 Connect a standard 25-pin PC parallel port cable to your computer's parallel port. Connect the other end of the cable to E5 Evaluation Board using the parallel port connector.

3 Enable the parallel port connections to the TE520 JTAG pins by switching SW6.4 to the DOWN position. Disconnect other TE520 PIO ports from the same parallel port signals by switching SW6.3 to the UP position. The positions of switches SW6.2 and SW6.1 do not matter.



4 Switch the evaluation board's power switch to the ON position. If there was a previous application stored in Flash, the board will boot from Flash. However, the JTAG interface is able to overwrite any currently-loaded application.

Using the 14-Pin JTAG Header

The 14-pin JTAG header, JP7, provides future expansion capabilities for the E5 Evaluation Board. It is not currently supported.

This 14-pin header does not support the E5 JTAG download/debug cable, also called the Wiggler cable.

FastChip Device Link (FDL) Configuration Settings

The FastChip Device Link (FDL) utility creates a configuration image for your application that you then download to the E5 Evaluation Board. The following configuration options are available, shown in Figure 12.

1 Select Target Memory Type

Choose the target memory where FDL will download the configuration image. When the E5 Evaluation Board operates stand-alone, the available options are as listed below.

- CSoC internal RAM
- Flash Memory

2 Select Memory Part Number

If downloading to "CSoC internal RAM", no memory part number is required. If downloading to Flash, select the Flash part number from your E5 Evaluation Board. The specific part number may vary, depending on when your board was manufactured.

At introduction, the E5 Evaluation Board includes an AMD 1M-bit Flash with 90 ns access time, or **AM29LV001B-90** from the part drop list.

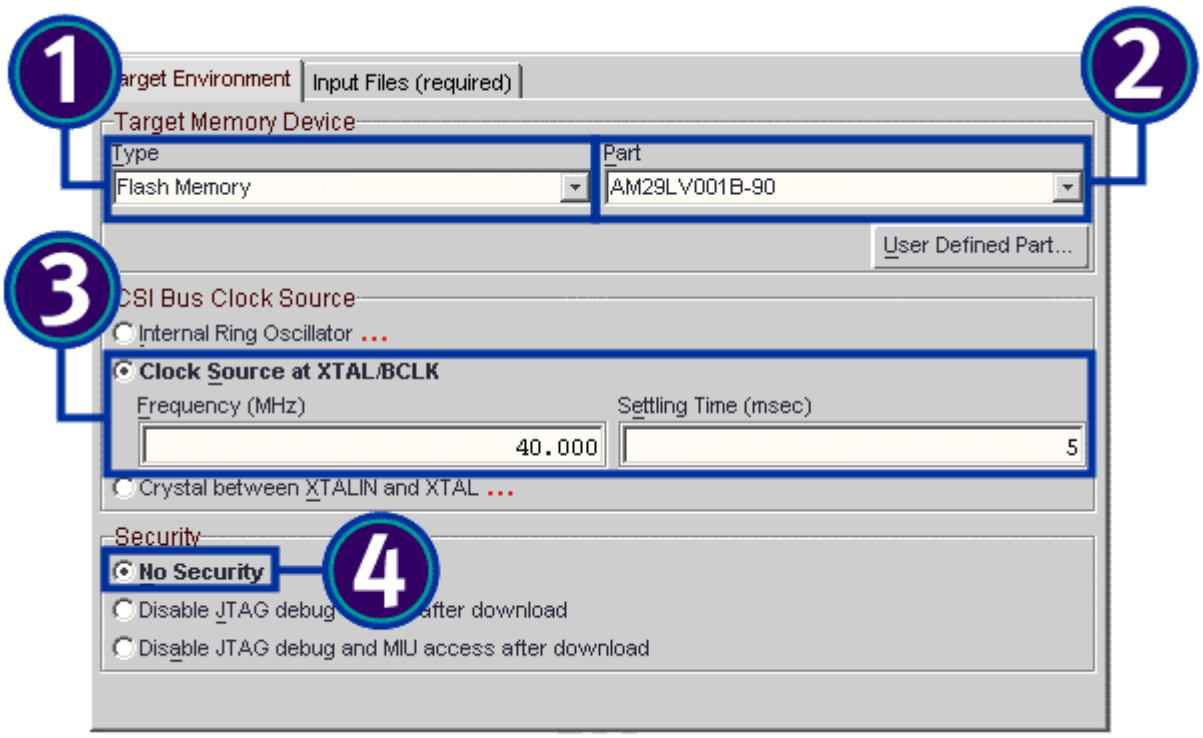


Figure 12. Typical FastChip Device Link (FDL) Settings for Downloading to the E5 Evaluation Board's Flash Memory.

3 Choose the CSI Bus Clock Source

There are two potential CSI bus clock sources available on the E5 Evaluation Board. The internal ring oscillator is available within each E5 CSoC device. Its frequency ranges between 5 MHz and 20 MHz.

Typically, however, most applications will use the external crystal clock oscillator provided on the board as it supplies a known, constant frequency.

At introduction, the E5 Evaluation Board includes a **40.000** MHz clock oscillator. Allow **5** ms for the oscillator to settle after power-on.

4 Disable Security Options for Easier Debugging

By default, always choose the **No Security** option when downloading, especially to Flash. If any of the security options are set, you will not be able to debug your application.

Triscend Development Base Board

Board Overview

Figure 13 shows the major features of the Triscend Development Base Board. When partnered with the E5 Evaluation Board, the base board provides extended capabilities, including additional switches, LEDs, a LCD character display, and three expansion slots for prototype cards.

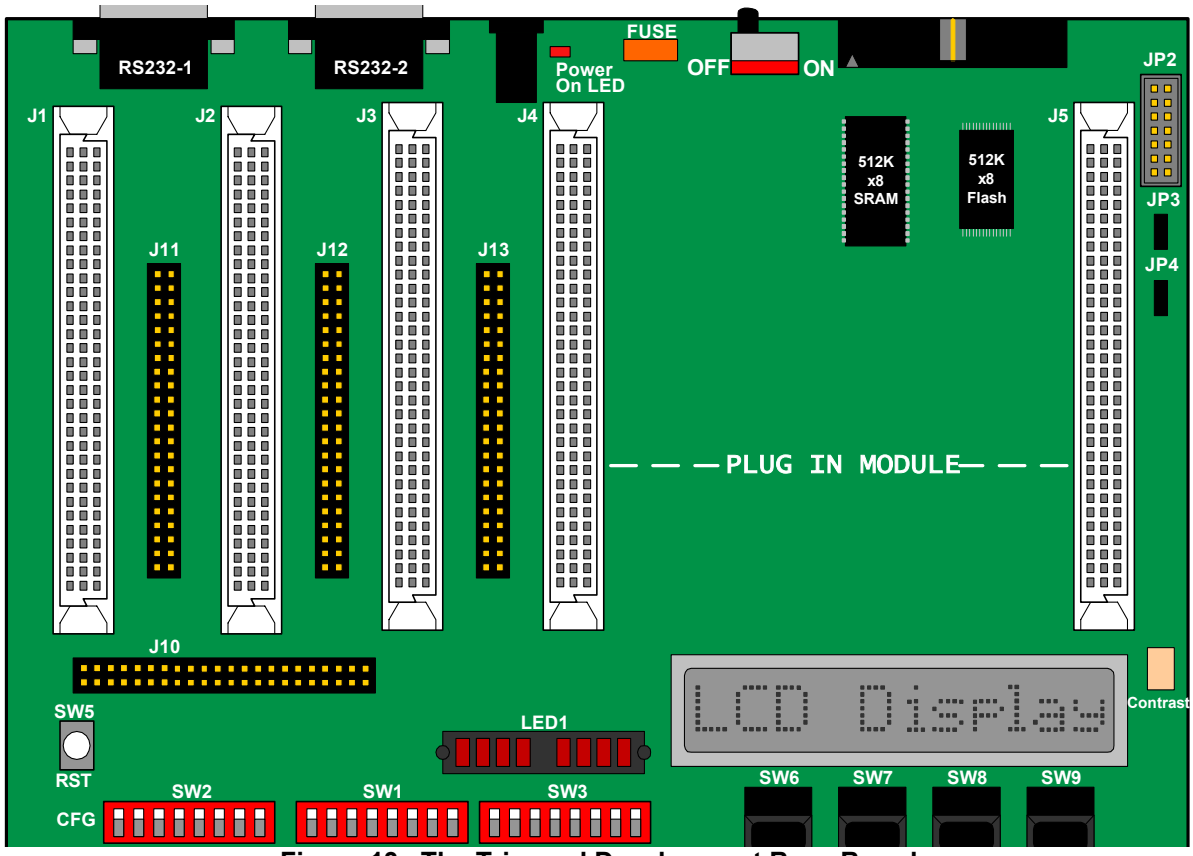


Figure 13. The Triscend Development Base Board.

Major Components

- Two 96-pin DIN connections to the E5 Evaluation Board
- Two RS232 drivers including connectors
- LCD character display (2x16) with contrast potentiometer
- Two user 8-position DIP-switches (SW1, SW3) with pull-up resistors
- Eight-LED bar display with current limiting resistors (LED1)
- Four pushbutton switches (SW6, SW7, SW8, SW9) with pull up resistors
- 4-Mbit (512Kx8) 90ns Flash memory
- 4-Mbit (512Kx8) 20ns SRAM memory with switches to configure as download memory or as stand-alone application RAM
- 5V to 3.3V regulator, rated at 2.5A over 0-40° C with heat sink
- 5VDC power input jack with reversal protection diode, over voltage protection diode, fuse, on-off slide switch and power indicator

- Reset voltage-monitor circuit with reset button and LED
- Configuration DIP switch (SW2) to connect or disconnect the LCD display, DIP switches, LEDs, pushbutton switches, RS-232 driver, and Flash and SRAM memories from PIO pins
- AUX 26-pin connector (digital and analog power pins, AUX1-AUX16 pins, Reset/Manual Reset signals)
- 14-pin JTAG connector
- Prototyping expansion board
- Three 96-pin expansion slots
- A replacement fuse

Board Option Switch Settings (SW2)

The base board supports a variety of options, all controlled via the SW2 8-position DIP-switch. Figure 14 graphically shows the options provided by the SW2 switch, while Table 9 describes the switch settings in more detail.

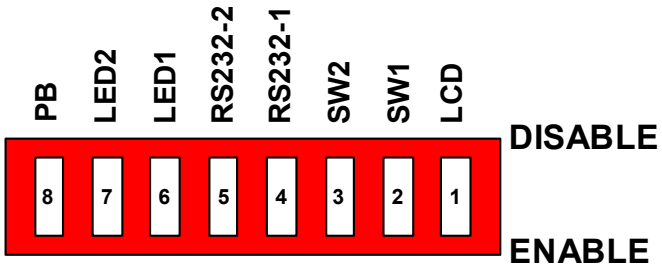


Figure 14. Baseboard Switch SW2 Configures Various Board Options.

Table 9. Base Board Configuration Options.

Switch	Switch Position	Function
SW2.1 (LCD)	Up	Disconnects TE520 PIO pins from the LCD character display.
	Down	Connects TE520 pins to the LCD character display. The connections are in parallel with the left-most 7-segment LED display. Remove jumper JP6 on the evaluation board.
SW2.2 (Switch SW1)	Up	Disconnects TE520 PIO pins from the 8-position DIP-switch SW1 on the baseboard.
	Down	Connects TE520 pins to the 8-position DIP-switch SW1 on the baseboard. The connections are in parallel with DIP-switch SW5 on the evaluation board. All SW5 DIP-switches should be OFF, the up position.
SW2.3 (Switch SW3)	Up	Disconnects TE520 PIO pins from the 8-position DIP-switch SW3 on the baseboard.
	Down	Connects TE520 pins to the 8-position DIP-switch SW3 on the baseboard. The connections are in parallel with the right-most 7-segment LED display. Remove jumper JP5 on the evaluation board. Switches SW3.7 and SW3.8 may also be shared with pushbutton switches SW8 and SW9.
SW2.4 (RS232-1)	Up	Disconnects TE520 PIO pins from RS-232 port P1.
	Down	Connects TE520 pins to RS-232 port P1 on the baseboard. The connections may be in parallel with the nError and Select signals from the parallel port if SW6.2 is in the DOWN position. SW6.2 should be in the UP position.
SW2.5 (RS232-2)	Up	Disconnects TE520 PIO pins from RS-232 port P2.
	Down	Connects TE520 pins to RS-232 port P2 on the baseboard. The connections may be in parallel with the nAck and Paper-Out/Paper-End signals from the parallel port if SW6.2 is in the DOWN position. SW6.2 should be in the UP position.
SW2.6 (Right side LED1)	Up	Disconnects TE520 PIO pins from right side of LED bar, LED1.
	Down	Connects TE520 pins to right four LEDs on LED bar, LED1. The connections may be in parallel with the Data[7:4] signals from the parallel port if SW6.2 is in the DOWN position. SW6.2 should be in the UP position.
SW2.7 (Left side LED1)	Up	Disconnects TE520 PIO pins from left side of LED bar, LED1.
	Down	Connects TE520 pins to left four LEDs on LED bar, LED1. The connections may be in parallel with the nStrobe, nAuto-Linefeed, nInitialize, and nSelect-Printer signals from the parallel port if SW6.2 is in the DOWN position. SW6.2 should be in the UP position.

Switch	Switch Position	Function
SW2.8 (PB)	Up	Disconnects TE520 PIO pins from the four large pushbutton switches on the baseboard, SW6, SW7, SW8, and SW9.
	Down	Connects TE520 pins to the four large pushbutton switches on the baseboard, SW6, SW7, SW8, and SW9. SW6 on the baseboard is in parallel with PB2 on the evaluation board. SW7 on the baseboard is in parallel with PB1 on the evaluation board. Pushbutton SW8 on the baseboard is in parallel with segment 'g' on the right-most 7-segment LED display on the evaluation board. SW9 on the baseboard is in parallel with the decimal point segment on the right-most 7-segment LED display on the evaluation board. Remove jumper JP6 on the evaluation board.

LCD Character Display

The base board includes a 2x16 character LCD display, located in the lower right-hand corner as shown in Figure 15. The LCD data inputs are shared with the left-most 7-segment LED display on the evaluation board.

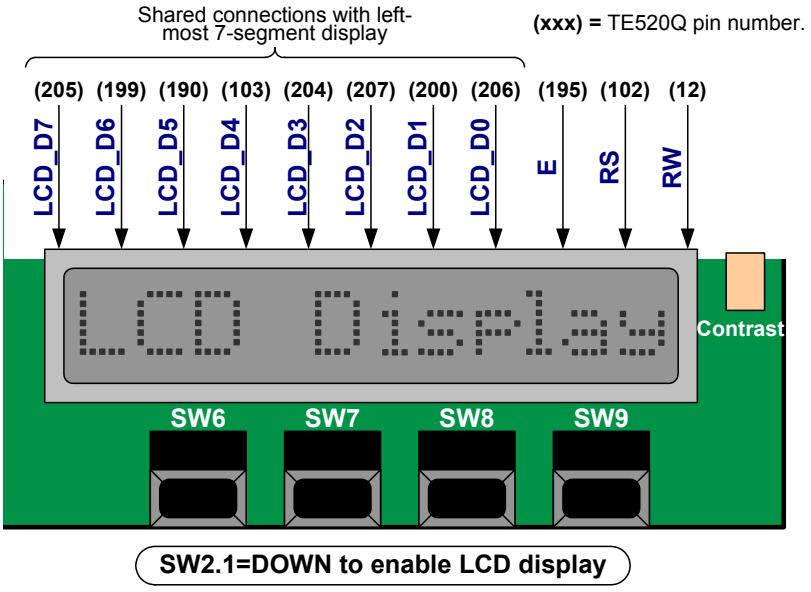


Figure 15. Character LCD Display.

To use the 2x16 character LCD display in an application, follow these steps.

- SW2.1 must be in the DOWN position to connect the TE520 to the LCD display.
- Ideally, remove jumper JP6 on the evaluation board, which controls the left-most 7-segment display. This step is not required but writing to the LCD display may cause strange flickering on the left-most 7-segment display.

Pin Connections

Table 10 shows the TE520 PIO connections to the LCD display. Some of the LCD connections are also shared with the left-most 7-segment display on the evaluation board if jumper JP6 is installed.

Table 10. Character LCD Display Pin Connections.

LCD Signal	TE520 PIO	Left-Most LED Segment
LCD_D0	206	'a'
LCD_D1	200	'b'
LCD_D2	207	'c'
LCD_D3	204	'd'
LCD_D4	103	'e'
LCD_D5	190	'f'
LCD_D6	199	'g'
LCD_D7	205	Decimal point
E	195	—
RS	102	—
RW	12	—

Supporting IP Modules

The FastChip "**LCD Char Driver**" module easily connects your application to the base board's LCD character display. To locate this module, simply type "**LCD**" in the Find text box, as shown in Figure 16.

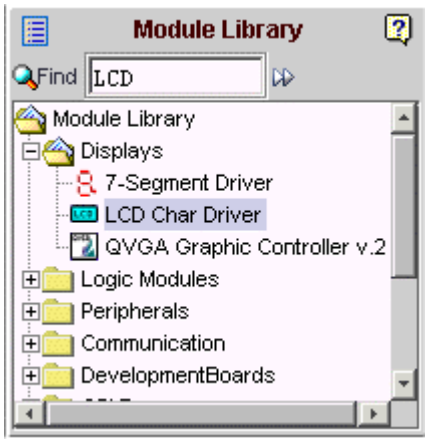


Figure 16. Find the "LCD Char Driver" by Typing "LCD".

The LCD character display driver has few options, as shown in Figure 17. All the connections to I/O pins are embedded within the module. It is possible to change the symbolic names for the two LCD registers, though Triscend recommends leaving them set to the default value, shown in Table 11, to be compatible with the various sample applications provided.

Table 11. LCD Character Display Symbolic Addresses.

Symbolic Address	Function
LCD_CTR	LCD Command Register
LCD_DATA	LCD Data Register

For additional information on the module, click the **Help** button at the bottom of the dialog box.

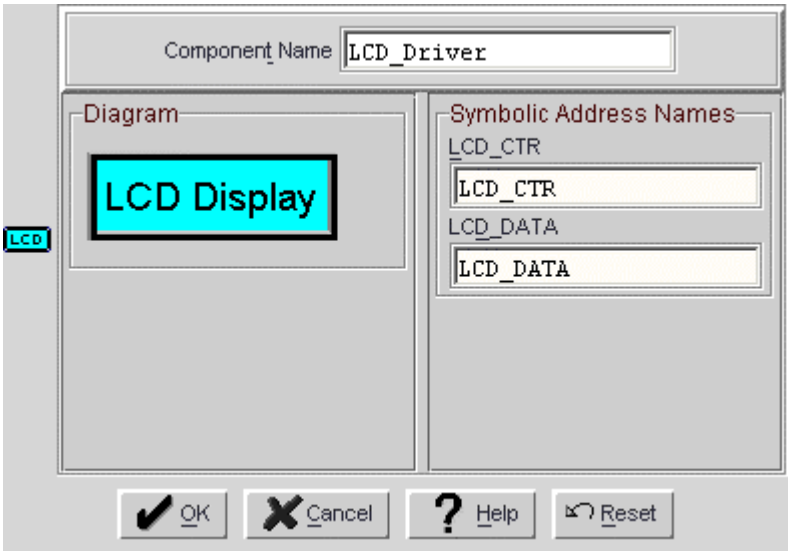


Figure 17. FastChip's LCD Character Display Driver Module.

Use FastChip's I/O Editor, shown in Figure 18, to assign the LCD driver pins to the appropriate TE520 PIO pins, according to Figure 15 and Table 10.

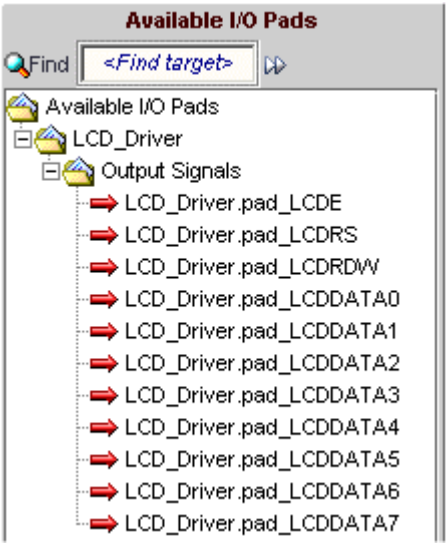


Figure 18. FastChip I/O Editor Displays the LCD Driver Module Pins.

NOTE:

Applications originally created for the iKit 2000 development board also operate on the E5 Development Platform with minimal modifications. Be sure to re-assign PIO locations.

Reclaiming PIO Pins

To reclaim all the PIO connections to the LCD display, simply flip switch SW2.1 to the UP (off) position.

Contrast Adjustment

The character LCD display has an associated contract adjustment potentiometer R17, located immediately to the right of the display, as shown in Figure 15. If you expect to see characters on the display and none appear, try adjusting the potentiometer.

LED Display Bar (LED1)

The base board includes an eight-LED bar display, located immediately above the 8-position DIP-switches along the bottom edge of the board.

The display is split into two groups of four LEDs, as shown in Figure 19. To enable the four left LEDs, flip switch SW2.7 to the DOWN (on) position. To enabled the four right LEDs, flip switch SW2.6 to the DOWN (on) position.

The LED outputs are also shared with some signals from the E5 Evaluation Board's parallel port, as shown in Table 12. If using the LED bar then switch SW6.2 on the evaluation board should be in the UP (off) position to disable the parallel port connections.

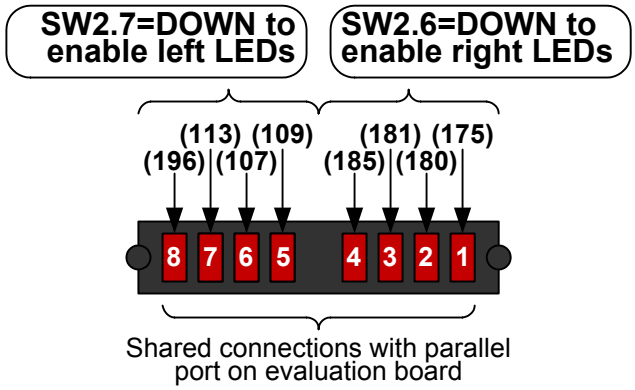


Figure 19. Eight-LED Bar Display.

Table 12 shows the connections to the LED bar display from the TE520. The connections could be shared with some of the parallel port connection if switch SW6.3 is in the DOWN position.

Table 12. LED Bar Pin Connections.

Group	LED	TE520 PIO	Enable Switch	Shared Parallel Port Connection
Left	8	196	SW2.7=DOWN (Left Group)	nSelect-Printer/ nSelect-In
	7	113		nInitialize
	6	107		nAuto-Linefeed
	5	109		nStrobe
Right	4	185	SW2.6=DOWN (Right Group)	Data 7
	3	181		Data 6
	2	180		Data 5
	1	175		Data 4

8-Position DIP-Switches (SW1, SW3)

The base board has two 8-position DIP-switch blocks, as shown in Figure 20. Each individual switch is pulled to VCC through a 10kΩ pull-up resistor. Closing a switch, turning it ON, creates a logic Low. Opening a switch, turning it OFF, opens the connection. The connection is then pulled high via a 10 kΩ pull-up resistor, creating a logic High.

To enable SW1, set switch SW2.2 on the baseboard to the DOWN position.

To enable SW3, set switch SW2.3 to the baseboard to the DOWN position.

Baseboard switch SW1 shares TE520 PIO pins with the right-most LED display on the evaluation board. To disconnect the right-most LED display, remove the JP6 jumper from the E5 Evaluation Board.

Baseboard switch SW3 shares TE520 PIO pins with the 8-position DIP-switch on the evaluation board, SW5. To disconnect SW5, position each switch to the UP position.

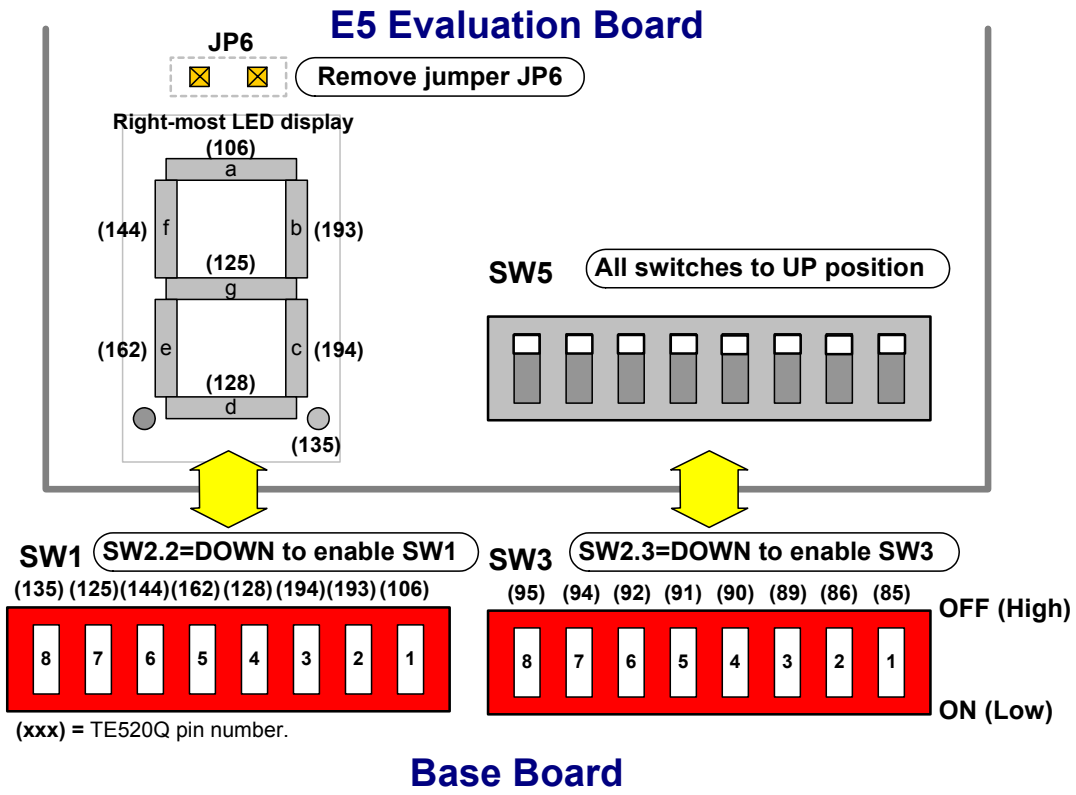


Figure 20. User Switches on Baseboard (SW1, SW3) Share Connections with Evaluation Board.

Four Pushbutton Switches (SW6, SW7, SW8, SW9)

The base board has four black, momentary contact pushbutton switches located immediately below the LCD character display, as shown in Figure 21.

To enable the pushbutton switches, flip switch SW2.8 to the DOWN position. When pressed, the pushbutton switch is shorted to ground, creating a logic Low. When released, the PIO is disconnected and pulled to VCC via a pull-up resistor, creating a logic High.

The two left-most switches, SW6 and SW7, are wired in parallel with the two pushbutton switches on the evaluation board, PB2 and PB1 respectively.

The two right-most switches, SW8 and SW9 share some connections with the right-most 7-segment LED display on the evaluation board.

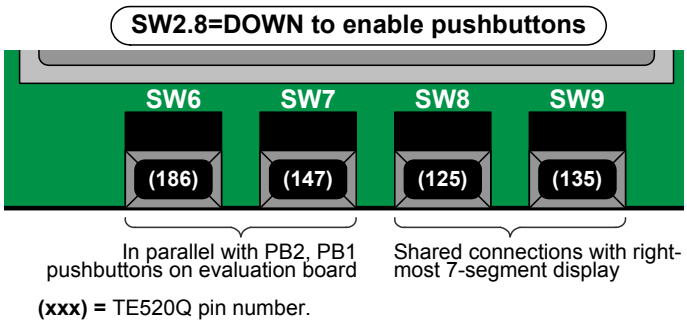


Figure 21. Four Pushbutton Switches.

Table 13 shows the TE520 PIOs that connect to each pushbutton switch.

Table 13. Pushbutton Switch Pin Connections.

Pushbutton	TE520 PIO
SW6	186
SW7	147
SW8	125
SW9	135

Reset Pushbutton (SW5)

When pressed, the RST pushbutton switch directly resets the TE520 device using the RST- input, pin 154. Holding down the button holds the TE520 in reset. When released, the TE520 begins its boot sequence.

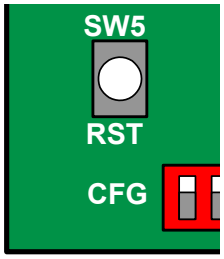


Figure 22. The Base Board Reset Pushbutton is Located in the Lower Left Corner.

The RST pushbutton on the base board is wired in parallel with the Reset pushbutton on the evaluation board.

If the on-board Flash or SRAM is properly enabled using jumpers JP3 and JP4, then the TE520 loads the configuration from Flash or SRAM, regardless of the previously downloaded configuration. If Flash or SRAM is disabled or holds invalid configuration data, the E5 attempts to boot itself and then automatically enter power-down mode because the TE520 VSYS pin is pulled to VCC.

RS-232 Ports with Connectors (RS232-1, RS232-2)

The base board has two DB9 male serial port connectors, as shown in Figure 23, located in the upper left-hand corner near the AC power connector. The RS-232 ports on the base board are completely independent of the RS-232 drivers available on the evaluation board.

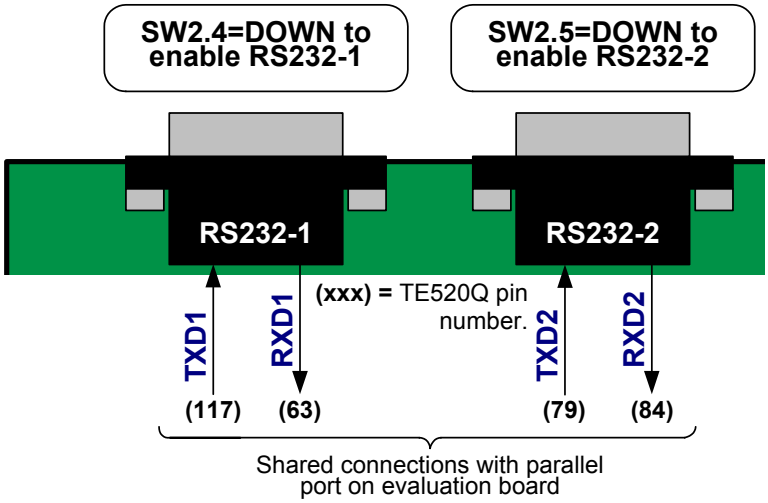


Figure 23. Connections to Two RS-232 Port Connectors.

Pin Connections to TE520

The serial port signals are also shared with some signals from the E5 Evaluation Board's parallel port, as shown in Table 12. If using either serial port, then switch SW6.2 on the evaluation board should be in the UP (off) position to disable the parallel port connections.

Table 14. Base Board RS-232 Port Connections.

RS-232 Port	Signal	TE520 PIO	Enable Switch	Shared Parallel Port Connection
RS232-1	TXD1	117	SW2.4=DOWN	nError/ nFault
	RXD1	63		Select
RS232-2	TXD2	79	SW2.5=DOWN	Paper-Out/ Paper-End
	RXD2	84		nAck

RS-232 Port Connectors

Both serial ports provide a Data Terminal Equipment (DTE) interface, shown in Figure 24, similar to the serial interface found on a PC computer. Typically, a UART within the TE520 drives the serial port. An application uses either the embedded 8051's UART or uses a UART soft IP module from the FastChip library. The data transmit and receive signals must be connected to the PIOs indicated in both Figure 23 and Table 14.

Each 9-pin serial connector is wired for basic loopback handshaking, in case the other end of the connection requires hardware flow control.

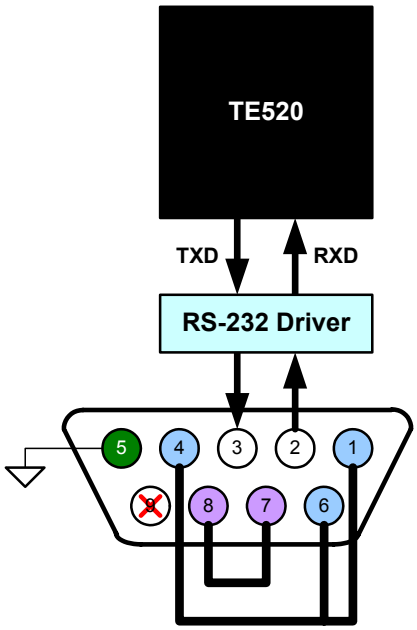


Figure 24. Each Base Board RS-232 Port is a DTE Connection with Loopback Handshaking (view looking into connector from top edge of base board)**.**

Table 15 shows the signals connected to each 9-pin 'D' shell connector. The signals to and from the TE520 are buffered through an RS-232 driver before appearing on the connector.

Table 15. RS-232 Port Signals on 9-Pin Connector.

Pin	RS-232 Function	Connection
1	Data Carrier Detect (DCD)	Connected to DTR, DSR (loopback)
2	Receive Data (RXD)	RS-232 receive data. Buffered receive data arrives as input to TE520. See Table 14.
3	Transmit Data (TXD)	RS-232 transmit data. Transmit data is an output from TE520 to RS-232 driver. See Table 14.
4	Data Terminal Ready (DTR)	Connected to DCD, DSR (loopback)
5	Ground	Ground
6	Data Set Ready (DSR)	Connected to DCD, DTR (loopback)
7	Request to Send (RTS)	Connected to CTS (loopback)
8	Clear to Send (CTS)	Connected to RTS (loopback)
9	Ring Indicator (RI)	No Connect

Cabling Requirements

The base board's RS-232 ports are on the Data Terminal Equipment (DTE) side of the connection. Consequently, to connect the base board to a PC computer, which is another DTE device, you must use a "null" modem connection.

If connecting the base board to a Data Communications Equipment (DCE) device, like a modem, then you may use a standard, "straight-through" serial cable.

512Kx8 Base Board Flash and SRAM Memory

The base board has its own separate external Flash and SRAM, as shown in Figure 25. These are primarily used to hold the TE520's configuration and application program.

Flash memory is non-volatile and holds its contents, even while power is removed from the board. However, reprogramming a Flash memory requires many minutes.

To aid in faster debugging, the base board also includes a large SRAM memory, large enough to simulate Flash. Downloading to SRAM usually takes less than a minute, significantly faster than programming a Flash device. However, SRAM is volatile and loses its contents if you remove power from the board.

The SRAM is also available as a separate memory to store application data. In this mode, the SRAM's enable, read, and write control signals are provided by user-defined logic in the TE520's configurable system logic (CSL) and supplied on three PIO pins.

Memory Jumper Settings

Two jumpers, JP3 and JP4, select the download target memory on the base board. The jumpers are located in the upper right-hand corner of the board, below the 14-page JTAG header, as shown in Figure 25.

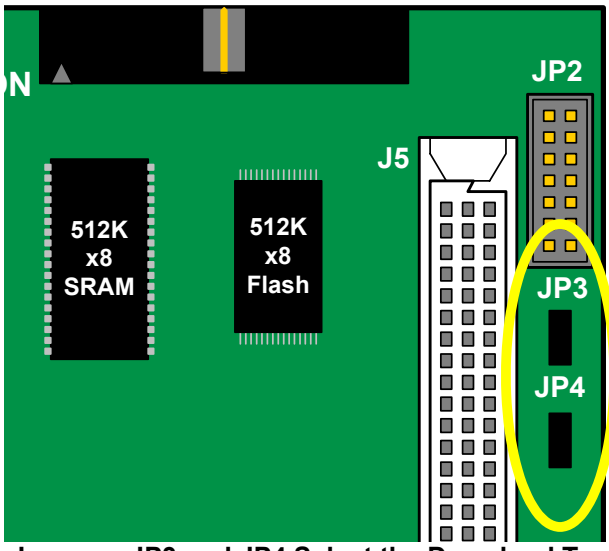


Figure 25. Jumpers JP3 and JP4 Select the Download Target Memory.

NOTE:

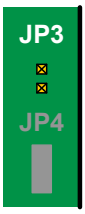
Be sure to disconnect jumper JP4 on the E5 Evaluation Board before attempting to download a design to the base board.

Table 16 shows the jumper settings required to select a specific download target memory.

Applications can always be downloaded to and executed from the TE520's internal SRAM, regardless of the Jumper J3 and J4 settings.

Jumper JP3 must always be installed in order to download to and execute from Flash.

Table 16. Modify Jumpers JP3 and JP4 to Select the Download Target Memory.

Download Target	Diagram	Jumper JP3	Jumper JP4
Internal SRAM		Don't Care	Don't Care
External SRAM		REMOVED	Don't Care
External Flash (disable SRAM)		INSTALLED	REMOVED
External Flash (enable SRAM for use by application as data storage via separate PIO pins)		INSTALLED	INSTALLED

Using External SRAM to Store Application Data

The large, single-cycle 512Kx8 SRAM can optionally be used to store application data. To use the external SRAM in an application, jumpers JP3 and JP4 must both be installed. Installing both jumpers connects the external SRAM's control signals to TE520 PIO pins, instead of the usual Memory Interface Unit (MIU) dedicated outputs, as shown in Figure 26. The data and address signals are still provided by the MIU, however.

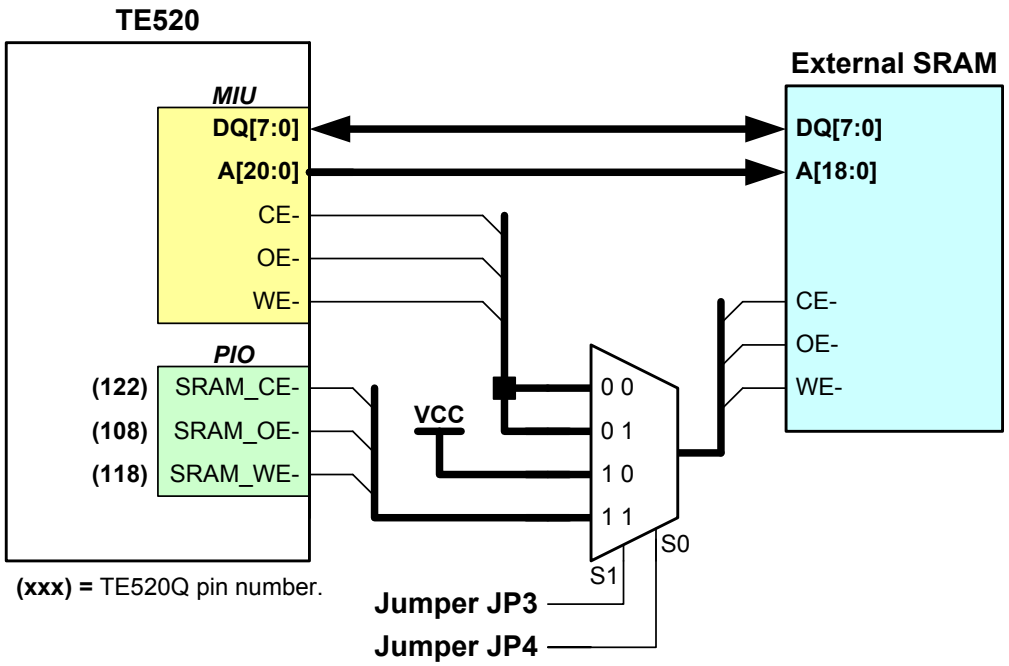


Figure 26. Installing Jumper JP3 and JP4 Allows External SRAM for Application Data.

Table 17 shows the PIO pins that connect to the external SRAM when jumpers JP3 and JP4 are both installed, allowing the application to store data in the SRAM.

Table 17. TE520 Connections to External SRAM when Used for Application Data.

External SRAM Control Signal	TE520 PIO
Chip Enable (CE-)	122
Output Enable (OE-)	108
Write Enable (WE-)	118

The SRAM control signals are supplied by logic in the TE520's Configurable System Logic (CSL). A Chip Select module in the CSL matrix supplies the chip enable control signal to the external SRAM. In The Chip Select module must be configured to drive the MIU when the 8051 or one of the DMA controllers accesses the external SRAM.

For more information on connecting a large external memory to the TE520's Memory Interface Unit (MIU), see application note, **AN10: Setting Up a Secondary External Memory**, available from the Triscend web site.

Auxiliary Connector (AUX, JP1)

The development board has a 26-pin male auxiliary socket, located near the power switch. This optional socket is used to distribute analog and other special signals to off-board connections. Figure 27 shows the pin layout of the socket. All pins are on 0.1-inch centers.

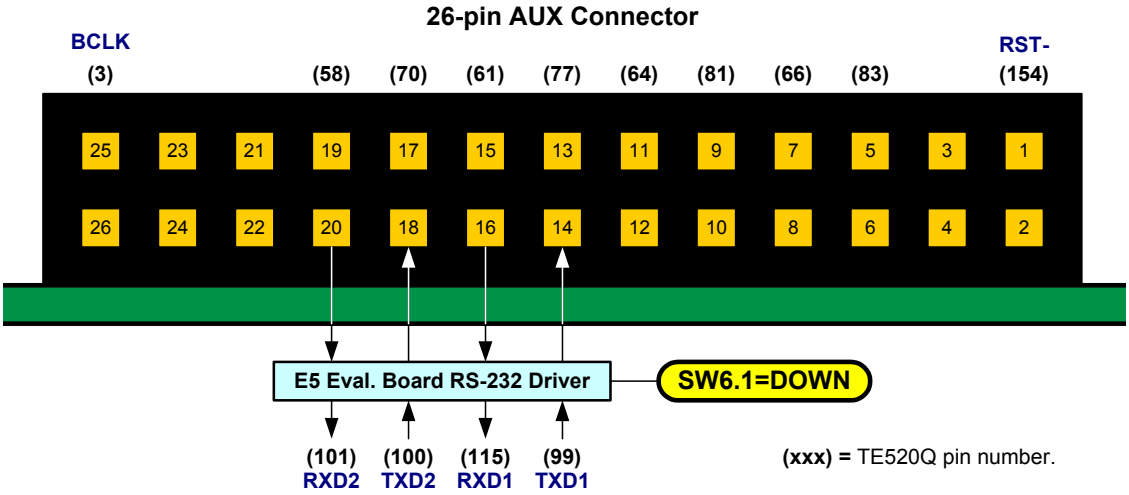


Figure 27. Layout of the Auxiliary Connector, Looking from Top Edge of the Board.

The E5 Evaluation Board optionally uses four pins on the connector—pins 14, 16, 18, and 20—that connect to the RS-232 driver on the evaluation board, when the evaluation board is plugged into the base board and switch SW6.1 is in the DOWN position.

Table 18. Auxiliary Connector Signals.

Socket Pin	Signal Name	TE520 PIO
1	RST-	154
2	+5	—
3	RST- button	—
4	VCC	—
5	AUX16	83
6	GND	—
7	AUX15	66
8	V+	—
9	AUX14	81
10	V-	—
11	AUX13	64
12	Analog ground	—
13	AUX12	77

Socket Pin	Signal Name	TE520 PIO
14	AUX1 (TX1)	99
15	AUX11	61
16	AUX2 (RX1)	115
17	AUX10	70
18	AUX3 (TX2)	100
19	AUX9	58
20	AUX4 (RX2)	101
21	AUX8	—
22	AUX5	—
23	AUX7	—
24	AUX6	—
25	BCLK	3
26	GND	—

Expansion Bus

The base board provides three 96-pin DIN expansion connectors, as shown in Figure 28. Labeled and J1, J2, and J3, these sockets allow easy expansion and prototyping of designs based around the Triscend E5 family.

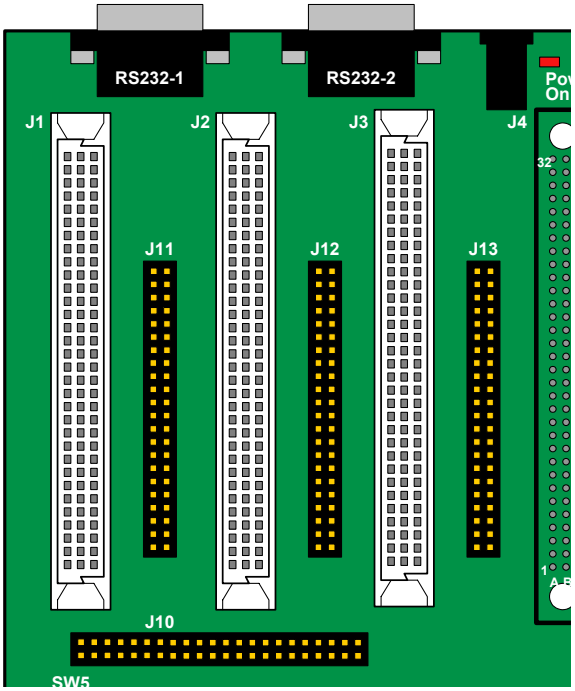


Figure 28. Expansion Bus Connectors and Probe Pins on the Base Board.

The included prototype card plugs into any of the three expansion sockets. Adding special circuitry to the prototype card minimized any disruption to the remainder of the development platform.

A complete connection listing for each expansion socket is provided in Table 20.

Probe Pins

The base board also provides easy-to-use probe point connections, also shown in Figure 28.

The probe pins, shown in their relative locations in Figure 29, provide convenient connections to an oscilloscope, logic analyzer, or to other prototype circuitry.

Signals on connector J11 correspond to signals found on the J1 96-pin DIN expansion bus connector. Similarly, J12 signals correspond to the J2 connector and J13 signals to the J3 connector.

Signals on the J10 connector correspond to a majority of the TE520 system signals, including address, data, and control signals.

The underlined signals connect to one or more I/O devices on the development platform. In the electronic version of this document, these signals are hyperlinked to the TE520 pin description.

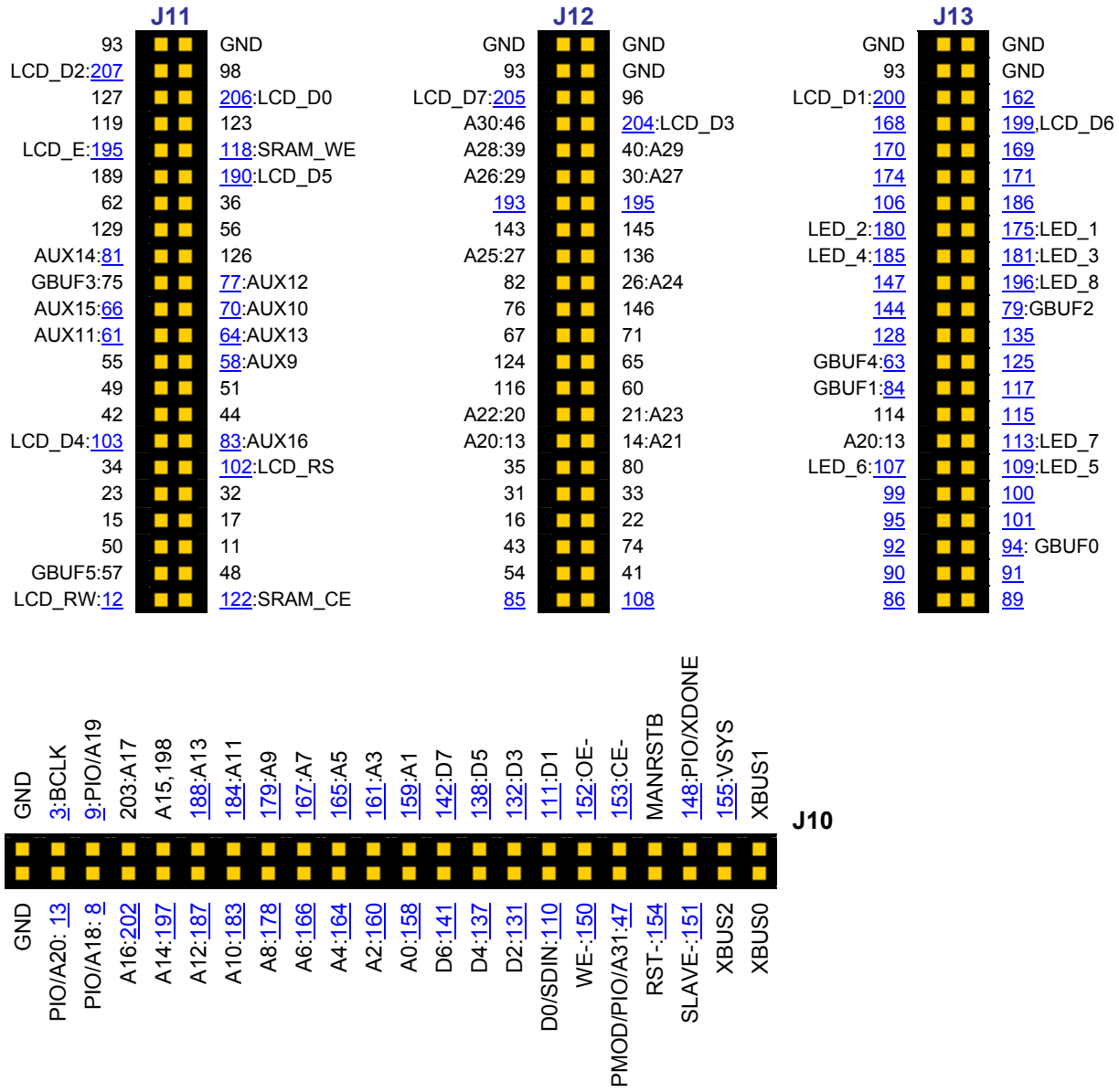


Figure 29. Probe Pins on the Base Board.

Triscend E5 Development Platform

Mounting the E5 Evaluation Board on the Base Board creates the Triscend E5 Development Platform. This section describes how to download to the development platform and how to mount and unmount the evaluation board form the base board.

Downloading to the E5 Development Platform

The E5 Development Platform can be configured and debugged using a standard parallel printer cable connected to your computer's parallel printer port. For future expansion, the base board also has a separate 14-pin JTAG header, JP2.

Using the Parallel Port

To download and debug a design on the E5 Development Platform using the parallel port, please follow these steps, as outlined in Figure 30.

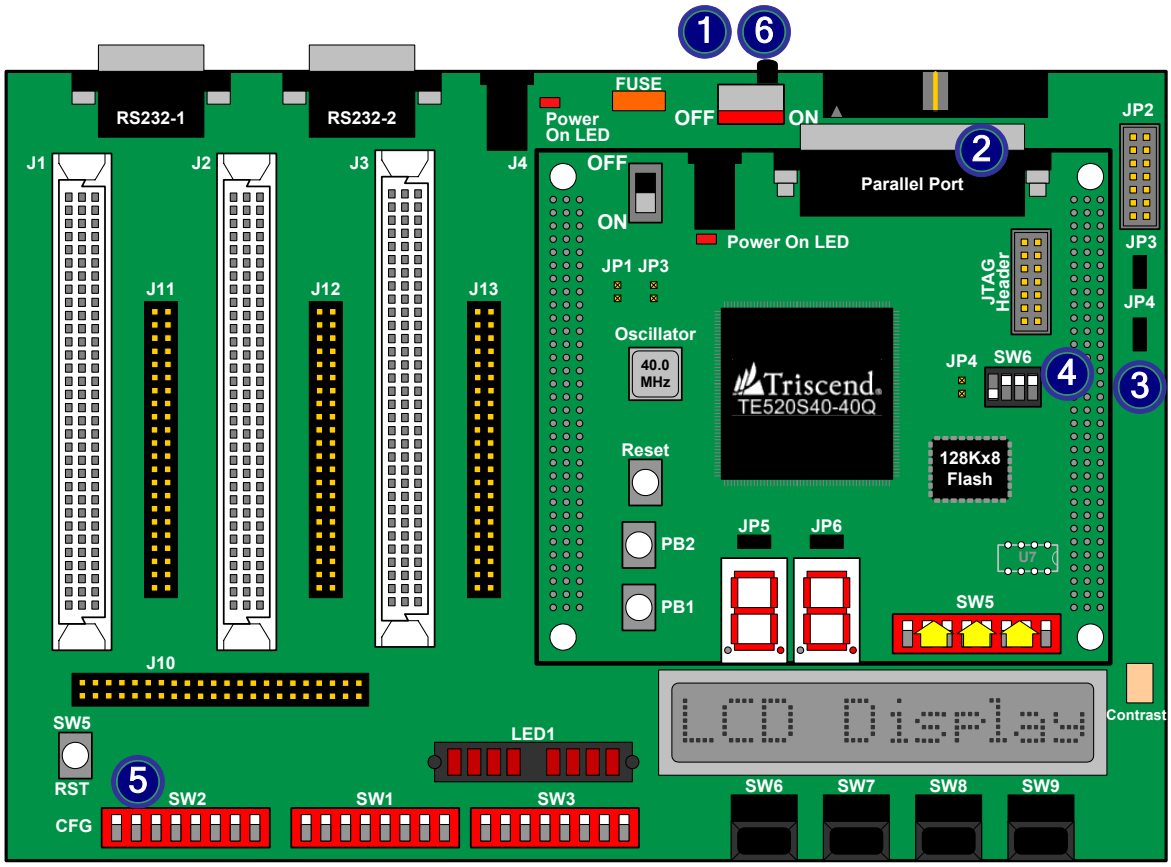


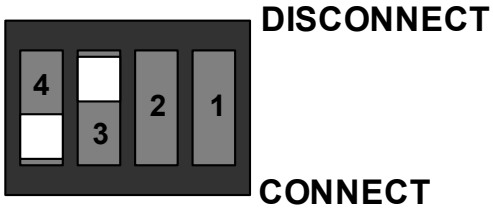
Figure 30. Preparing to Download to the E5 Development Platform.

1 Switch the base board's power switch to the OFF position.

2 Connect a standard 25-pin PC parallel port cable to your computer's parallel port. Connect the other end of the cable to the E5 Evaluation Board using the parallel port connector.

3 Using jumper JP3 and JP4 on the base board, select the desired download target memory.

4 Enable the parallel port connections to the TE520 JTAG pins by switching SW6.4 to the DOWN position. Disconnect other TE520 PIO ports from the same parallel port signals by switching SW6.3 to the UP position. The positions of switches SW6.2 and SW6.1 do not matter.



5 Configure the base board to enable the desired I/O devices using switch SW2.

6 Switch the base board's power switch to the ON position. If there was a previous application stored in Flash, the board will boot from Flash. However, the JTAG interface is able to overwrite any currently-loaded application.

FastChip Device Link (FDL) Configuration Settings

The FastChip Device Link (FDL) utility creates a configuration image for your application that you then download to the development platform. The following configuration options are available, as shown in Figure 31.

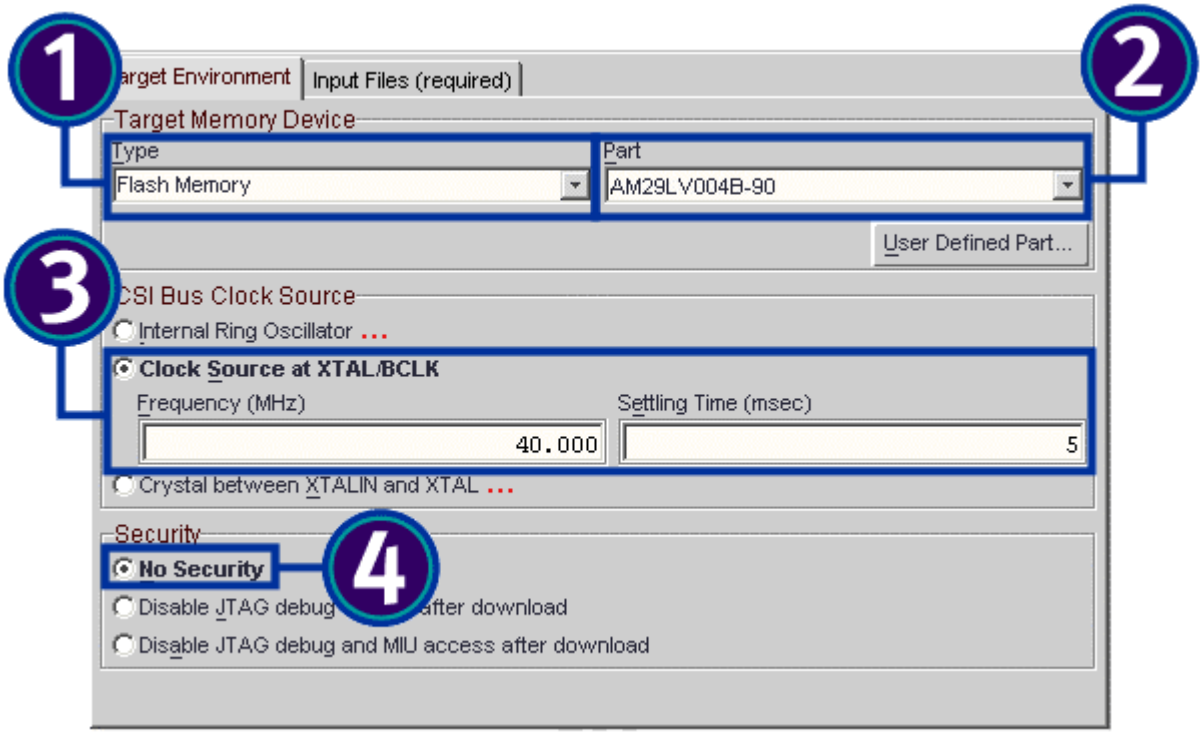


Figure 31. Typical FastChip Device Link (FDL) Settings for Downloading to the Base Board's Flash Memory.

1 Select Target Memory Type

Choose where FDL will download the configuration image. For the E5 Development Platform with the E5 Evaluation Board installed, the available options are as listed below.

- CSoC internal RAM (any JP3, JP4 jumper settings will work)
- Flash Memory (jumper JP3 must be installed)
- External SRAM (jumper JP3 must be removed)

2 Select Memory Part Number

- If downloading to **CSoC internal RAM**, no memory part number is required.
- If downloading to **Flash Memory**, select the Flash part number from your base board. The specific part number may vary, depending on when your board was manufactured.

  At introduction, the base board includes an AMD 512Kx8 (4M-bit) Flash device with 90 ns access time, or **AM29LV004B-90** from the part drop list.
- If downloading to **External SRAM**, select the SRAM device part number from your base board. The specific part number may vary, depending on when your board was manufactured.

  At introduction, the base board includes a Cypress Semiconductor 512Kx8 (4M-bit) SRAM device with 15 ns access time, or **CY7C1046BV33-20** from the part drop list.

3 Choose the CSI Bus Clock Source

There are two potential CSI bus clock sources available. The internal ring oscillator is available within each E5 CSoC device. Its frequency ranges between 5 MHz and 20 MHz.

Typically, however, most applications will use the external crystal clock oscillator provided on the board as it supplies a known, constant frequency.

At introduction, the E5 Evaluation Board includes a **40.000** MHz clock oscillator. Allow **5** ms for the oscillator to settle after power-on.

4 Disable Security Options for Easier Debugging

By default, always choose the **No Security** option when downloading, especially to Flash. If any of the security options are set, you will not be able to debug your application.

Connecting the E5 Evaluation Board to the Base Board

The E5 Evaluation Board functions as a low-cost stand-alone development platform. However, the evaluation board plugs into the baseboard to provide a richer set of capabilities including a LCD character display, two serial port connectors, and an expansion bus suitable for prototype cards.

Before attaching the evaluation board to the baseboard, please follow these steps.

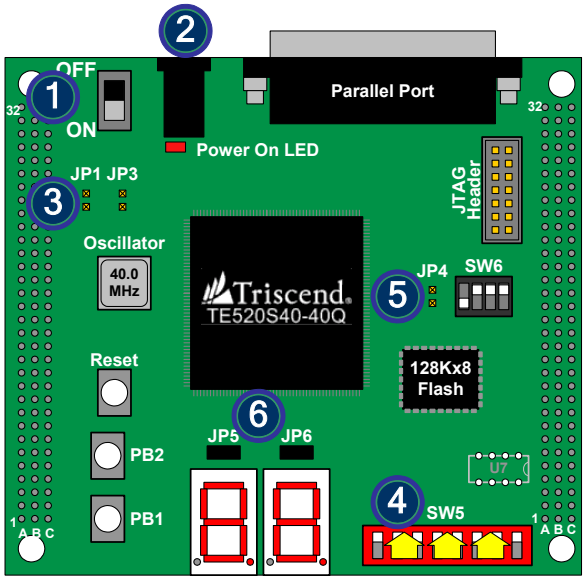


Figure 32. Preparing the Evaluation Board Before Installation on Base Board.

1 Switch the evaluation board's power switch to the OFF position.

2 Unplug the power adaptor from the JP2 barrel connector on the E5 Evaluation Board.

3 Remove jumpers JP1 and JP3. This disconnects the power adaptor connection from the E5 Evaluation Board circuitry. The Base Board will provide all required power.

4 Flip all switches on switch block SW5 to the UP position (all switches off).

5 Remove jumper JP4 to disable the Flash memory on the evaluation board.

6 If reclaiming PIO pins connected to the 7-segment LED display, remove jumpers JP5 and JP6.

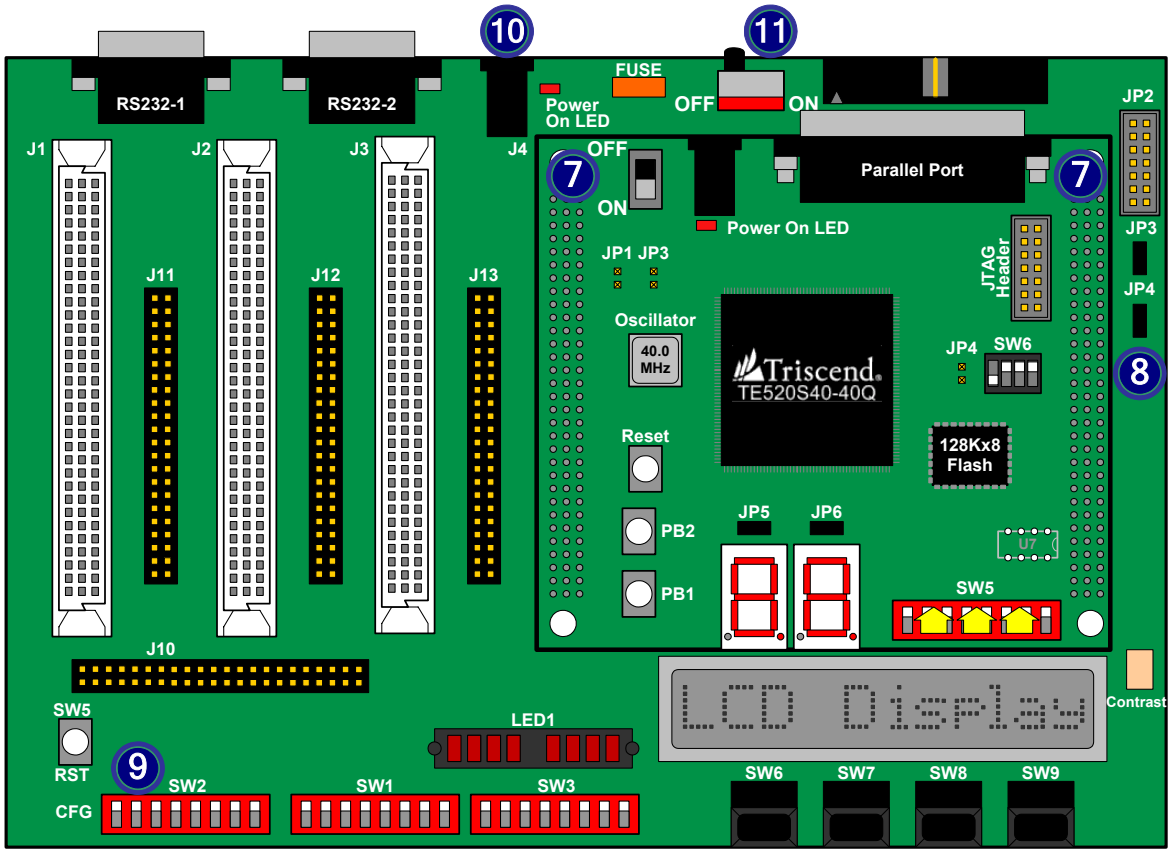


Figure 33. The E5 Evaluation Board Mounted on the Base Board.

7 Insert the E5 Evaluation Board into location on the two 96-pin DIN-connectors above the character LCD display.

8 Modify jumpers JP3 and JP4 on the base board for your preferred download method.

9 Configure the base board to enable the desired I/O devices using switch SW2.

10 Insert the +5VDC/AC power adaptor into the JP6 barrel connector on the base board.

11 Switch the base board's power switch to the ON position.

Removing the E5 Evaluation Board from the Base Board

If the E5 Evaluation Board is already installed on the Base Board and you wish to use the evaluation board in a stand-alone application, follow these steps to remove and prepare the evaluation board.

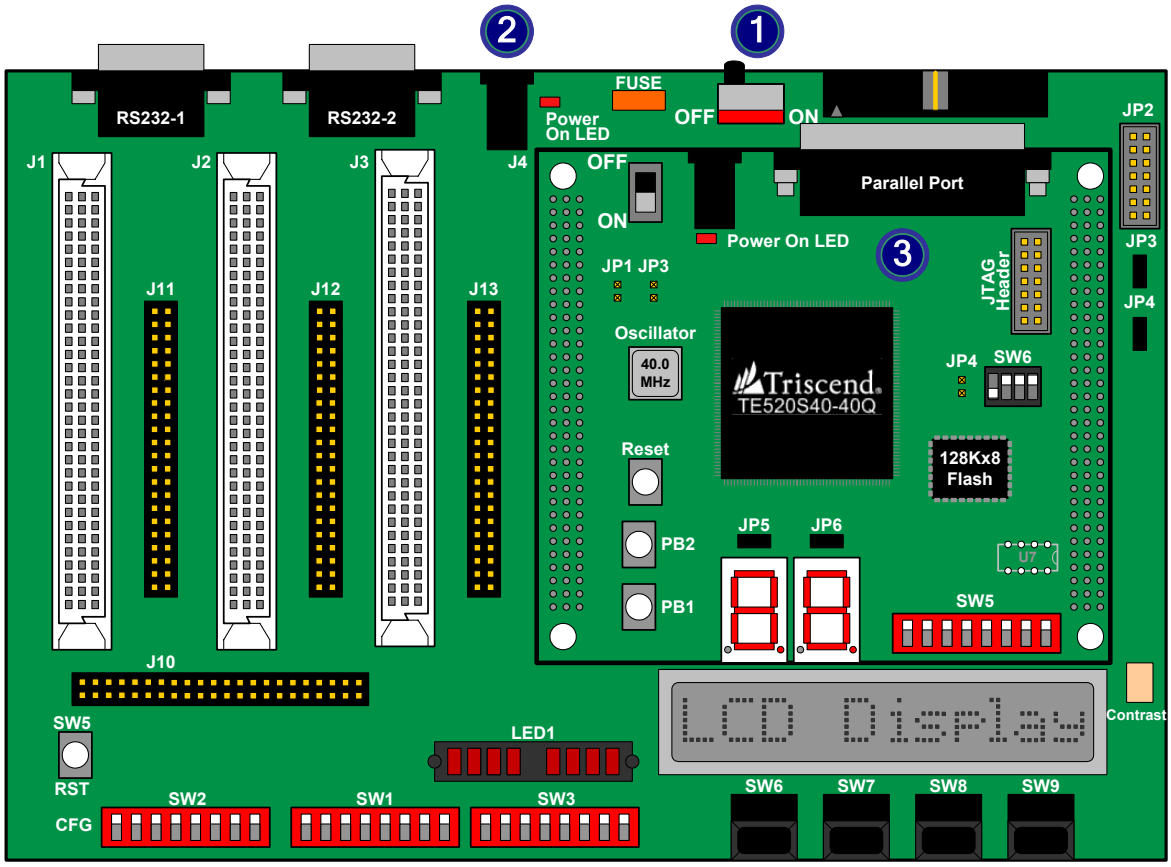


Figure 34. Preparing to Remove the E5 Evaluation Board from the Base Board.

1 Switch the base board's power switch to the OFF position.

2 Unplug the power adaptor from the barrel connector on the base board.

3 Firmly grasp the E5 Evaluation Board by the edges and gently rock it to separate the board from the base board's DIN connectors.

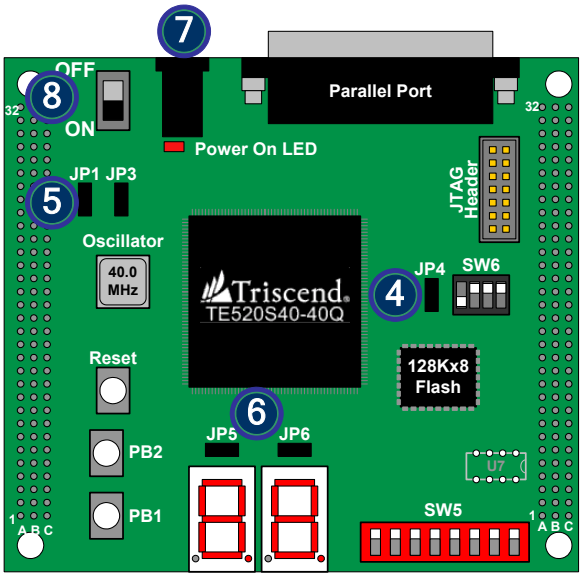


Figure 35. Preparing the Evaluation Board for Stand-Alone Operation.

4 Re-install jumper JP4 to enable the evaluation board's Flash memory.

5 Re-install jumpers JP1 and JP3 to enable the on-board power supply.

6 If previously removed, re-install jumper JP5 and JP6 to enable the two 7-segment LED displays.

7 Insert the +5VDC/AC power adaptor into the JP2 barrel connector on the evaluation board.

8 Switch the evaluation board's power switch to the ON position.

Troubleshooting Guide

Evaluation Board

Power-on LED doesn't light up

- Check that the +5VDC power adaptor is connected to the power jack and to AC wall power.
- Check that the power switch is turned ON. The Power-On LED should be lit.
- Check the integrity of the fuse. The fuse is designated at component F1 and is located on the bottom side of the board, near the power adaptor, the parallel port connector, and the +3.3V regulator. Using an ohmmeter or connectivity tester, check to see if there is a connection between both sides of the fuse.

7-segment LEDs don't light up

- Observe the Power-On LED. Check that power is applied to the board.
- If using the evaluation board stand-alone, without the base board, check that jumpers JP1 and JP3 are installed.
- Check that jumpers JP5 and JP6 are installed.
- Check that the application inside the Triscend E5 CSoC device drives the selected segment Low to light the segment.

7-segment LEDs momentarily glow slightly and then light up

- If driven by signals controlled by the pushbutton switches or the DIP switches, this condition might be caused because pull-ups are required in PIO pins, in order to create a logic High.

FDL: "Unable to reset and halt CSoC. Command Halted"

- Press the Reset pushbutton.
- Try downloading again.
- If still unable to connect, quit and restart FDL.

FDL: "No Communication With Target"

- Check Option Switch Settings (SW6). Check that the settings match your intended download method.
- Check that the security options are not set in your FDL configuration options. If the security options were set and your application is downloaded into Flash, please follow these steps.
  - Turn off power to the board.
  - Remove jumper JP4, near switch SW6.
  - Re-apply power to the board.
  - Download any design to internal SRAM.
  - Replace jumper JP4. There is no need to disconnect power.
  - Download your application to Flash.

Development Platform (E5 Evaluation Board + Base Board)

Power-on LED doesn't light up

- Check that the +5VDC power adaptor is connected to the power jack and to AC wall power.
- Check that the power switch is turned ON. The Power-On LED should be lit.

- Check the integrity of the fuse, located adjacent to the base board's power switch. Using an ohmmeter or connectivity tester, check to see if there is a connection between both sides of the fuse.
- If there is no continuity, remove the socketed fuse from the base board and insert the replacement fuse shipped with the base board.

LCD display: No characters visible

- Switch SW2.1 must be in the DOWN position to enable the display.
- Characters may not display if the contrast is set too low. Adjust potentiometer R17 to see if text appears.

FDL Download: "The MIU size setting (256KB) is not large enough"

- Change MIU settings. The size settings are available within FastChip by selecting **Constraints → I/O Editor**.
- Click the **MIU** button and select the proper size settings for your target download memory.
- Click the **Bind** button to create a new CSoC design.
- Within FDL, **Configure** and **Download** the new design.

7-segment LEDs on evaluation board flicker but not being used

- Some of the 7-segment LED connections are shared with resources on the base board
- If the 7-segment LED is not being used in the application, remove either jumper JP5 or JP6 on the evaluation board.

General

Unable to create a precise UART baud rate using the 40.000 MHz oscillator

- If you are using the E5's dedicated UART, please visit the following web link.

  How Do I Set the Baud-Rate for the 8051's Dedicated UART?
  http://portal.knowledgebase.net/article.asp?article=9661&p=171

- If you are using a CSL-based UART, please visit the following web link.

  How Do I Set the Baud-Rate for the Full UART Soft IP Module?
  http://portal.knowledgebase.net/article.asp?article=9576&p=171

- Both web links have an associated Excel spreadsheet for calculating baud rates for any input frequency.
- The crystal oscillator component is socketed on the evaluation board. You can remove the 40.000 MHz component and replace it with the one of your choice.

TE520 Device Pin Connections to Board Resources

Table 19 lists the connections for every pin on the TE520 device, including connections to the …

- J1 and J2 connectors on the evaluation board, which are identical to the base board's J4 and J5 connector footprints
- J1, J2, and J3 expansion bus connectors on the base board
- J10, J11, J12, and J13 probe point stake pins on the base board

AUX: Auxiliary connector on the base board, (x) indicates connector pin number.

JTAG: TE520 JTAG connections. Signal name indicated. Used to download and debug a CSoC application.

LCD: LCD character display on the base board. Signal name indicated. Enabled by SW2.1=DOWN. Shares connections with left-most 7-segment LED display on evaluation board.

L7S: Left 7-segment LED display on the E5 Evaluation Board, segment name indicated. Enabled when evaluation board jumper JP5 is installed. Shares connections with LCD character display.

R7S: Right 7-segment LED display on the E5 Evaluation Board, segment name indicated. Enabled when evaluation board jumper JP6 is installed. Shares connections with 8-position DIP-switch SW1 on the base board.

PP: Parallel Port. Signal name indicated, (x) indicates connector pin number. Configuration switch SW6 on the evaluation board optionally connects parallel port signals to the TE520's JTAG pins or to user-defined PIO pins.

SRAM: SRAM on base board. Controlled by jumpers JP3 and JP4 on the base board.

Flash: Flash on both evaluation and base board. When using the evaluation board in stand-alone mode, install jumper JP4 on the evaluation board. When using the evaluation board mounted on the base board, remove jumper JP4 on the evaluation board, use base board jumpers JP3 and JP4 to control Flash as a download target.

PB: Pushbutton switches on the evaluation board.

SWx.y: Switch. The value of 'x' identifies the specific switch. If the location is a switch block, the value of 'y' indicates the specific switch within the block.

LED: LED bar display. LED segment number indiated. The left and right sides of the display are separately enabled. Switch SW2.7 controls the left side. Switch SW2.6 controls the right side.

SP: RS-232 serial ports on base board. Transmit (TXD) or receive (RXD) indicated, along with port number.

ED: RS-232 drivers on evaluation board. Transmit (TXD) or receive (RXD) indicated, along with port number. There are no associated connectors.

Note: The evaluation board connects to the base board via the J1 and J2 96-pin DIN connectors. Consequently, the J1 96-pin DIN connector footprint on the evaluation board is identical to the J4 connector on the base board. Similarly, the J2 connector is identical to the J5 connector on the base board.

Table 19. Complete TE520 Pin Connections List.

Pin	Name	Connections	E5 Eval.		Base Board							Notes
			96-pin DIN		96-pin DIN			Probe Pins				
			J1	J2	J1	J2	J3	J10	J11	J12	J13	
1	GNDIO											
2	XTALIN											
3	BCLK/ XTAL	AUX: (25)	A17					41				
4	TDI	**JTAG**: TDI	B16									
5	TDO	**JTAG**: TDO	A16									
6	TCK	**JTAG**: TCK	B15									
7	TMS	**JTAG**: TMS	A15									
8	PIO/A18		A12		A32	A32	A32	40				
9	PIO/A19		C11		A12	A12	A12	39				
10	GNDIO											
11	PIO											
12	PIO	LCD: RW	B14		A1				2			
13	PIO/A20		B11		A20	A20	A20	42		14	14	
14	PIO/A21		A11			C7				13		
15	PIO											
16	PIO											
17	PIO											
18	VCCIO											
19	GNDIO											
20	PIO/A22		C10			A8				16		
21	PIO/A13		B10			B8				15		
22	PIO											
23	PIO											
24	VCC											
25	GND											
26	PIO/A24		A10			B12				25		
27	PIO/A25		C9			C12				28		
28	GNDIO											
29	PIO/A26		B9			A19				34		
30	PIO/A27		A9			B19				33		
31	PIO											
32	PIO											
33	PIO											
34	PIO											
35	PIO											
36	PIO											
37	VCCIO											
38	GNDIO											
39	PIO/A28		B8			C19				36		
40	PIO/A29		A8			A20				35		
41	PIO											
42	PIO											
43	PIO											
44	PIO											
45	GNDIO											
46	PIO/A30		C7			B20				38		
47	PMOD/ PIO/A31		B7		C18	C18	C18	10				4.7K pull-up resistor

Pin	Name	Connections	E5 Eval.		Base Board							Notes
			96-pin DIN		96-pin DIN			Probe Pins				
			J1	J2	J1	J2	J3	J10	J11	J12	J13	
48	PIO											
49	PIO											
50	PIO											
51	PIO											
52	VCCIO											
53	GNDIO											
54	PIO											
55	PIO											
56	PIO											
57	PIO/ GBUF5											
58	PIO	AUX: AUX9, (19)		A5	A9				19			
59	GNDIO											
60	PIO											
61	PIO	AUX: AUX11, (15)		C5	B9				22			
62	PIO											
63	PIO/ GBUF4	SP: RXD1 PP: Select, (13)		B6			B9				20	
64	PIO	AUX: AUX13, (11)		C6	C9				21			
65	PIO											
66	PIO	AUX: AUX15, (7)		B7	A10				24			
67	PIO											
68	VCCIO											
69	GNDIO											
70	PIO	AUX: AUX10, (17)		B5	C10				23			
71	PIO											
72	VCC											
73	GND											
74	PIO											
75	PIO/ GBUF3											
76	PIO											
77	PIO	AUX: AUX12, (13)		A6	B11				25			
78	GNDIO											
79	PIO/ GBUF2	SP: TXD2 PP: Paper End, (12)		B10			B11				23	
80	PIO											
81	PIO	AUX: AUX14, (9)		A7	C11				28			
82	PIO											
83	PIO	AUX: AUX16, (5)		C7	A7				13			
84	PIO/ GBUF1	SP: RXD2 PP: nAck, (10)		B12			C8				18	
85	PIO	SW1.1 SW5.1		C12		A1				2		
86	PIO	SW1.2 SW5.2		A13			A1				2	
87	VCCIO											
88	GNDIO											
89	PIO	SW1.3 SW5.3		B13			A2				1	
90	PIO	SW1.4 SW5.4		C13			B2				4	

Pin	Name	Connections	E5 Eval.		Base Board							Notes
			96-pin DIN		96-pin DIN			Probe Pins				
			J1	J2	J1	J2	J3	J10	J11	J12	J13	
91	PIO	SW1.5 SW5.5		A14			A3				3	
92	PIO	SW1.6 SW5.6		B14			B3				6	
93	PIO			C14	C32	C32	C32		44	42	42	
94	PIO/ GBUF0	SW1.7 SW5.7		A15			A4				5	
95	PIO	SW1.8 SW5.8		B15			B4				8	
96	PIO											
97												
98	PIO											
99	PIO	ED: TXD1 AUX: AUX1, (14)		C16			A5				10	
100	PIO	ED: TXD2 AUX: AUX3, (18)		A17			B5				9	
101	PIO	ED: RXD2 AUX: AUX4, (20)		B17			C4				7	
102	PIO	LCD: RS		C17	B6				11			
103	PIO	LCD: LCD_D4 L7S: 'e'		A18	C6				14			
104	VCCIO											
105	GNDIO											
106	PIO	SW3.1 R7S: 'a'		B18			A15				32	
107	PIO	LED: 6 PP: AutoLineFeed, (14)		C18			C5				12	
108	PIO	SRAM: OE-		C24		A2				1		
109	PIO	LED: 5 PP: nStrobe, (1)		A25			A7				11	
110	D0/ SDIN	D0		C21	C25	C25	C25	14				
111	D1/PIO	D1		A22	A26	A26	A26	13				
112	GNDIO											
113	PIO	LED: 7 PP: nInitialize, (16)		B25			C7				13	
114	PIO			C25			A8				16	
115	PIO	ED: RXD1 AUX: AUX2, (16)		A26			B8				15	
116	PIO											
117	PIO	SP: TXD1 PP: Error, (15)		C26			A9				17	
118	PIO	SRAM: WE-		A27	B19				35			
119	PIO											
120	VCCIO											
	GNDIO											
122	PIO	SRAM: CE-		C27	A2				1			
123	PIO											
124	PIO											
125	PIO	SW3.7 R7S: 'g' SW8		A29			C9				19	
126	PIO											
127	PIO											
128	PIO	SW3.4 R7S: 'd'		A30			A10				22	

Pin	Name	Connections	E5 Eval.		Base Board							Notes
			96-pin DIN		96-pin DIN			Probe Pins				
			J1	J2	J1		J3	J10	J11	J12	J13	
129	PIO											
130	GNDIO											
131	D2/PIO	D2		B22	B26	B26	B26	16				
132	D3/PIO	D3		C22	C26	C26	C26	15				
133	VCC											
134	GND											
135	PIO	SW3.8 R7S: 'dp' SW9		C30			C10				21	
136	PIO											
137	D4/PIO	D4		A23	A28	A28	A28	18				
138	D5/PIO	D5		B23	B28	B28	B28	17				
139	VCCIO											
140	GNDIO											
141	D6/PIO	D6		C23	C28	C28	C28	20				
142	D7/PIO	D7		B24	A29	A29	A29	19				
143	PIO											
144	PIO	SW3.6 R7S: 'f'		C31			A11				24	
145	PIO											
146	PIO											
147	PIO	PB2 SW7		C32			C11				26	
148	PIO/ XDONE		C32		C14	C14	C14	5				
149	GNDIO											
150	WE-/ SEN-	Flash: WE- (eval) Flash: WE- (base) SRAM: WE-		B19	C23	C23	C23	10				
151	SLAVE-	SLAVE-		C19	B13	B13	B13	6				4.7K pull-up resistor
152	OE-/ SRST	Flash: OE- (eval) Flash: OE- (base) SRAM: OE-		B20	A24	A24	A24	11				
153	CE-	Flash: CE- (eval) Flash: CE- (base) SRAM: OE-		C20	A23	A23	A23	9				
154	RST-	Reset button (eval) Reset button (base) AUX: (1) Reset circuit (base)		A21	A18	A18	A18	8				
155	VSYS	VSYS		B21	A13	A13	A13	3				4.7K pull-up resistor
156	VCCIO											
157	GNDIO											
158	A0/ SCLK	A0	C29		C20	C20	C20	22				
159	A1/PIO	A1	B29		A21	A21	A21	21				
160	A2/PIO	A2	A29		B21	B21	B21	24				
161	A3/PIO	A3	B28		C21	C21	C21	23				
162	PIO	SW3.5 R7S: 'e'	B32				C31				39	
163	GNDIO											
164	A4/PIO	A4	A28		A22	A22	A22	26				
165	A5/PIO	A5	C27		B22	B22	B22	25				

Pin	Name	Connections	E5 Eval.		Base Board							Notes
			96-pin DIN		96-pin DIN			Probe Pins				
			J1	J2	J1		J3	J10	J11	J12	J13	
166	A6/PIO	A6	B27		C22	C22	C22	28				
167	A7/PIO	A7	A27		B24	B24	B24	27				
168	PIO	PP: Busy, (11) JTAG: TDO	A16				B20				38	*
169	PIO	PP: Data 0, (2)		A21			A20				35	*
170	PIO	PP: Data 1, (3) JTAG: TMS	A15				C19				36	
171	PIO	PP: Data 2, (4) JTAG: TCK	B15				B19				33	
172	VCCIO											
173	GNDIO											
174	PIO	PP: Data 3 (5) JTAG: TDI	B16				A19				34	
175	PIO	LED: 1 PP: Data 4, (6)	B30				B14				29	
176	VCC											
177	GND											
178	A8/PIO	A8	C26		C24	C24	C24	30				
179	A9/PIO	A9	B26		A25	A25	A25	29				
180	PIO	LED: 2 PP: Data 5, (7)	A30				A14				30	
181	PIO	LED: 3 PP: Data 6, (8)	A23				C13				27	
182	GNDIO											
183	A10/PIO	A10	A26		B25	B25	B25	32				
184	A11/PIO	A11	C26		B29	B29	B29	31				
185	PIO	LED: 4 PP: Data 7, (9)	C22				C12				28	
186	PIO	PB1 SW6	B22				B13				31	
187	A12/PIO	A12	B26		C29	C29	C29	34				
188	A13/PIO	A13	A26		A30	A30	A30	33				
189	PIO		C22		A15				34			
190	PIO	LCD: LCD_D5 L7S: ‘f’	C21		B15				33			
191	VCCIO											
192	GNDIO											
193	PIO	SW3.2 R7S: ‘b’	B21			A15				32		
194	PIO	SW3.3 R7S: ‘c’	A21			B15				31		
195	PIO	LCD: E	B20		A19				36			
196	PIO	LED: 8 PP: nSelect, (17)	A20				B12				25	
197	A14/PIO	A14	B24		B30	B30	B30	36				
198	A15/PIO	A15	A24		C30	C30	C30	35				
199	PIO	LCD: LCD_D6 L7S: ‘g’	B19				B27				37	
200	PIO	LCD: LCD_D1 L7S: ‘b’	A19				C27				40	
201	GNDIO											
202	A16/PIO	A16	C23		A31	A31	A31	38				
203	A17/PIO	A17	B23		B31	B31	B31	37				
204	PIO	LCD: LCD_D3 L7S: ‘d’	B18			B27				37		
205	PIO	LCD: LCD_D7	A18			C27				40		

Pin	Name	Connections	E5 Eval.		Base Board							Notes
			96-pin DIN		96-pin DIN			Probe Pins				
			J1	J2	J1		J3	J10	J11	J12	J13	
		L7S: 'dp'										
206	PIO	LCD: LCD_D0 L7S: 'a'	C17		B27				39			
207	PIO	LCD: LCD_D2 L7S: 'c'	B17		C27				42			
208	VCCIO											

Base Board Expansion Bus Connections

Table 20 provides a complete connection list for the J1, J2, and J3 expansion connectors on the base board. The signals are color coded according to function as shown below.

Legend

Analog power and ground
Unique to J1 only
Unique to J2 only
Unique to J3 only
E520 bussed pins
+5VDC
Digital GND
+3.3VDC
Other bussed pins

Total Active Pins: 161

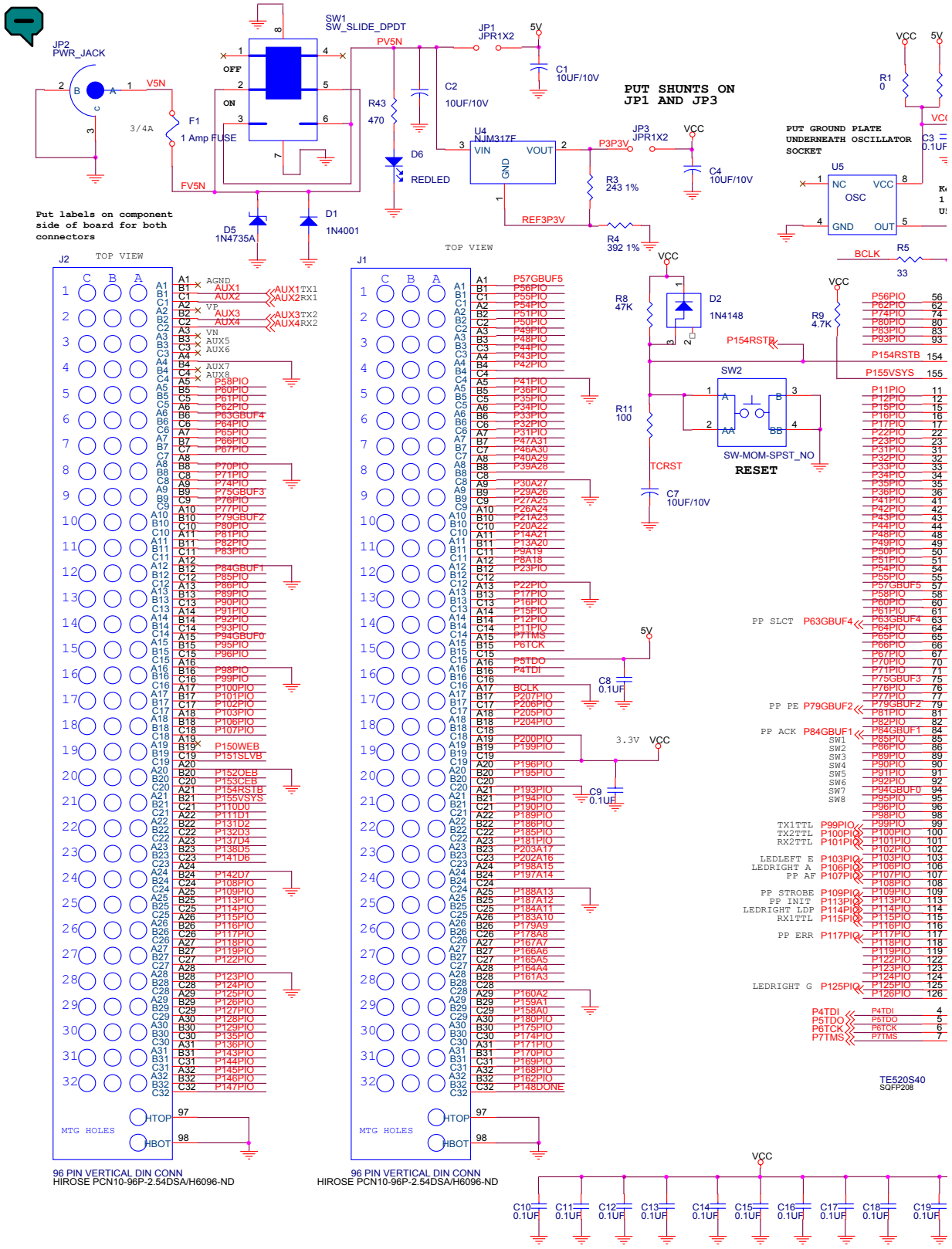
Table 20. Detailed Connection List for the J1, J2, and J3 Expansion Connectors on the Base Board.

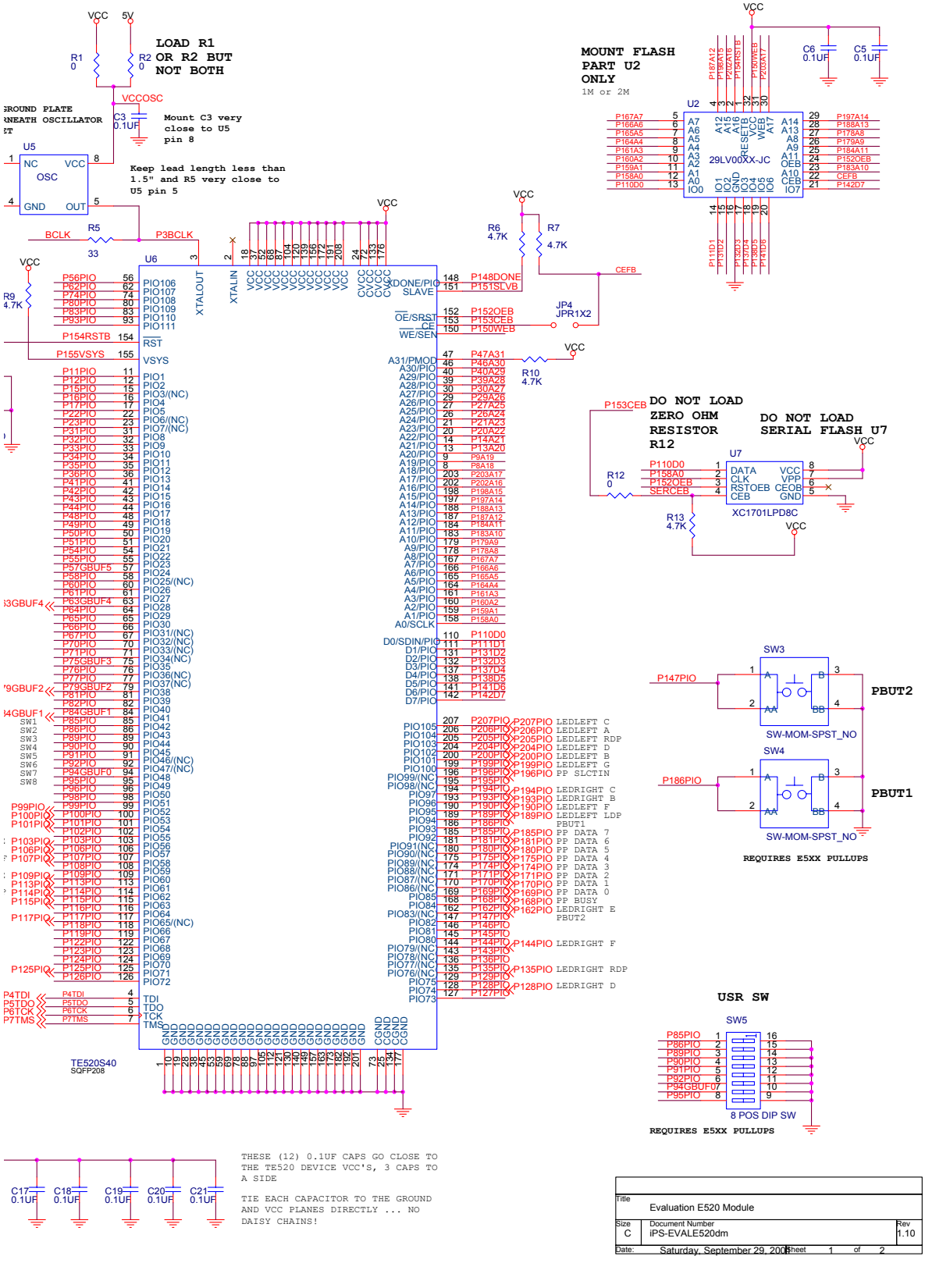
J1			J2			J3		
Pin	**Description**	**TE520**	**Pin**	**Description**	**TE520**	**Pin**	**Description**	**TE520**
A1	PIO	12	A1	PIO	85	A1	PIO	86
B1	XBUS0	NC	B1	XBUS0	NC	B1	XBUS0	NC
C1	AGND		C1	AGND		C1	AGND	
A2	PIO	122	A2	PIO	108	A2	PIO	89
B2	PIO/GBUF5	57	B2	PIO	54	B2	PIO	90
C2	V+		C2	V+		C2	V+	
A3	PIO	48	A3	PIO	41	A3	PIO	91
B3	PIO	50	B3	PIO	43	B3	PIO	92
C3	V-		C3	V-		C3	V-	
A4	PIO	11	A4	PIO	74	A4	PIO/GBUF0	94
B4	PIO	15	B4	PIO	16	B4		95
C4	PIO		C4	PIO	22	C4	PIO	101
A5	PIO	23	A5	PIO	31	A5		99
B5	PIO	32		PIO	33		PIO	100
C5	PIO	34	C5	PIO	35	C5	PIO	107
A6	DGND			DGND		A6	DGND	
B6	PIO	102	B6	XBUS1	NC	B6	XBUS1	NC
C6	PIO	103		XBUS2	NC	C6	XBUS2	NC
A7		83	A7	PIO	80	A7	PIO	109
	PIO	42	B7	PIO/A20	13	B7		13
C7	PIO	44	C7	PIO/A21	14	C7	PIO	113
A8	PIO	49	A8	PIO/A22	20	A8	PIO	114
B8		51	B8	PIO/A23	21	B8	PIO	115
C8	PIO	55	C8	PIO	116	C8	PIO/GBUF1	84
A9		58	A9	PIO	60	A9		117
B9	PIO/AUX11	61		PIO	124	B9	PIO/GBUF4	63
C9	PIO/AUX13	64		PIO	65	C9		125
A10	PIO/AUX15	66	A10	PIO		A10	PIO	128
B10	DGND			DGND		B10		
C10	PIO/AUX10	70	C10		71	C10	PIO	135

J1			J2			J3		
Pin	Description	TE520	Pin	Description	TE520	Pin	Description	TE520
A11	PIO/GBUF3	75	A11		76	A11	PIO	144
	PIO/AUX12	77	B11	PIO	146	B11	PIO/GBUF2	79
	PIO/AUX14	81	C11	PIO	82	C11	PIO	147
A12	PIO/A19		A12	PIO/A19	9	A12	PIO/A19	9
B12	PIO		B12	PIO/A24	26	B12	PIO	196
C12	PIO	129		PIO/A25	27	C12	PIO	185
A13	VSYS	155	A13	VSYS	155	A13	VSYS	155
B13	SLAVEB	151	B13	SLAVEB	151	B13	SLAVEB	151
C13		56	C13	PIO	136		PIO	181
A14	PIO	62	A14	PIO	143	A14	PIO	180
B14	PIO	36	B14	PIO	145	B14	PIO	175
C14	DONE/PIO	148	C14	DONE/PIO	148	C14	DONE/PIO	148
A15	PIO	189	A15	PIO	193	A15	PIO	106
B15	PIO	190	B15	PIO	194	B15	PIO	186
C15	5V	5V	C15				5V	
A16	DGND		A16	DGND		A16	DGND	
B16	DGND		B16	DGND		B16	DGND	
C16			C16	DGND		C16	DGND	
A17	3.3V		A17	3.3V		A17		
	3.3V			3.3V			3.3V	
	3.3V		C17	3.3V		C17	3.3V	
A18	RSTB	154	A18	RSTB	154	A18	RSTB	154
B18	MAN_RSTB		B18	MAN_RSTB		B18	MAN_RSTB	
C18	A31/PMOD	47	C18	A31/PMOD	47	C18	A31/PMOD	47
A19	PIO	195	A19	PIO/A26	29		PIO	174
B19		118	B19		30	B19	PIO	171
C19	PIO		C19	PIO/A28	39	C19		170
A20		123	A20	PIO/A29	40	A20	PIO	169
B20	PIO	127	B20	PIO/A30	46	B20	PIO	168
	A0/SCLK	158		A0/SCLK	158	C20	A0/SCLK	158
A21	PIO/A1	159	A21	PIO/A1	159	A21	PIO/A1	159
B21	PIO/A2	160	B21	PIO/A2	160	B21	PIO/A2	160
C21	PIO/A3	161	C21	PIO/A3	161	C21	PIO/A3	161
A22	PIO/A4	164	A22		164	A22		164
B22	PIO/A5	165	B22	PIO/A5		B22	PIO/A5	165
C22		166	C22	PIO/A6	166	C22	PIO/A6	166
A23		153	A23	CEB	153	A23		153
B23	DGND		B23	DGND		B23	DGND	
C23	WEB	150		WEB	150	C23	WEB	150
A24	OEB	152	A24	OEB	152	A24	OEB	152
B24	PIO/A7	167	B24	PIO/A7	167	B24	PIO/A7	167
C24		178	C24	PIO/A8	178		PIO/A8	178
A25	PIO/A9	179	A25	PIO/A9	179	A25		179
	PIO/A10	183		PIO/A10	183		PIO/A10	183
C25	D0/SDIN	110		D0/SDIN	110	C25	D0/SDIN	110
A26	PIO/D1	111		PIO/D1	111	A26	PIO/D1	111
B26		131	B26	PIO/D2	131	B26	PIO/D2	131
C26		132	C26	PIO/D3	132	C26		132
A27			A27	DGND		A27	DGND	
B27		206	B27	PIO	204	B27		199
C27	PIO	207	C27	PIO	205	C27		200
A28	PIO/D4	137		PIO/D4	137	A28	PIO/D4	137

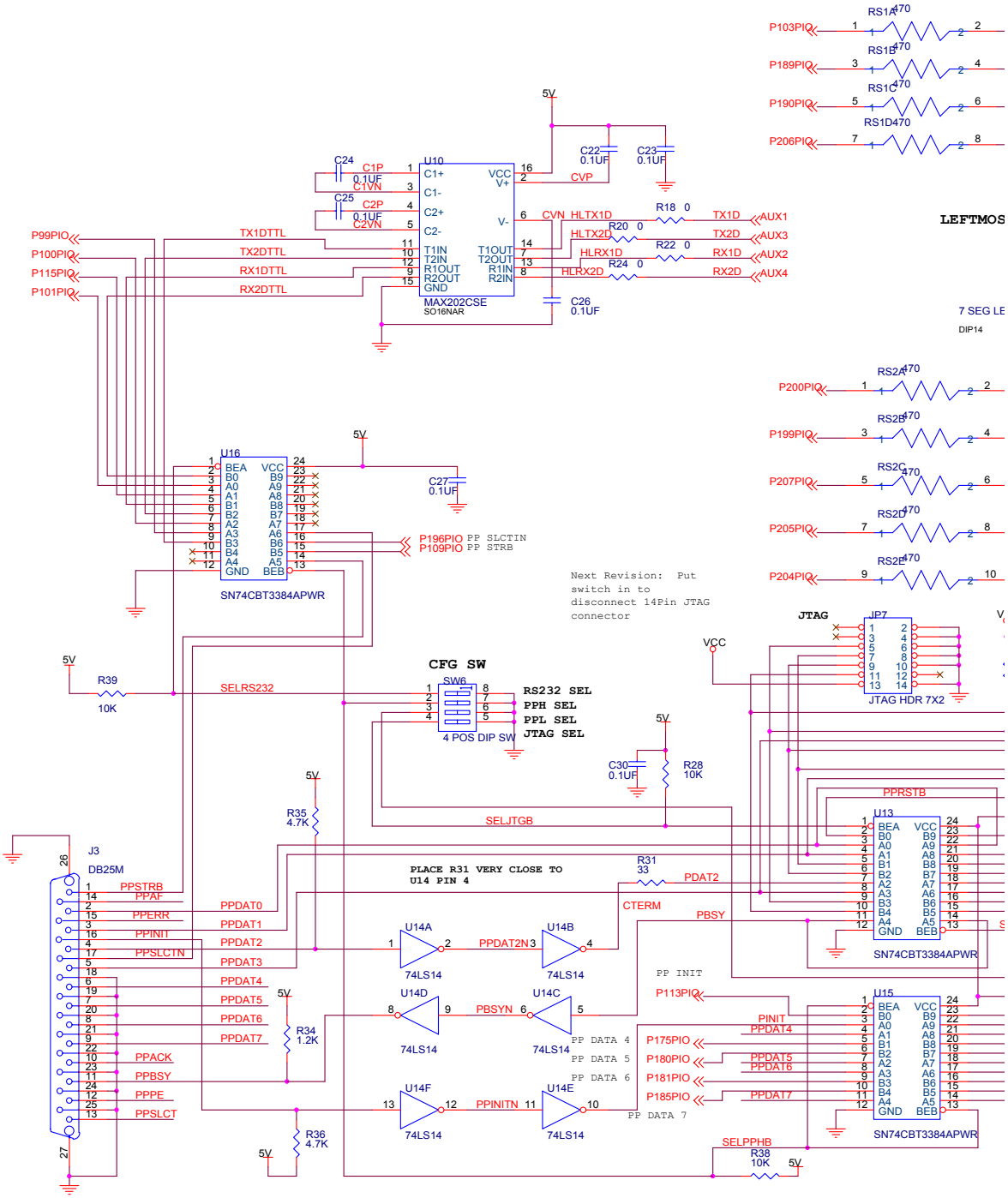
J1			J2			J3		
Pin	Description	TE520	Pin	Description	TE520	Pin	Description	TE520
B28	PIO/D5	138	B28	PIO/D5	138	B28	PIO/D5	138
C28		141	C28	PIO/D6		C28	PIO/D6	141
A29	PIO/D7	142		PIO/D7	142	A29	PIO/D7	142
B29		184	B29	PIO/A11	184	B29	PIO/A11	184
C29		187	C29	PIO/A12	187	C29	PIO/A12	187
	PIO/A13	188	A30	PIO/A13	188	A30	PIO/A13	188
B30	PIO/A14	197	B30		197	B30	PIO/A14	197
C30	PIO/A15	198	C30	PIO/A15	198	C30	PIO/A15	
A31	PIO/A16	202	A31	PIO/A16	202	A31	PIO/A16	
B31	PIO/A17		B31	PIO/A17	203	B31	PIO/A17	203
C31	PIO	98		PIO	96	C31		162
A32	PIO/A18	8	A32		8	A32	PIO/A18	8
	DGND		B32			B32	DGND	
C32		93	C32	PIO/UCLK	93	C32		93

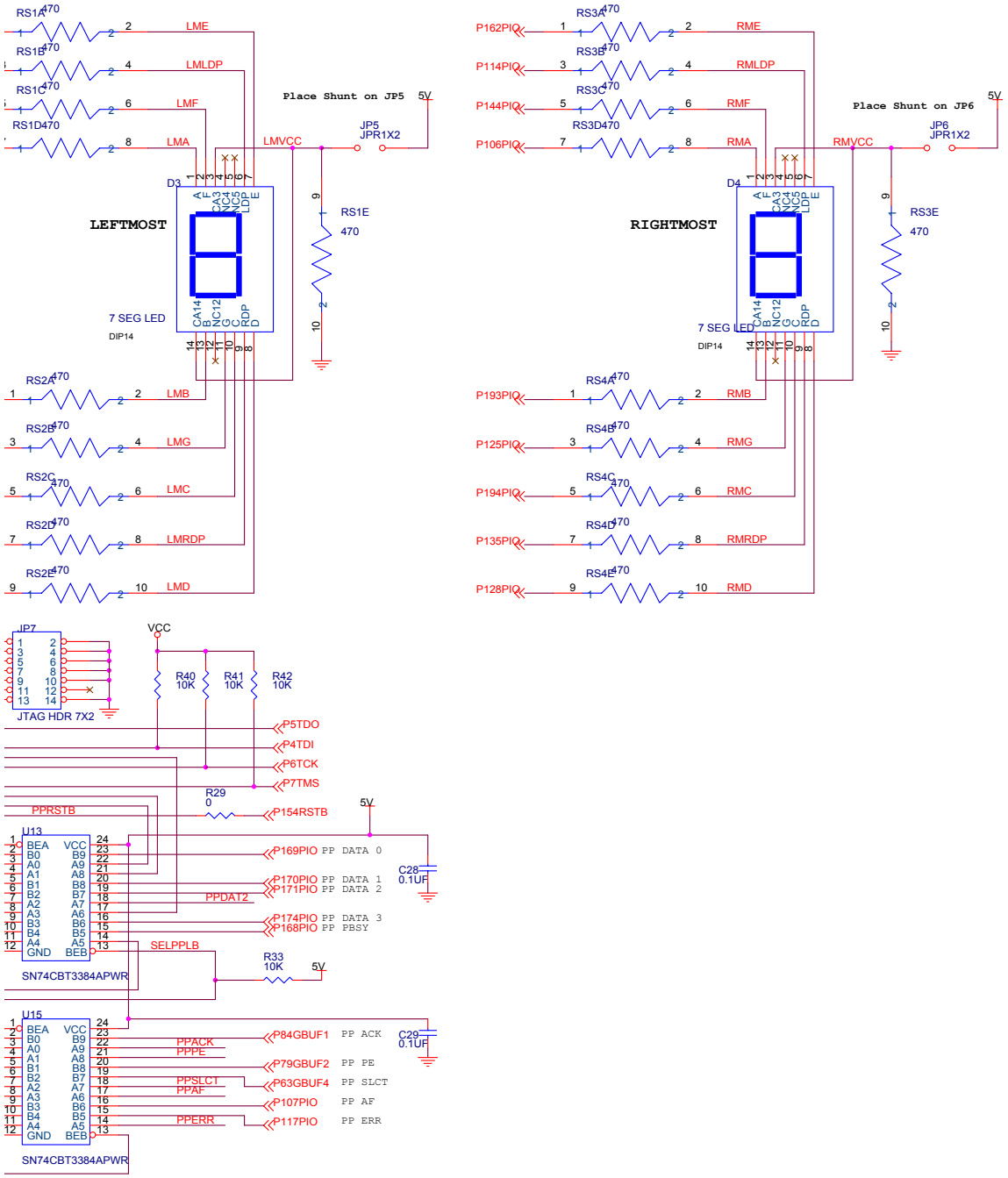
E5 Evaluation Board Schematic




LOAD R1
OR R2 BUT
NOT BOTH
Mount C3 very
close to U5
pin 8
Keep lead length less than
1.5" and R5 very close to
U5 pin 5
MOUNT FLASH
PART U2
ONLY
1M or 2M
DO NOT LOAD
ZERO OHM
RESISTOR
R12
DO NOT LOAD
SERIAL FLASH U7
XC1701LPD8C
PBUT2
PBUT1
SW-MOM-SPST_NO
REQUIRES E5XX PULLUPS
USR SW
8 POS DIP SW
REQUIRES E5XX PULLUPS
TE520S40
SQFP208
THESE (12) 0.1UF CAPS GO CLOSE TO
THE TE520 DEVICE VCC'S, 3 CAPS TO
A SIDE
TIE EACH CAPACITOR TO THE GROUND
AND VCC PLANES DIRECTLY ... NO
DAISY CHAINS!
Evaluation E520 Module
iPS-EVALE520dm
Saturday, September 29, 2005

(Evaluation Board, Page 2)

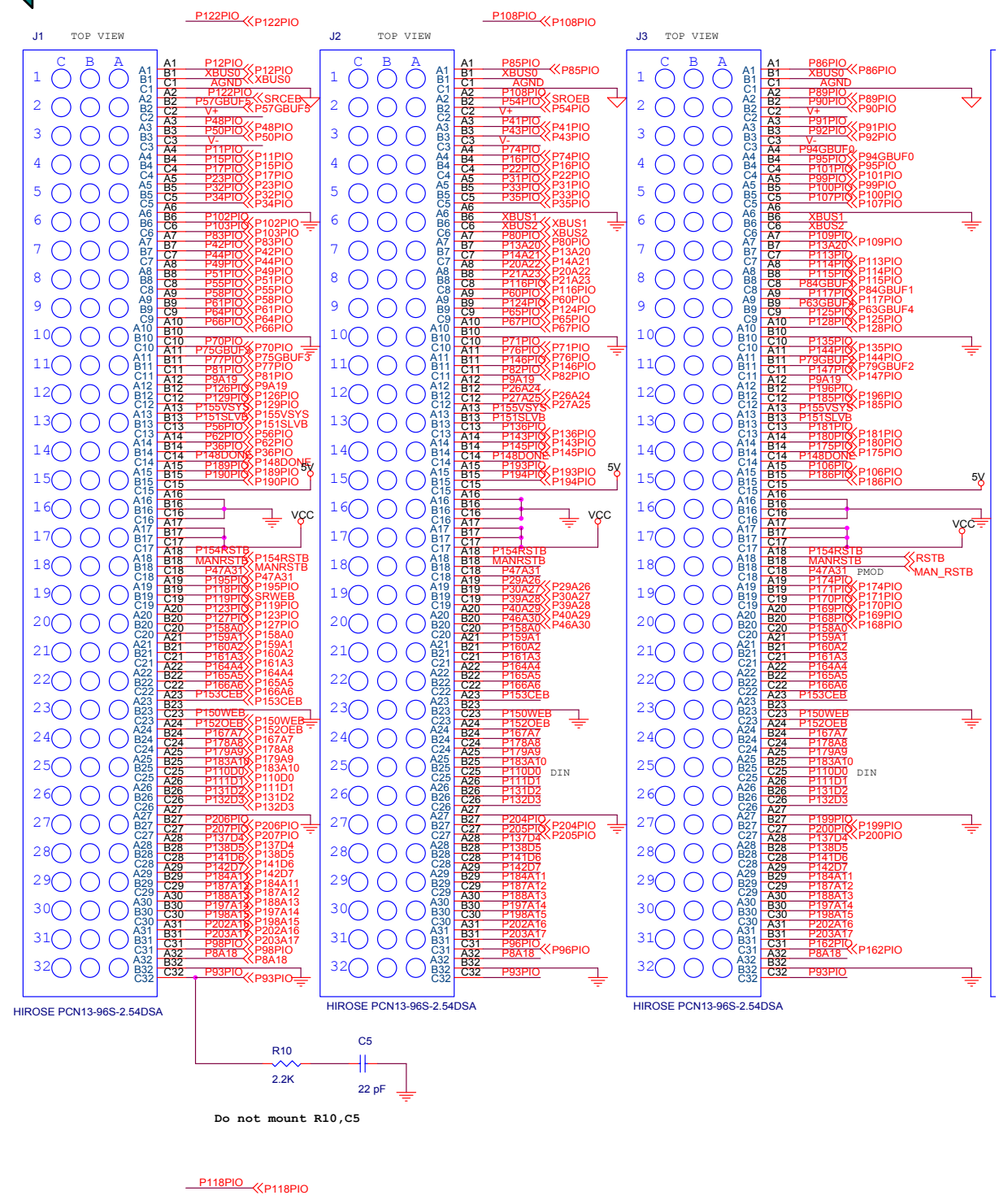




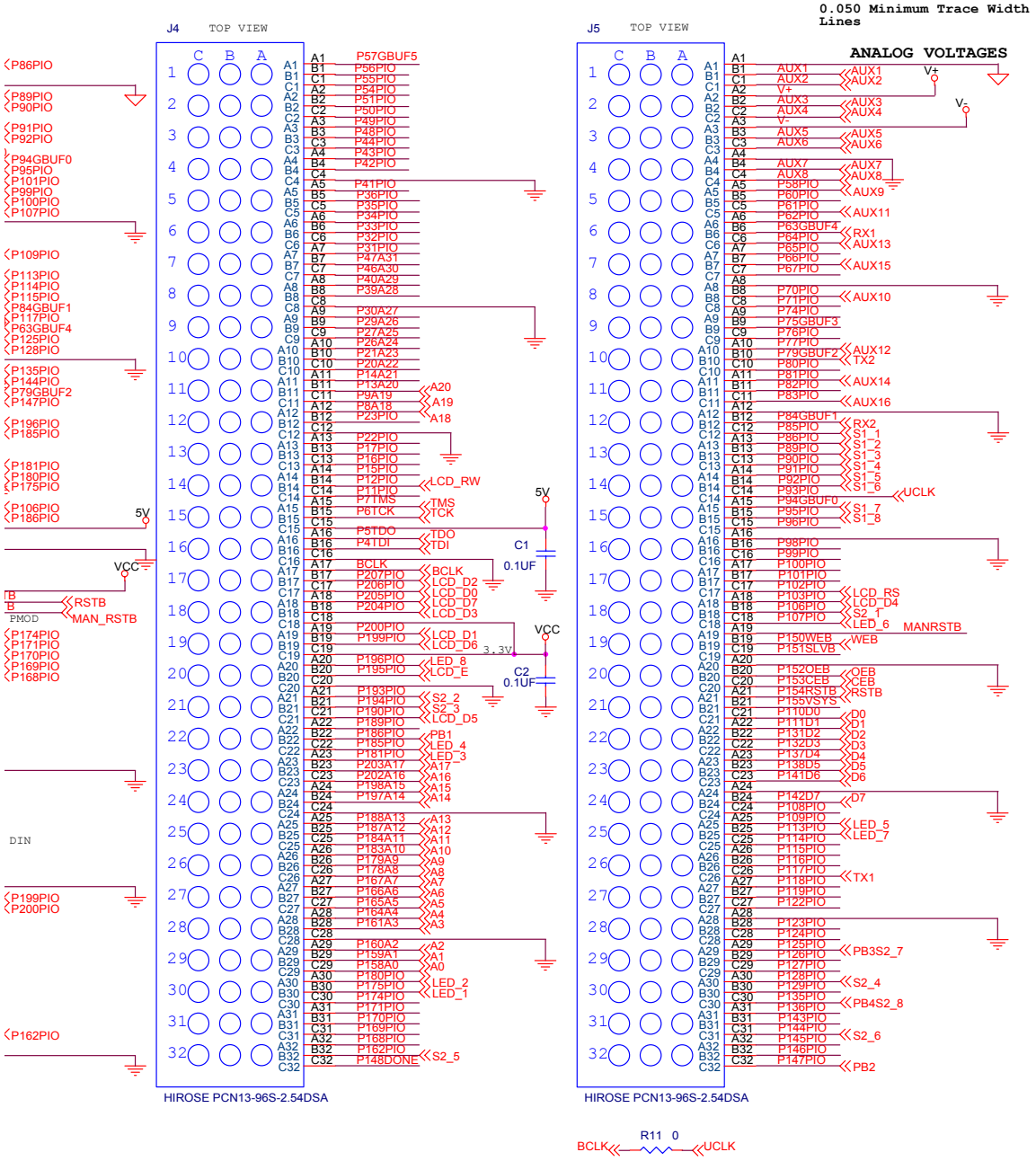
Title: Evaluation E520 Module: MISC		
Size: C	Document Number: iPS-EVALE520dm	Rev: 1.10
Date: Saturday, September 29, 2005	Sheet 1 of 2	

Base Board Schematic

Expansion Slots J1-J3



Processor Module Slots J4-J5

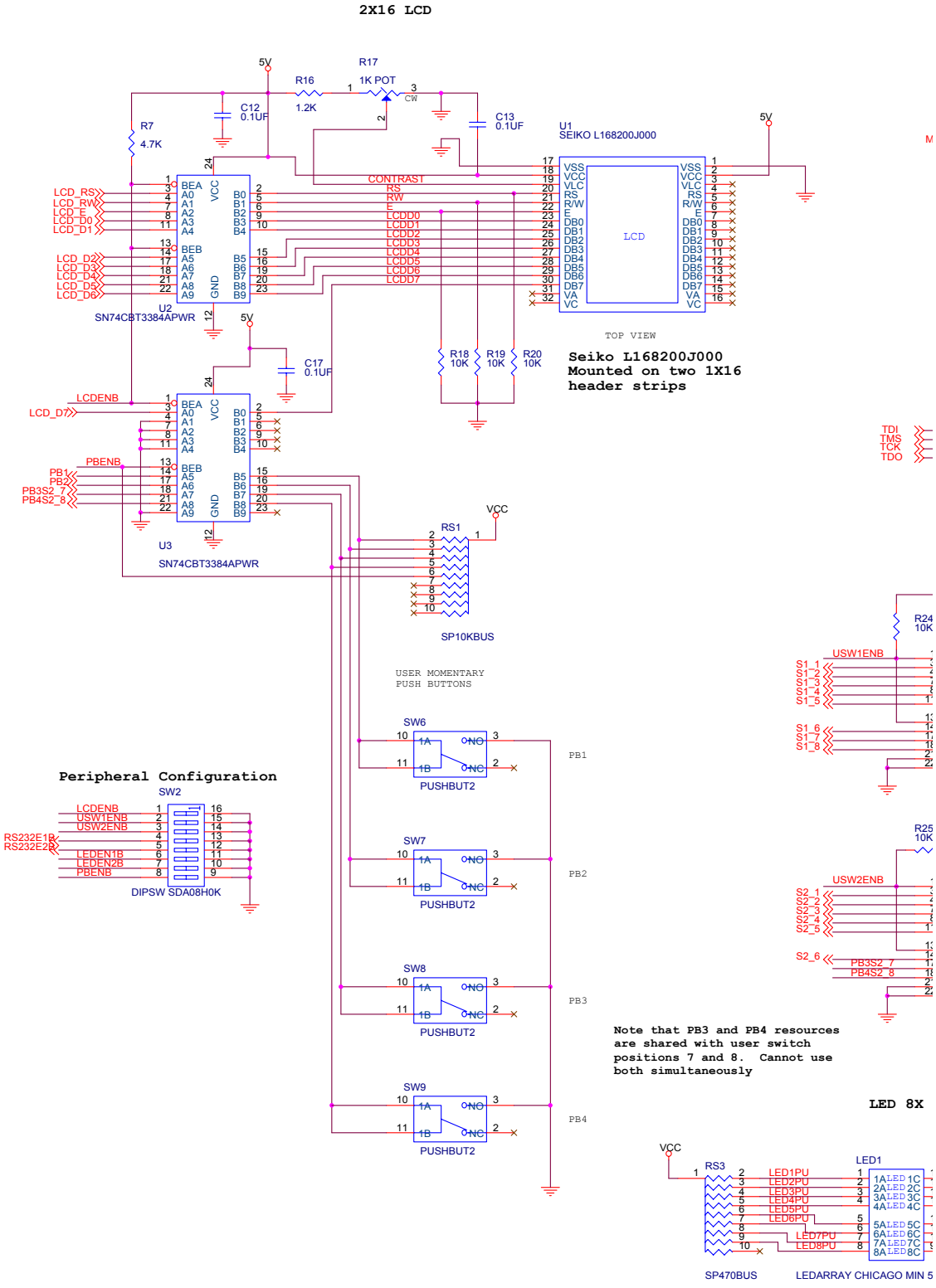


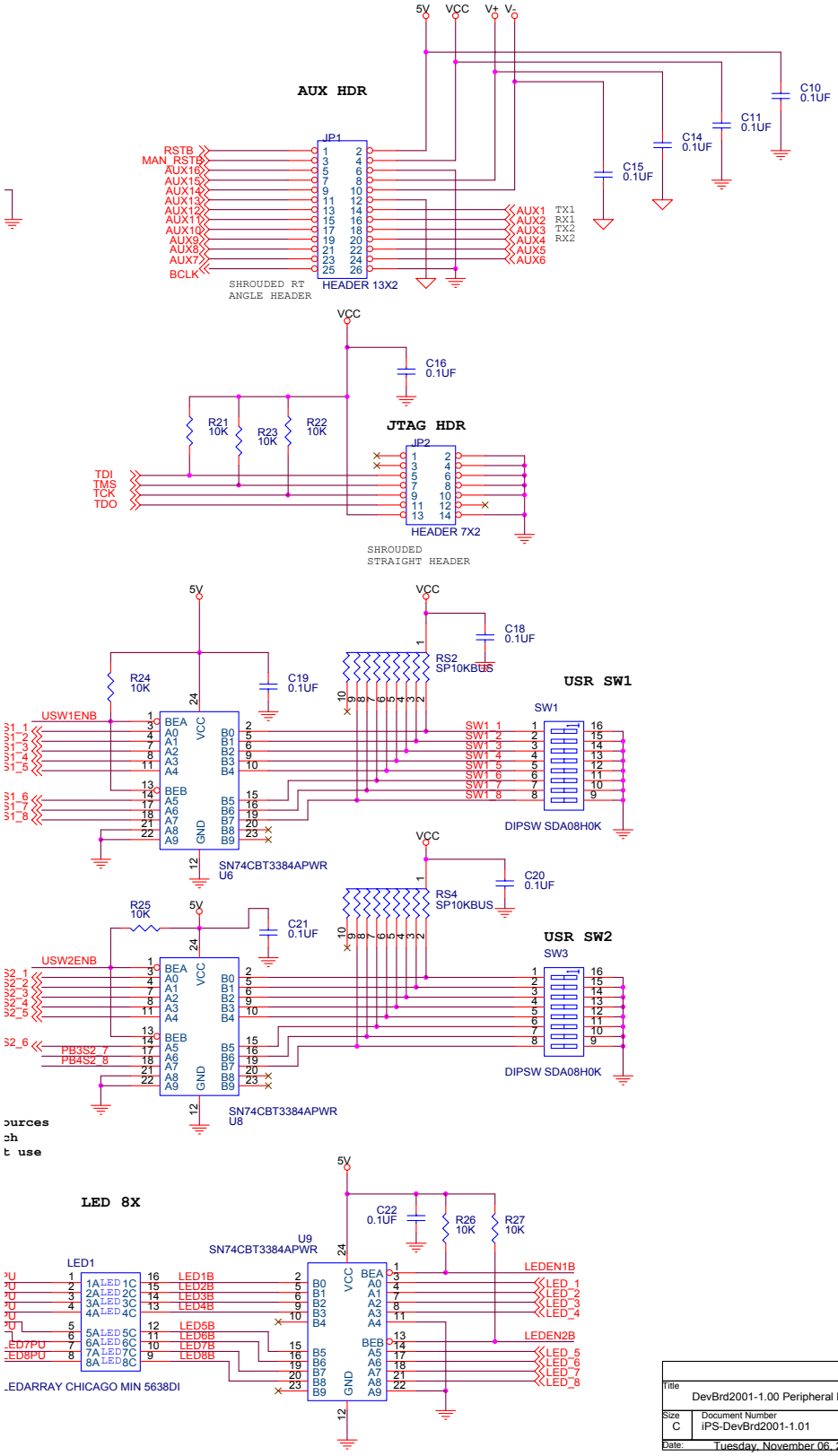
Three Planes:

1. **VCC (3.3V)**
2. **+5**
3. **GND**

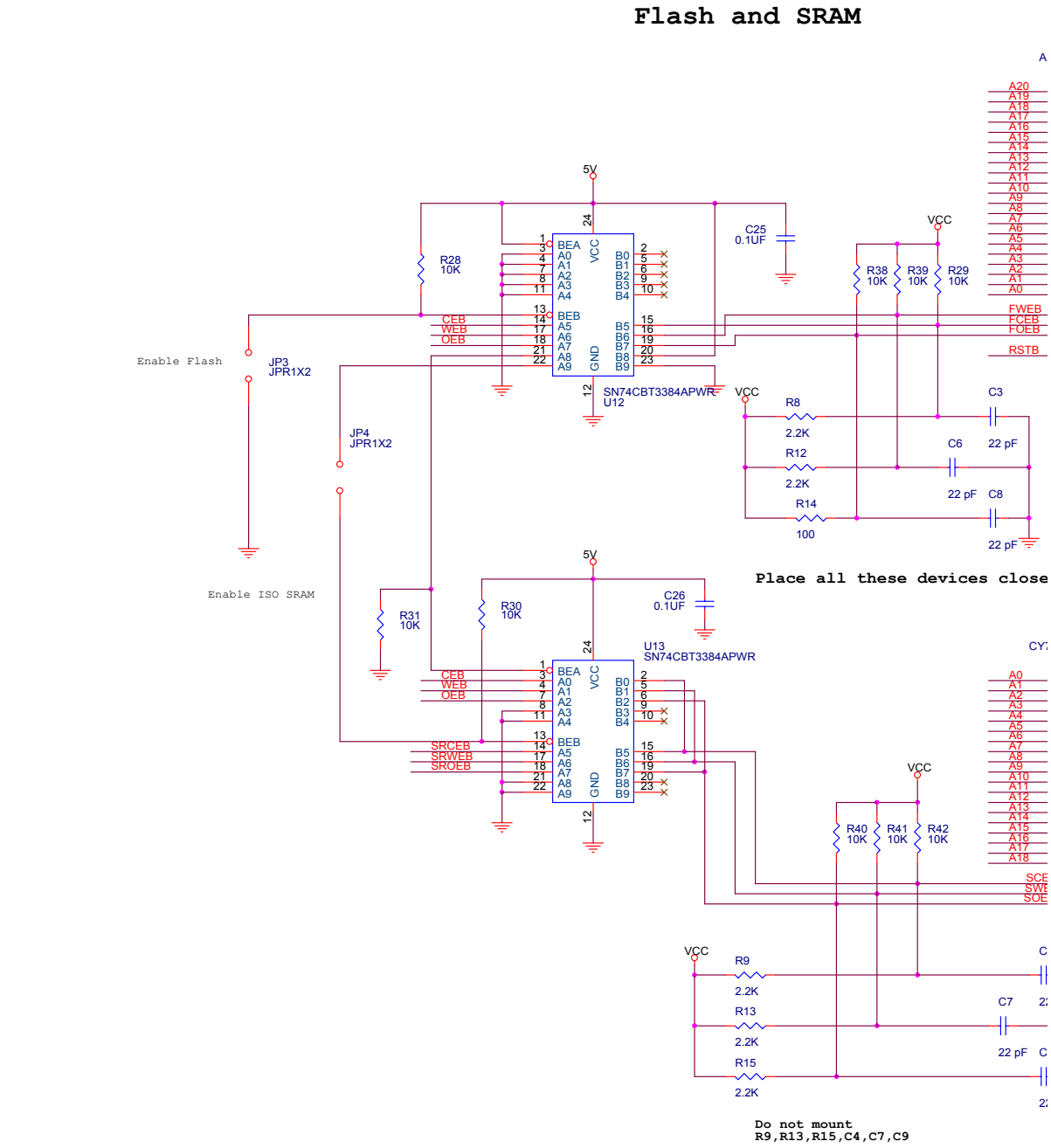
Title: DevBrd2001 Expansion and Processor Connectors		
Size: C	Document Number: iPS-DevBrd2001-1.02	Rev: 1.02
Date: Tuesday, November 06, 2001	Sheet 1 of 7	

(Base Board, Page 2)

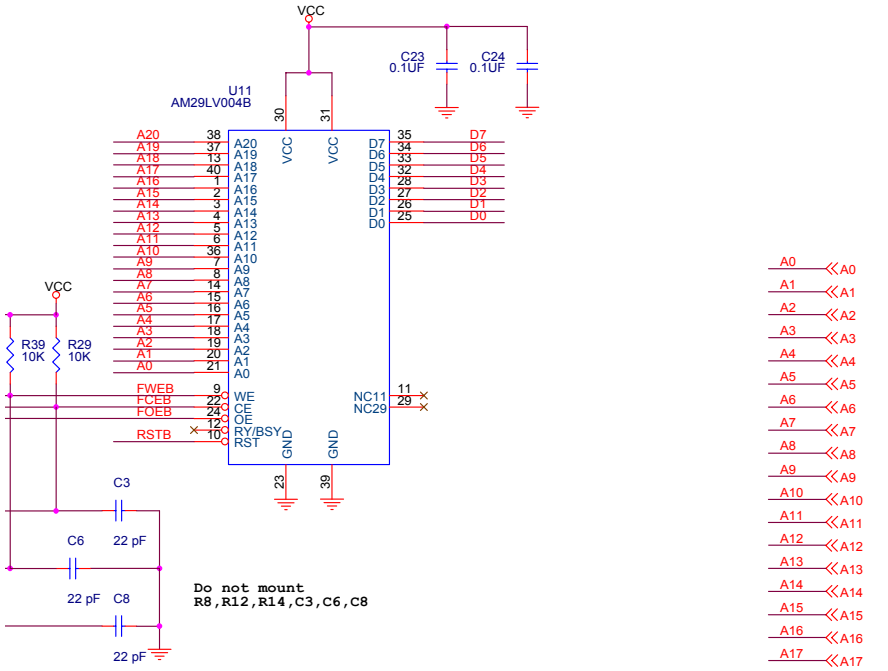



AUX HDR
JP1
HEADER 13X2
SHROUDED RT ANGLE HEADER
JTAG HDR
JP2
HEADER 7X2
SHROUDED STRAIGHT HEADER
USR SW1
SW1
DIPSW SDA08H0K
SN74CBT3384APWR
U6
USR SW2
SW3
DIPSW SDA08H0K
SN74CBT3384APWR
U8
LED 8X
U9
SN74CBT3384APWR
LED1
EDARRAY CHICAGO MIN 5638DI
DevBrd2001-1.00 Peripheral Logic
iPS-DevBrd2001-1.01
Tuesday, November 06, 2001
Sheet 2 of 7

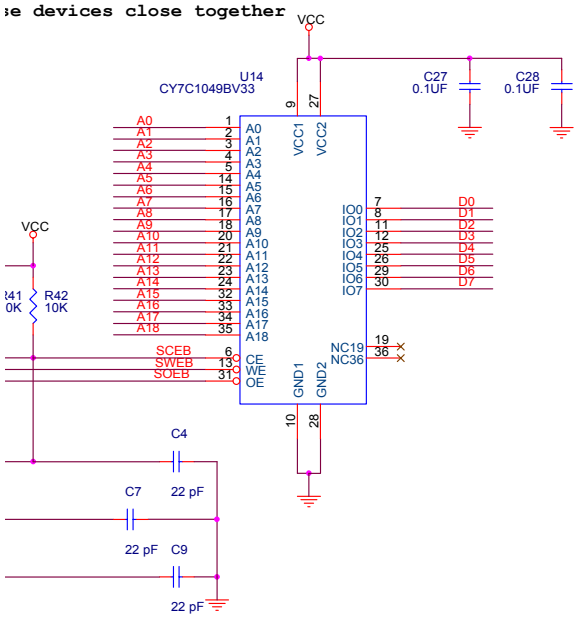
(Base Board, Page 3)

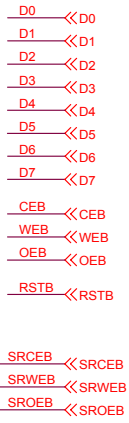


JP4	JP3	Function
X	OFF	DOWNLOAD TO SRAM, FLASH DISABLED
OFF	ON	DOWNLOAD TO FLASH, SRAM DISABLED
X	OFF	DOWNLOAD TO SRAM, FLASH DISABLED
ON	ON	ISO SRAM, DOWNLOAD TO FLASH



ɜe devices close together

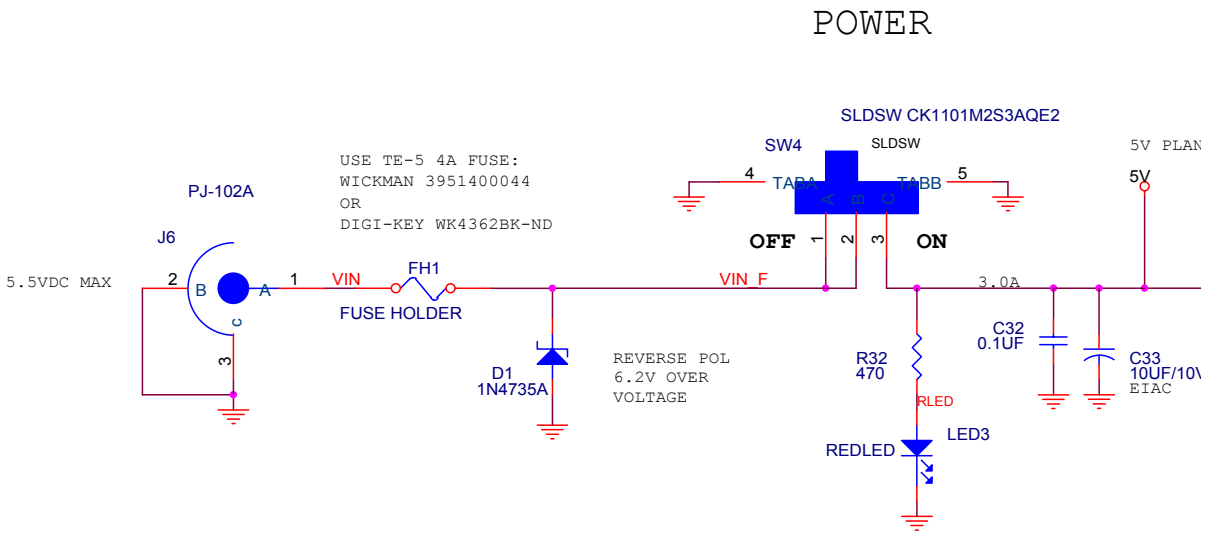


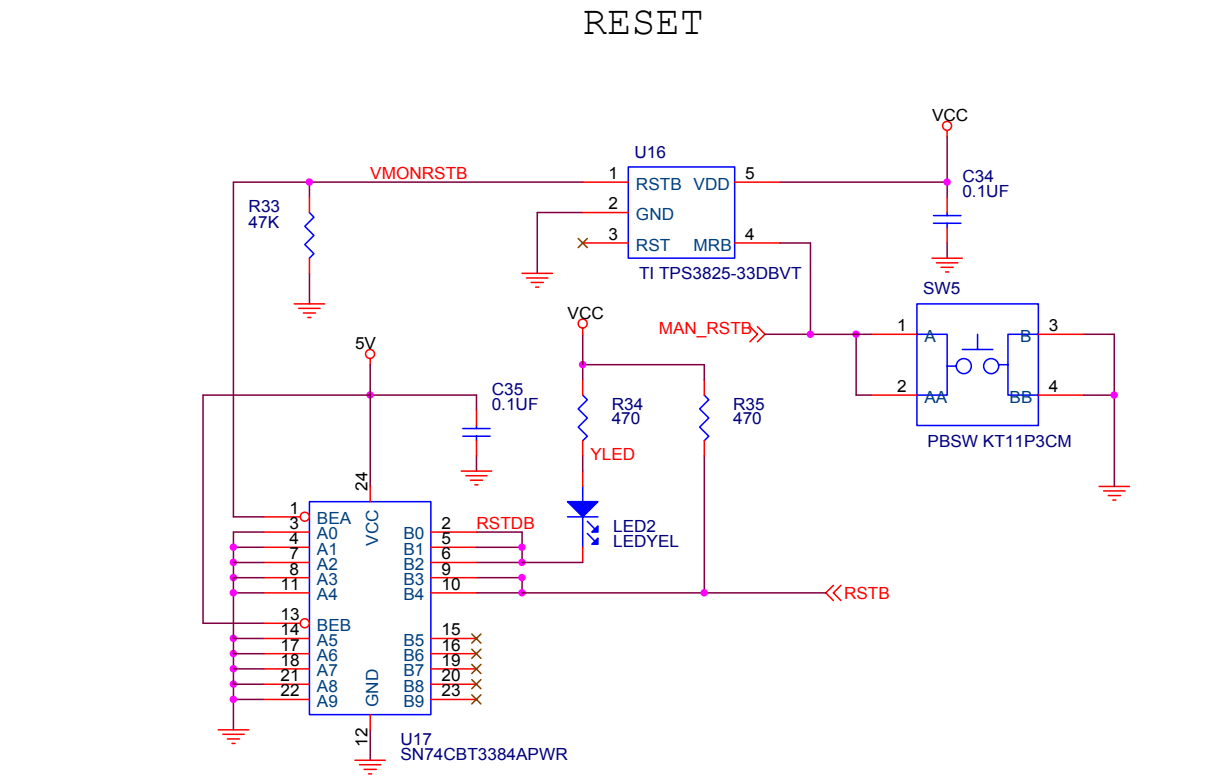


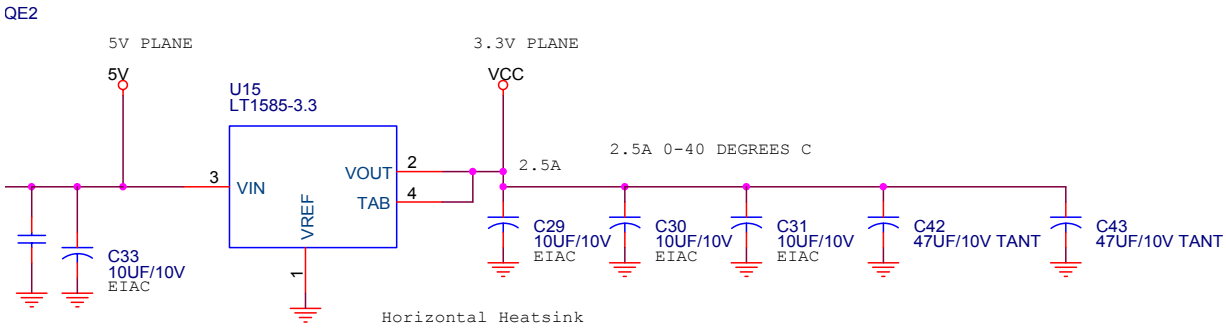
C9

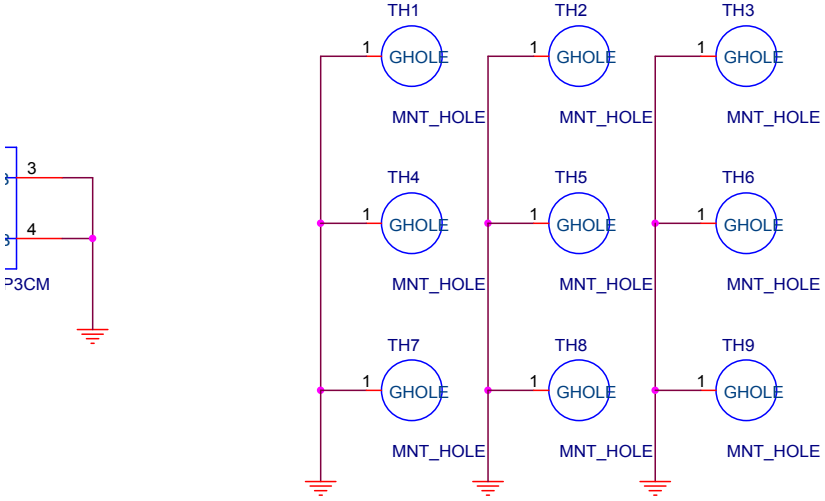
Title	DevBrd2001 SRAM and FLASH	
Size C	Document Number DevBrd2001-1.01	Rev 1.01
Date: Tuesday, November 06, 2001	Sheet 3 of 7	

(Base Board, Page 4)



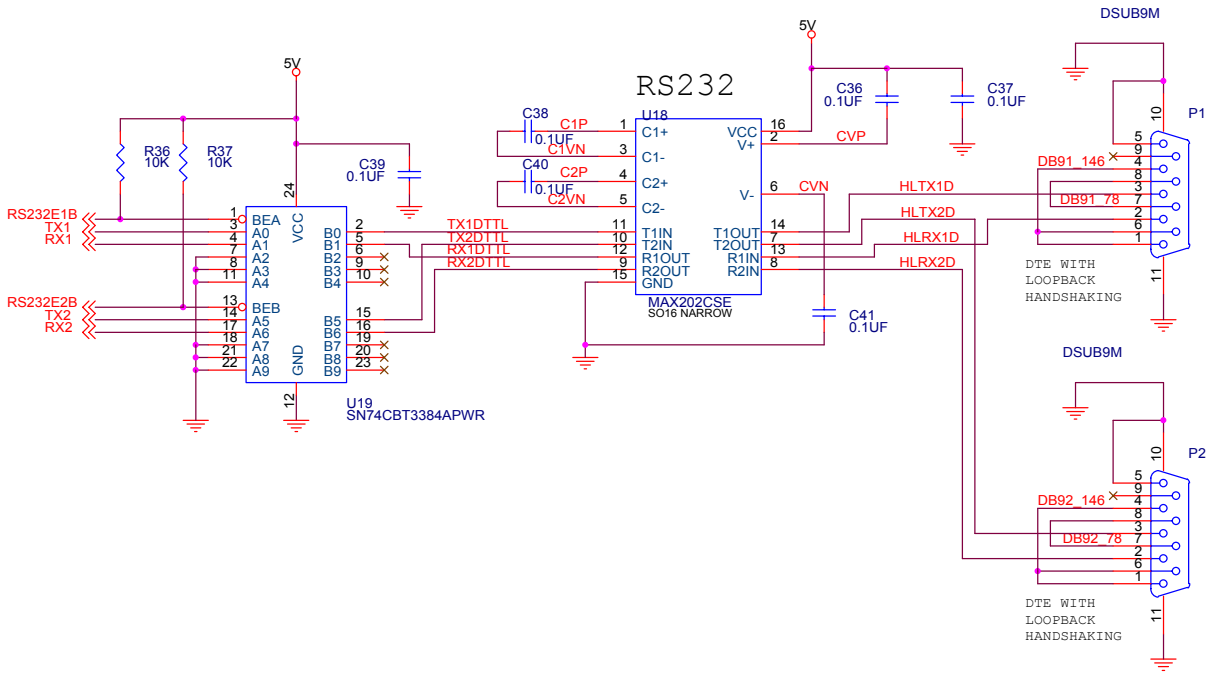



QE2
5V PLANE
3.3V PLANE
5V
VCC
U15
LT1585-3.3
VIN
VOUT
TAB
VREF
3
2
4
1
2.5A
2.5A 0-40 DEGREES C
C33
10UF/10V
EIAC
C29
10UF/10V
EIAC
C30
10UF/10V
EIAC
C31
10UF/10V
EIAC
C42
47UF/10V TANT
C43
47UF/10V TANT
Horizontal Heatsink

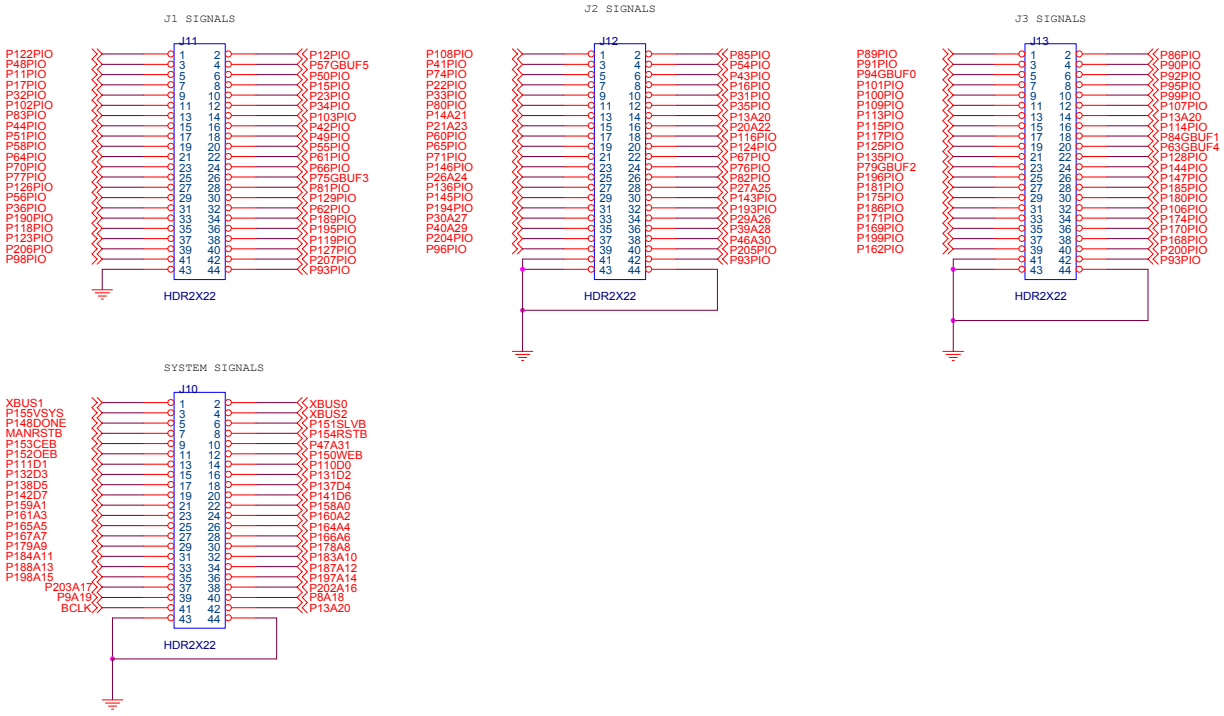

TH1
TH2
TH3
TH4
TH5
TH6
TH7
TH8
TH9
GHOLE
MNT_HOLE
1
3
4
P3CM

(Base Board, Page 5)

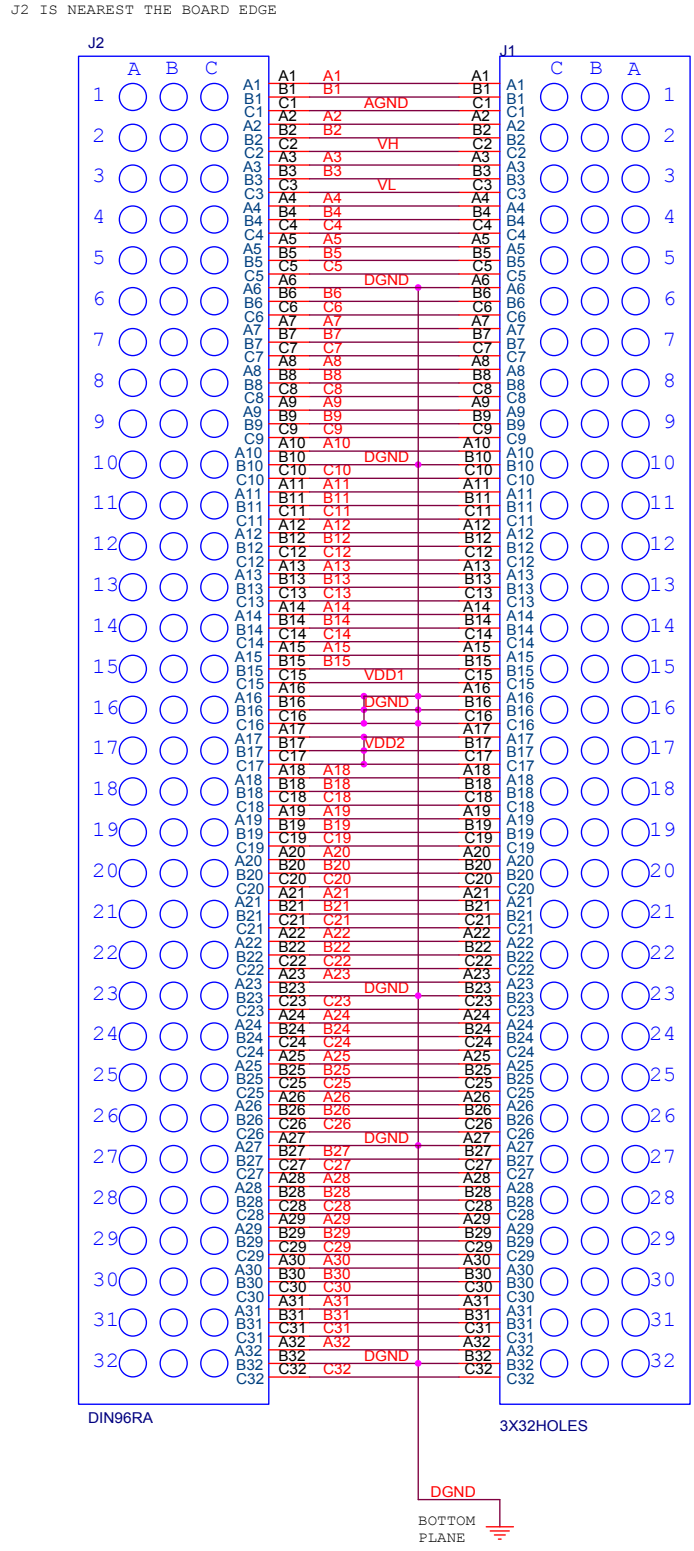
RS232

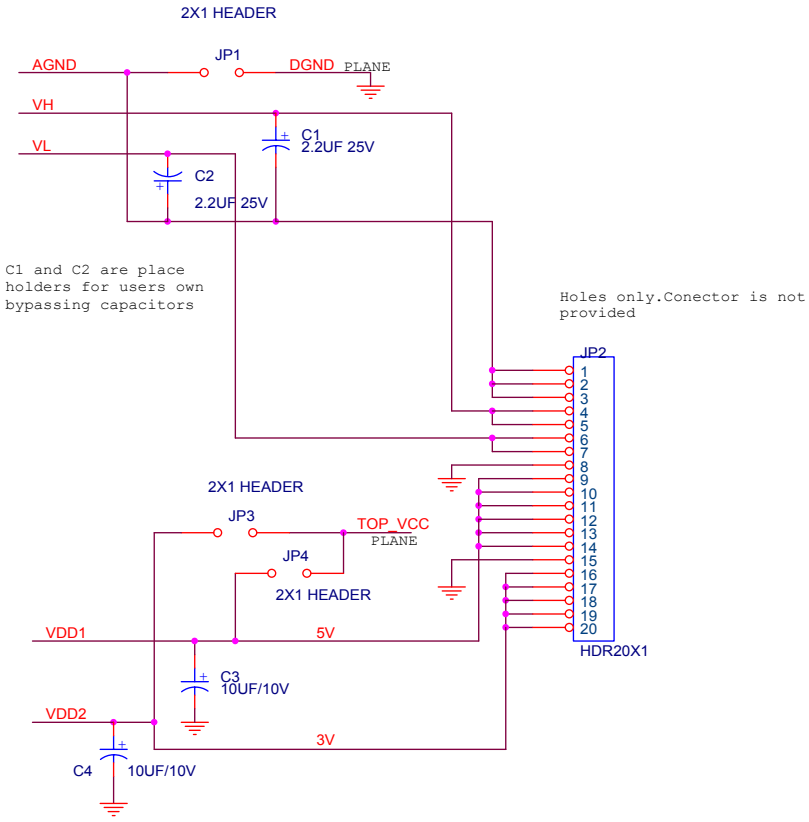


(Base Board, Page 6)



Prototype Card Schematic

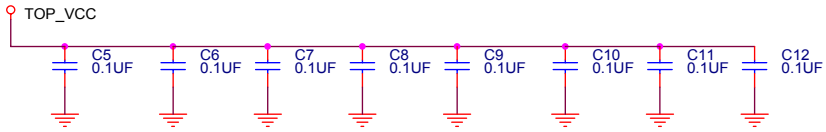




THIS IS A TWO LAYER BOARD WITH DGND
AS THE BOTTOM PLANE. THE TOP_VCC PLANE IS
DETERMINED BY WHICH JUMPER IS STRAPPED,
VDD1 OR VDD2.

TOP_VCC — TOP SEA OF HOLES PLANE
(0.1" spacing)

DGND — BOTTOM SEA OF HOLES PLANE
(0.1" spacing)



Revision History

Revision	Date	Comment
1.00	11-NOV-2001	Initial release.

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Tel: 1-650-968-8668 Fax: 1-650-934-9393 Web: www.triscend.com