FastChip 2.1.2 and the A7 CSoC Family

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Agenda

- Install A7 Development Environment
- FastChip Licensing
- Building an A7 Project with FastChip
  - Whirlwind tour with a few stops at points of interest
    - Address allocation
    - Timing-driven Bind

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System Requirements

- Pentium-class processor
- Windows 98, 2000, ME, and NT
  - Non-U.S. versions require international FastChip
  - No Windows 95 support
- 192 MB of RAM
  - Highly, high recommend 256 MB
  - FastChip, FDL both use 128 MB with virtual machine

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System Requirements (cont'd)

- Internet Explorer 5.0 or later
- HTML Help 1.21
- Adobe Acrobat 3.01 or later
- Optional Cygwin Make utilities for command-line automation
- Available in /ThirdParty directory on CD-ROM

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What's In the Box?

- FastChip 2.1.2 CD-ROM
- visionPROBE II JTAG download/debug cable
- visionCLICK CD-ROM
  - Version 7.6A with patch today
  - Version 7.7 at production
- WindRiver Diab Compiler CD-ROM

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Installation Logistics

- Use Diab and visionCLICK CD-ROMs from the A7 Starter Kit box
- Use FastChip CD-ROM hand-out
- **WARNING!** Your virus checker may flag *.tar and *.gzip files

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Installing FastChip 2.1.2

- Plug it in and it works!
- Be sure to update the Keil DLLs in you use the E5 CSoC Family
- FastChip Device Link (FDL) utility can be installed as a stand-alone application

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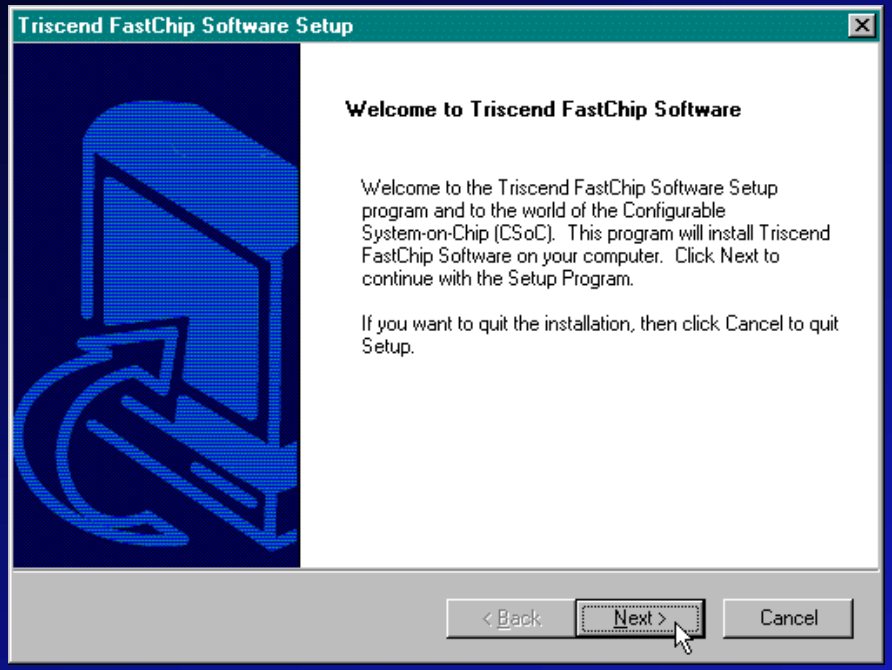
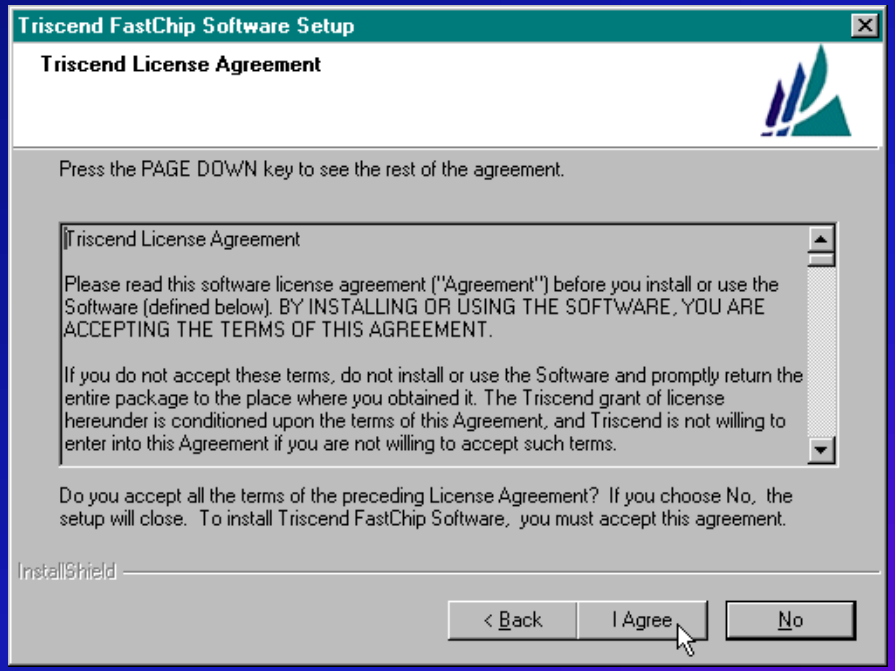
Installing FastChip 2.1.2 (a)



Read welcome. Click **Next >**.



Read license. Click **I Agree**.

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Start with a Clean Slate

- FC 2.1.1, rename the FastChip directory
  - Keep it around for customer support reasons
- Uninstall Diab, visionCLICK
- Delete **`/diab`** and **`/Estii`** directories

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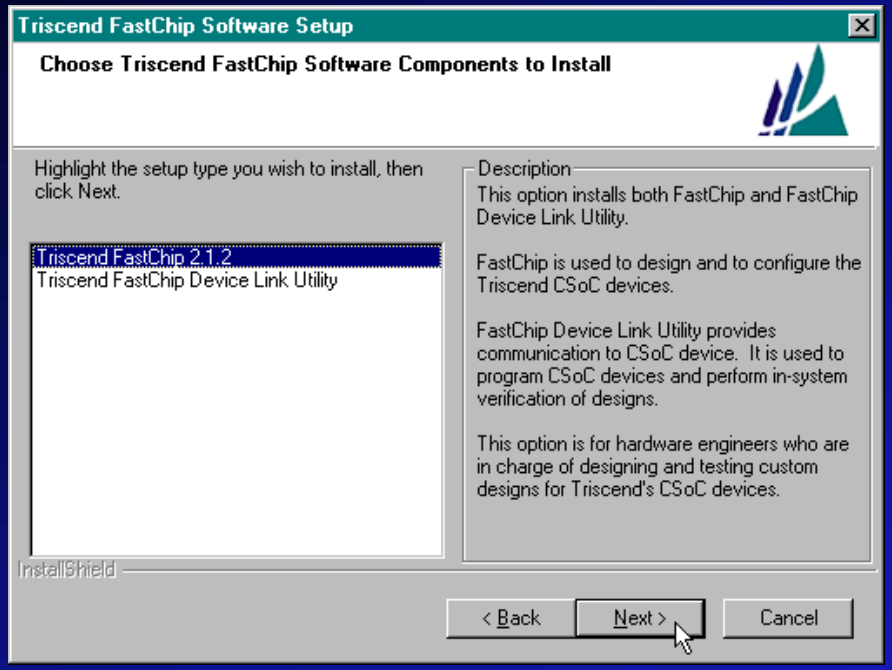
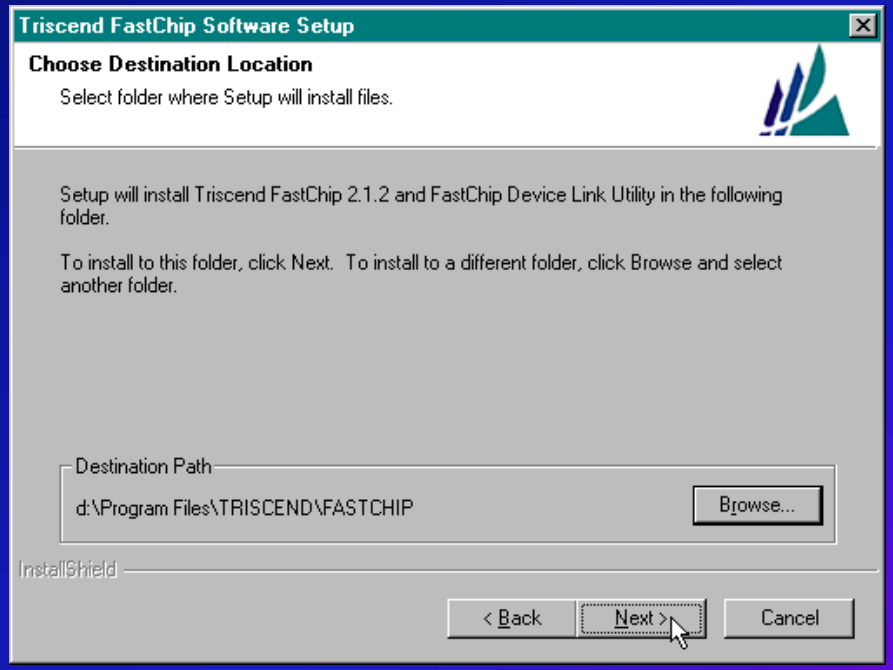
Installing FastChip 2.1.2 (b)





Installing FastChip 2.1.2 also installs FastChip Device Link. Click **Next >**.

Choose installation drive and directory. Click **Next >**.

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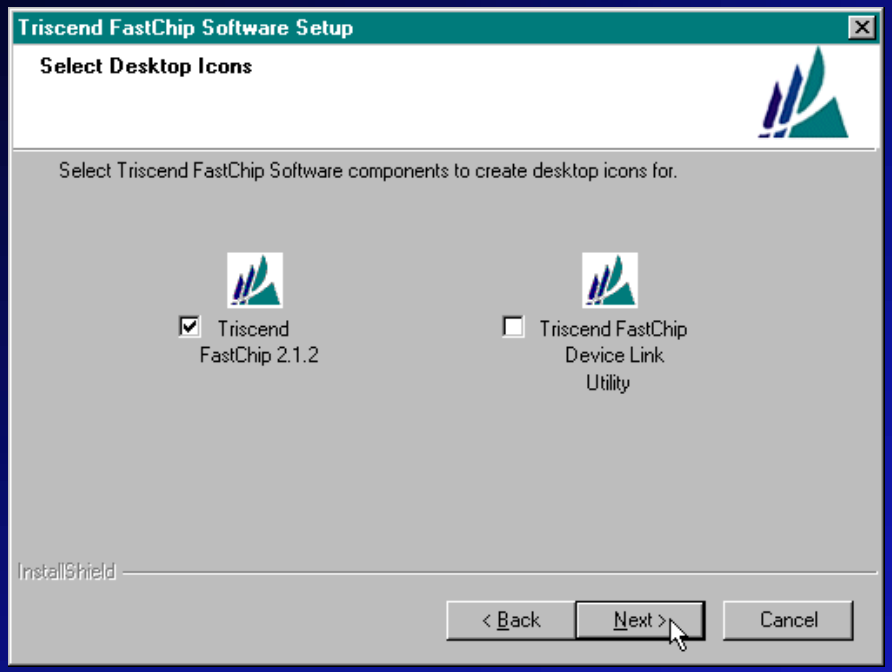
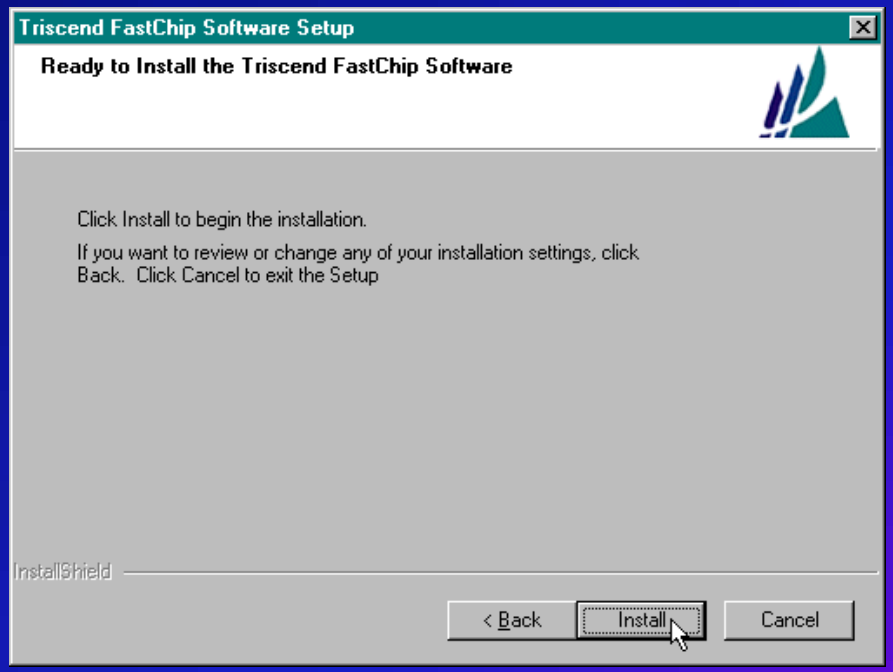
Installing FastChip 2.1.2 (c)



Select desktop icons, if any. Click **Next >**.



Ready to install. Click **Install**.

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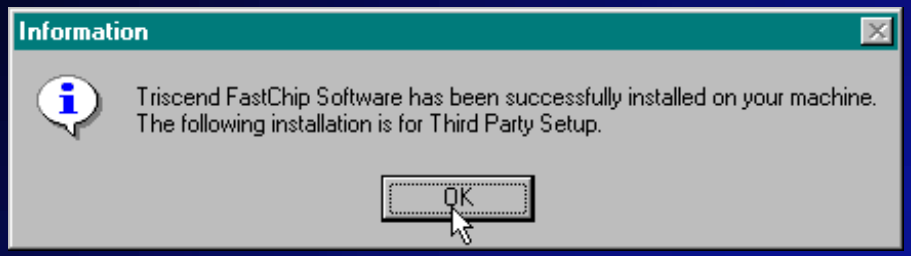
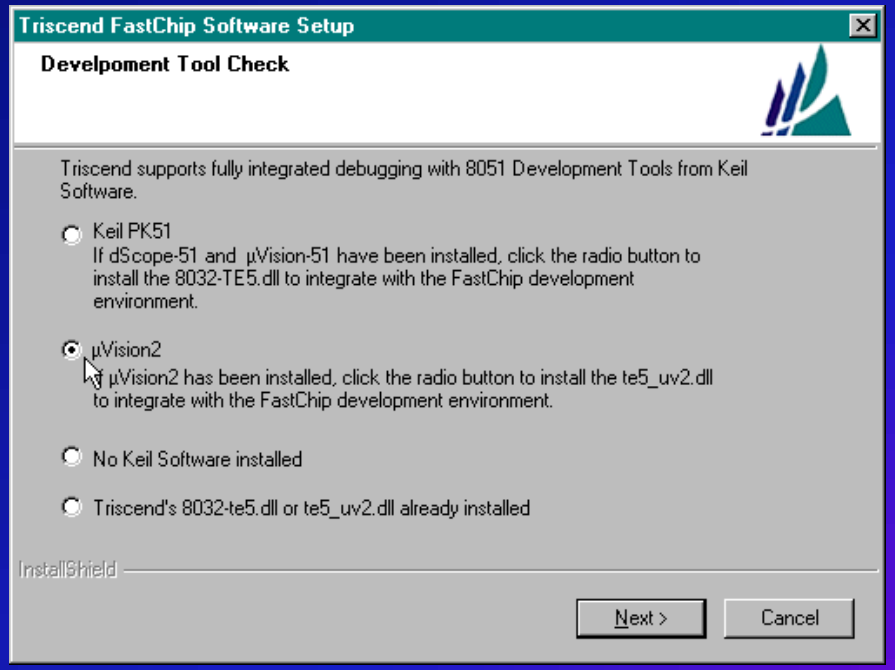
Installing FastChip 2.1.2 (d)





FastChip installation complete! Click **OK** to install third-party support software.

No A7-specific options. Be sure to install Keil DLLs if using E5. Click **Next >**.

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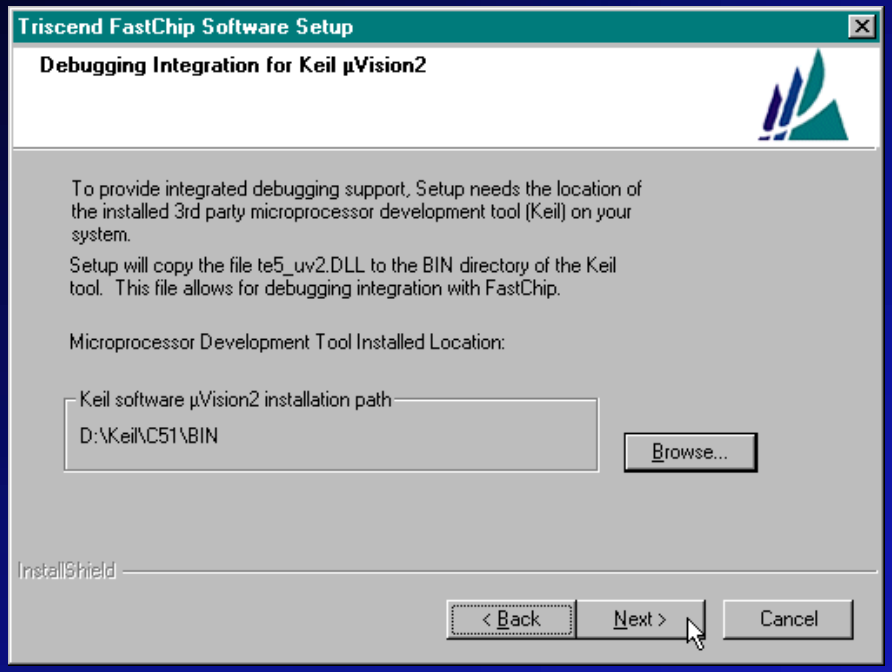
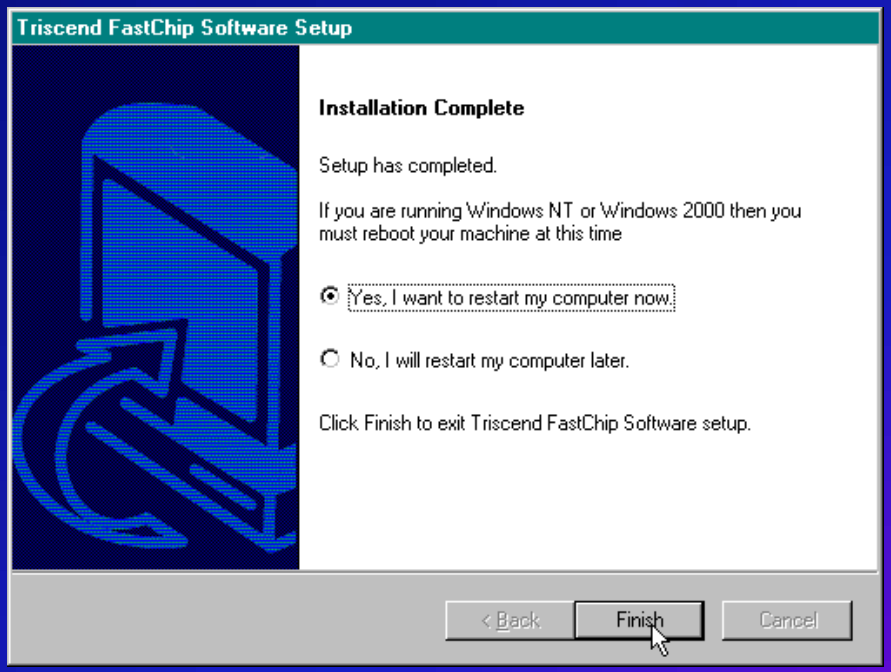
Installing FastChip 2.1.2 (e)





Locate the proper installation directory based on your previous selections. Click **Next >**.

Third-party installation complete. Reboot before using FastChip. Click **Finish**.

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Installing visionCLICK

- visionCLICK software required to use visionPROBE II cable
- Probably the most difficult part of installation

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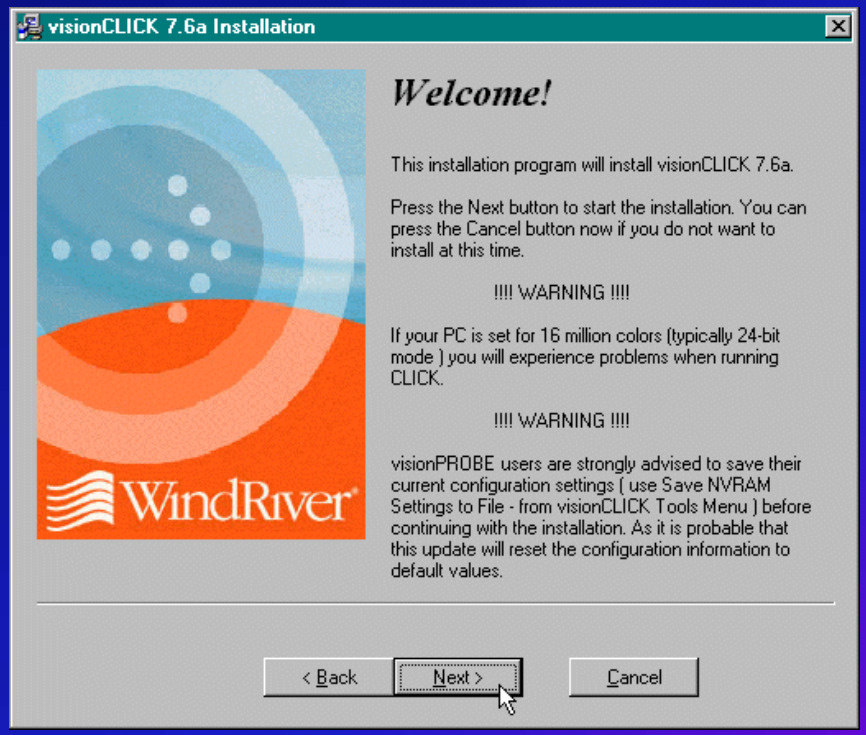
Installing visionCLICK (a)

If CD-ROM auto-runs, visionCLICK displays startup screen. Click **Install visionCLICK**.



Read important welcome screen. Click **Next >**.

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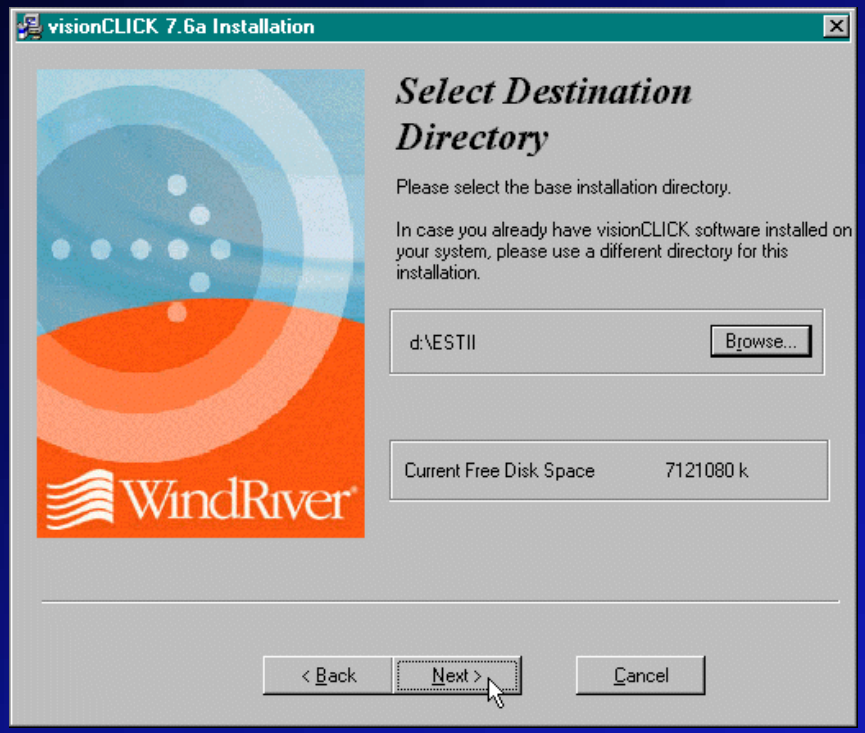
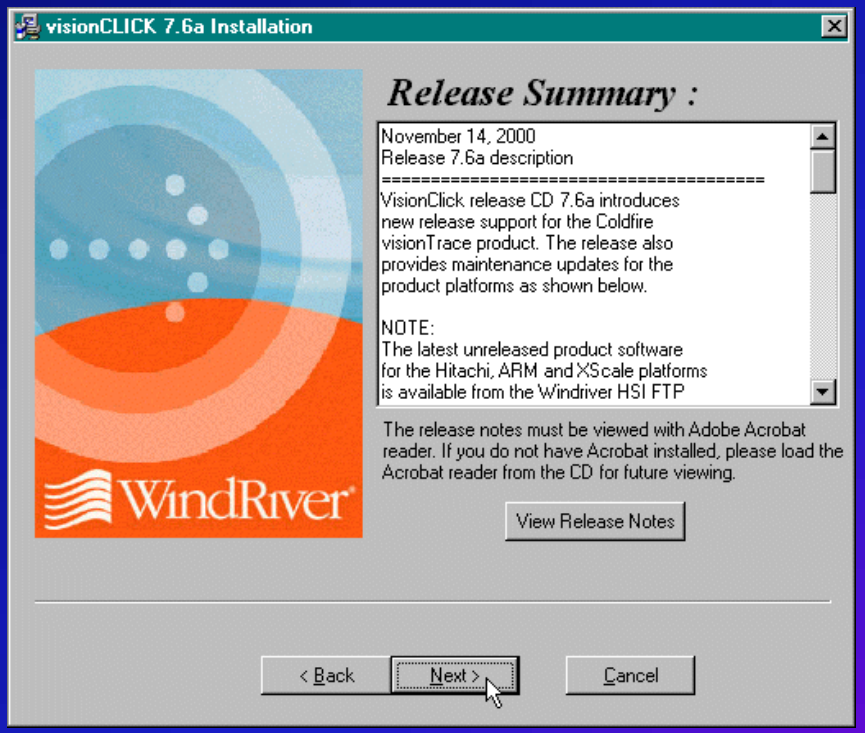
Installing visionCLICK (b)



Select installation directory.
Click **Next >**.



Scroll through release notes.
Click **Next >**.

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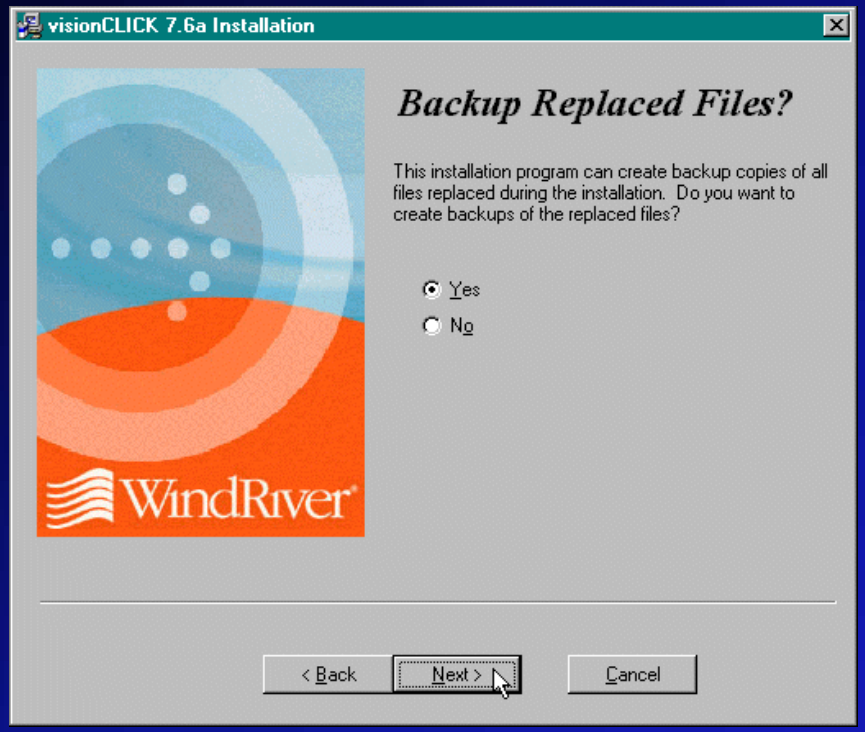
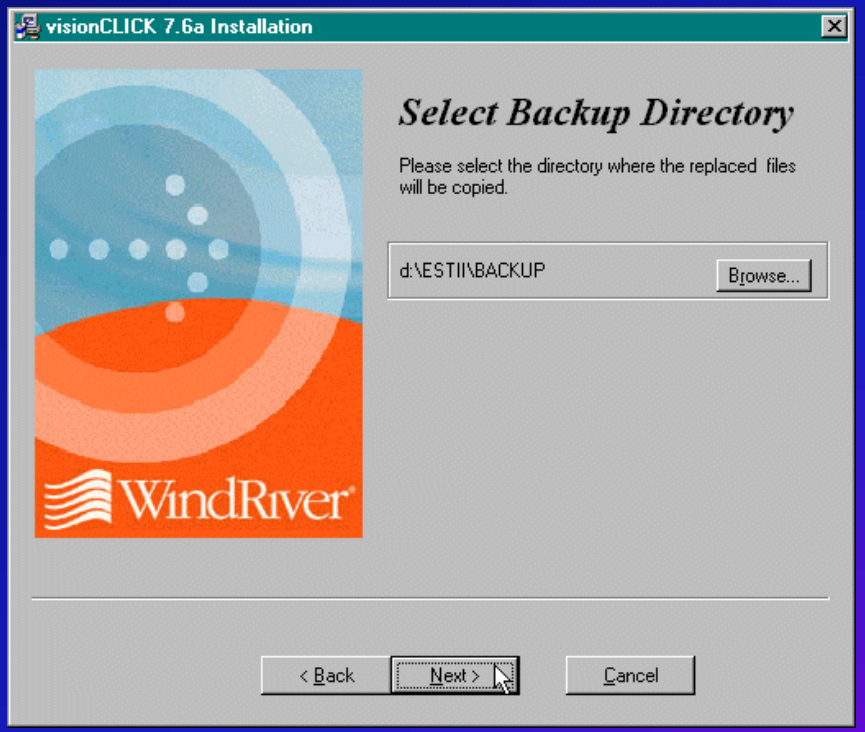
Installing visionCLICK (c)



If installing visionCLICK for the first time, select No backup. Click **Next >**.



If updating visionClick, select backup directory. Click **Next >**.

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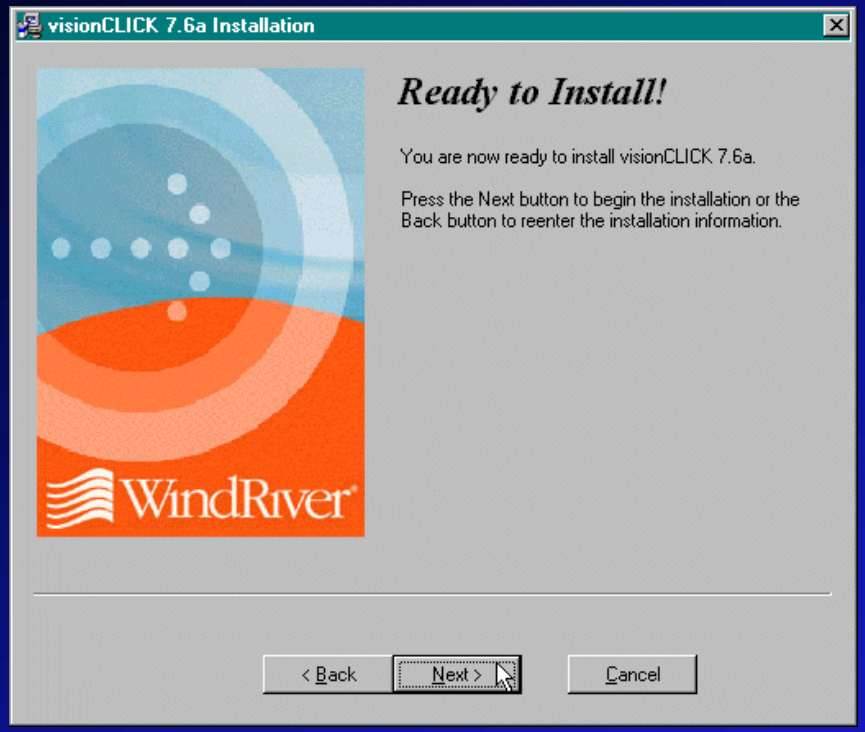
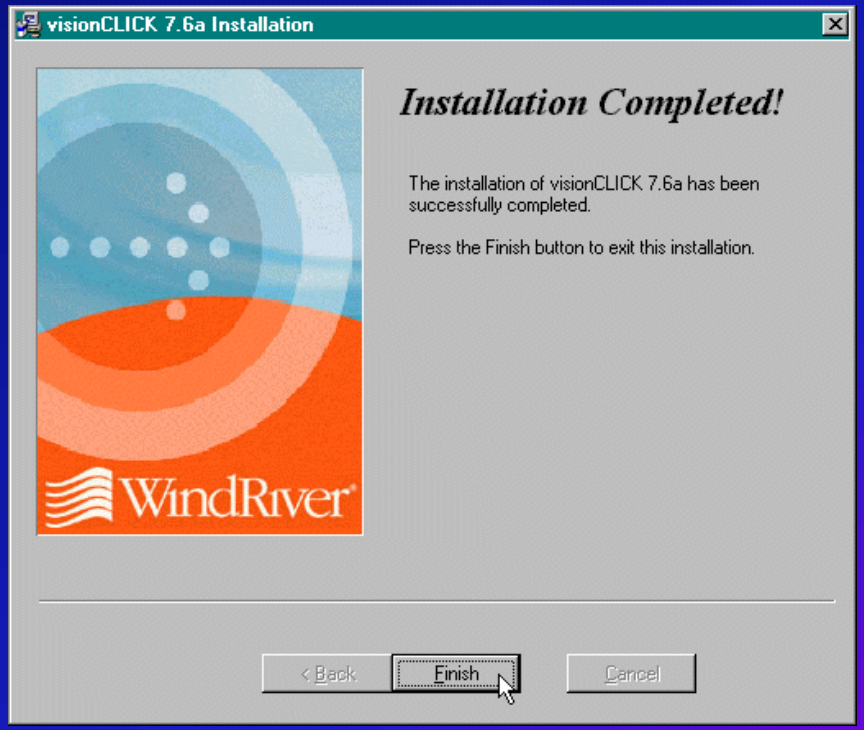
Installing visionCLICK (d)



Ready to install. Click **Next >**.



Installation complete. Click **Finish**.

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Installing visionCLICK (e)

From the visionCLICK startup screen, click **Exit**.

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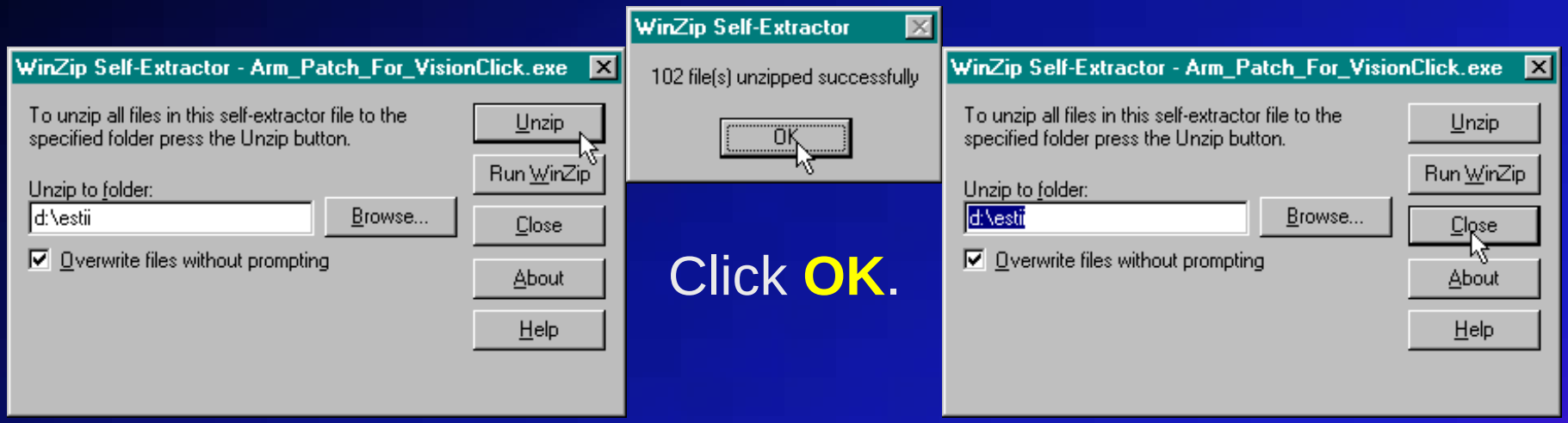
Install visionCLICK Patch



This step not required for FastChip 2.1.2 production release. Overwrite with visionCLICK update, Arm_Patch_For_VisionClick.exe

Click **Unzip**.

Click **OK**.

Click **Close**.

This step updates visionCLICK to support the ARM7 and Triscend A7.

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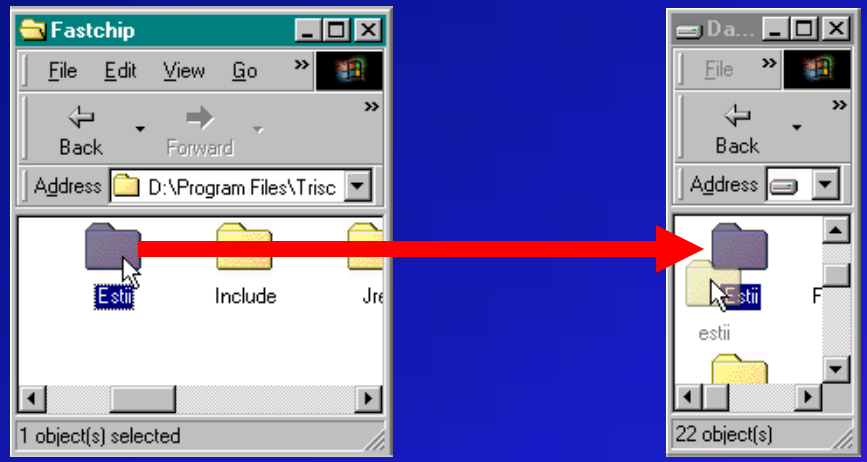
Copy FastChip \estii Directory

- Contains Triscend-specific configuration data
- Copy **<FastChip>\estii** directory from FastChip installation directory to **`\Estii`** installation directory UPDATE



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visionCLICK Software Limitations

- visionPROBE II cable does not require a license (unlimited use)
- A7 Starter Kit ships with an evaluation version of visionCLICK
- visionCLICK limited to 200 debugging sessions
- Full version of visionCLICK from WindRiver for additional $3,700

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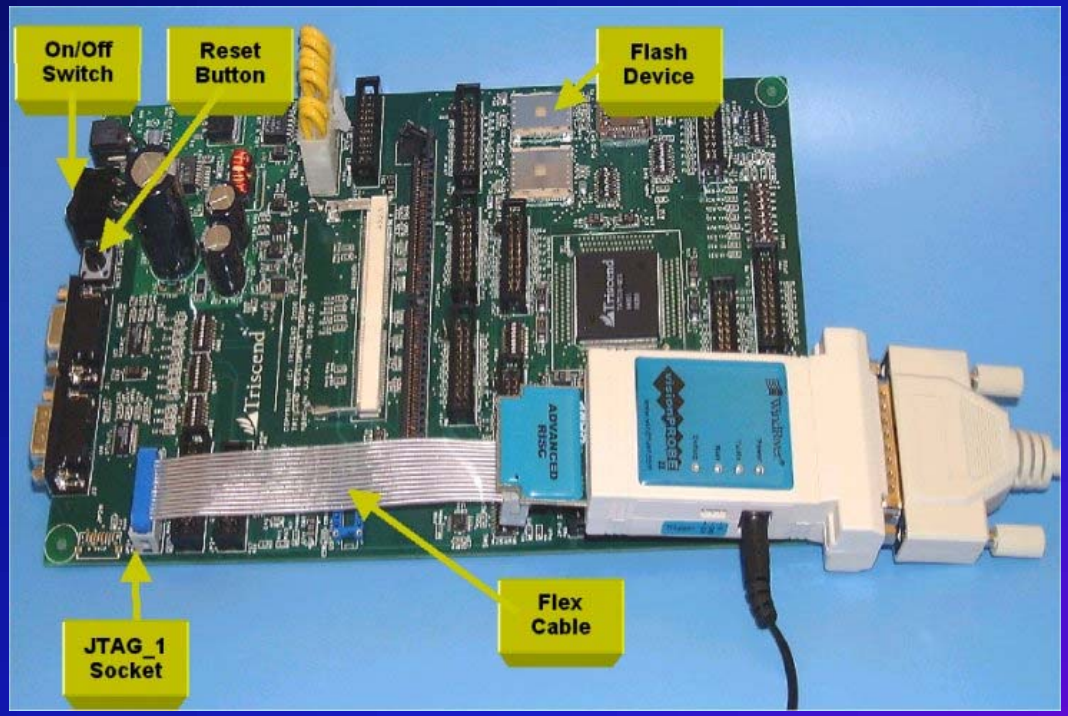
Installing visionPROBE (a)

- Connect parallel cable
- Connect flexible header to visionPROBE
- Connect power supply to visionPROBE
- Connect to JTAG_1 socket on A7 Eval. Board
- Apply power to all



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Installing visionPROBE (b)

- Parallel port must be configured and enabled as Extended Capabilities Port (ECP)
- visionPROBE **`comdll.cfg`** must specify I/O address and interrupt request number
- Use visionPROBE's **`VPTest.exe`** to verify proper connections

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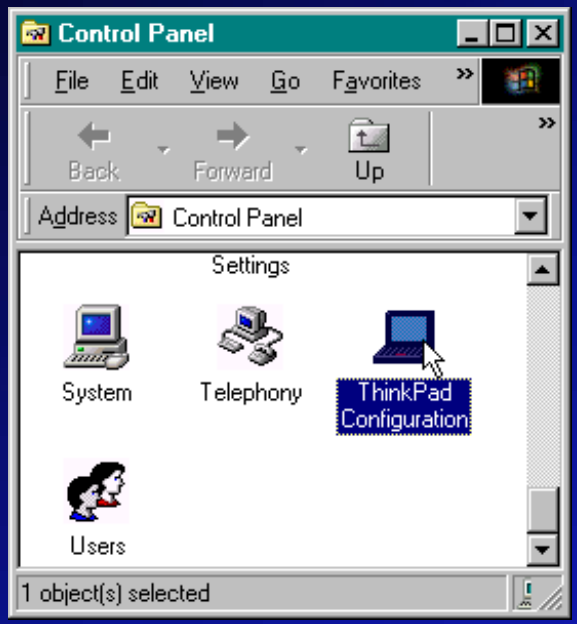
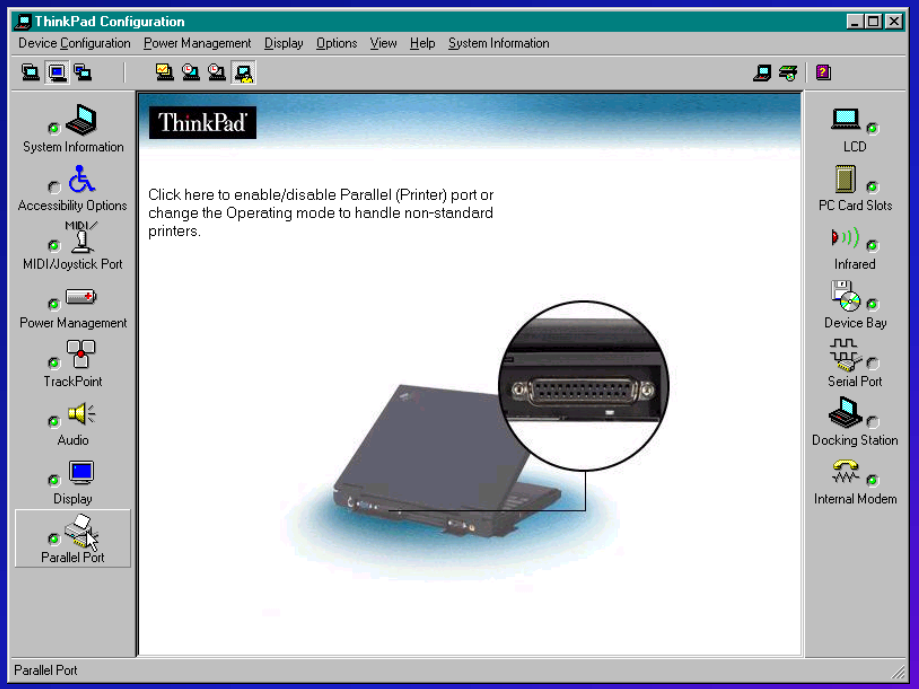
ECP Mode on Thinkpad (a)





Open the Windows Control Panel. Double-click **ThinkPad Configuration**.

Click **Parallel Port**.

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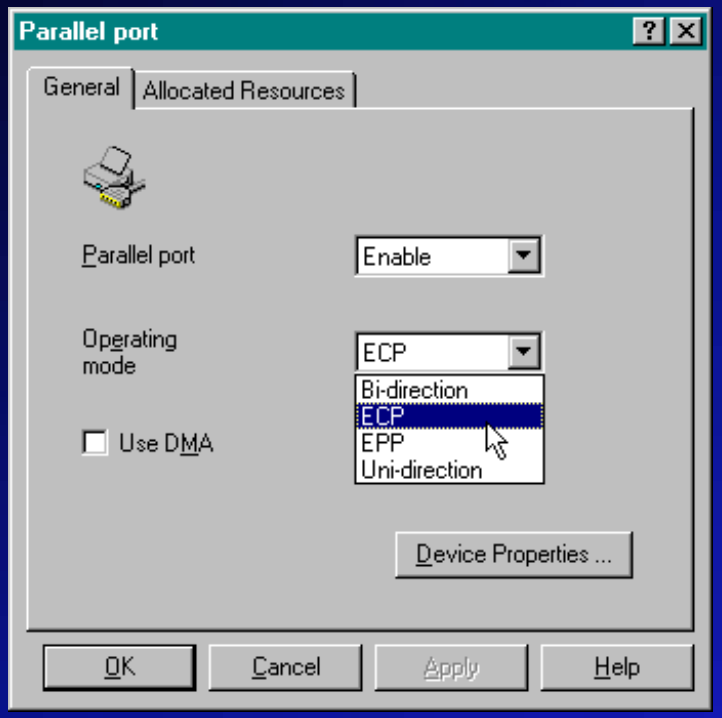
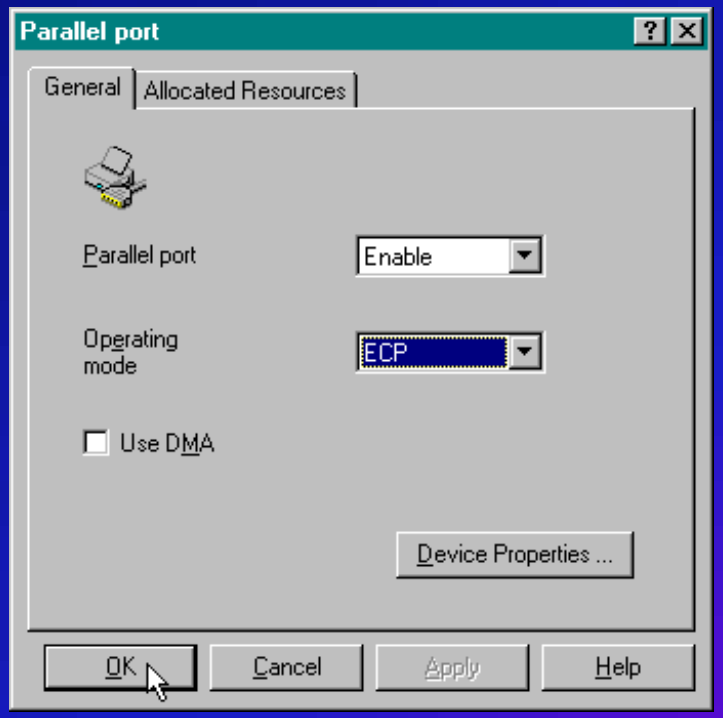
ECP Mode on Thinkpad (b)



Enable parallel port. Select **ECP** mode.



Click **OK**. May require rebooting your computer.

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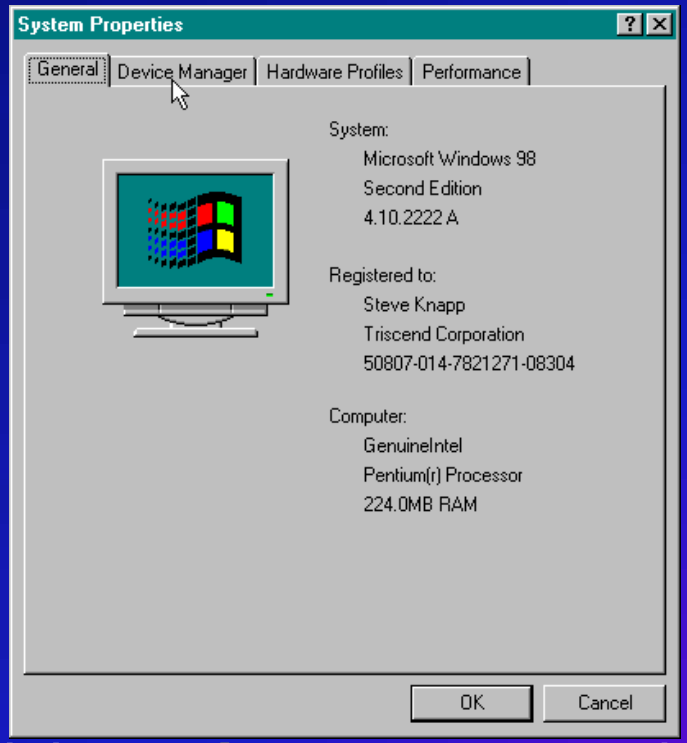
Determine ECP Settings (a)

Open the Windows Control Panel. Double-click **System**.



Click **Device Manager** tab.

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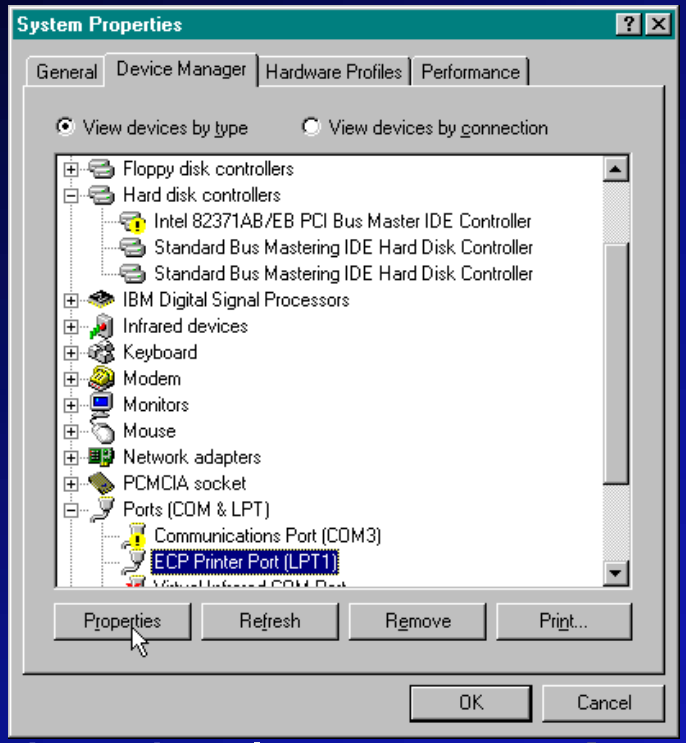
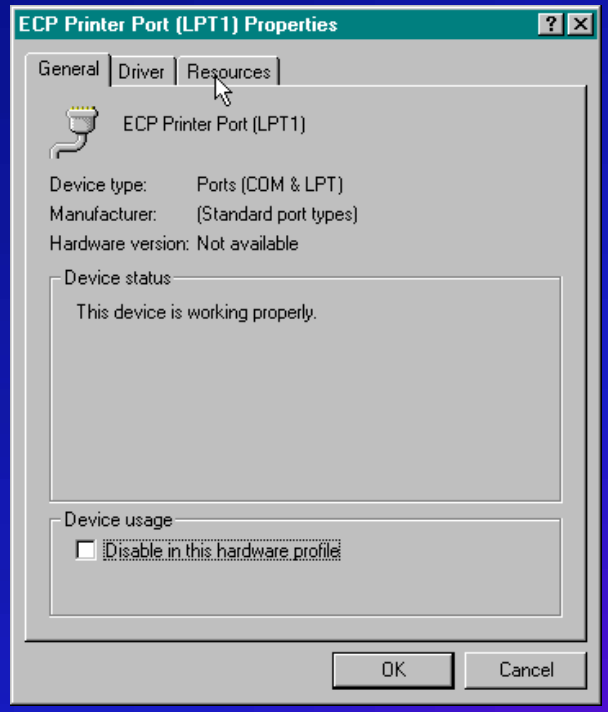
Determine ECP Settings (b)



Find and select **ECP Printer Port**. Click **Properties**.



Click **Resources** tab.

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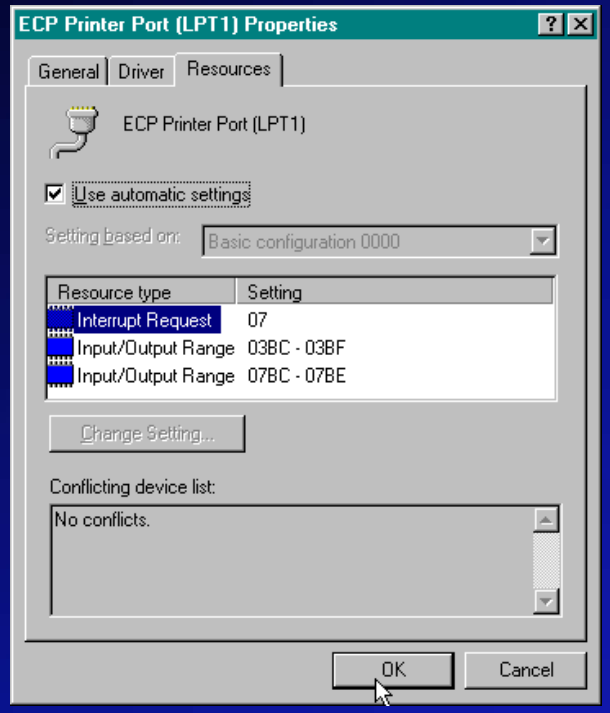
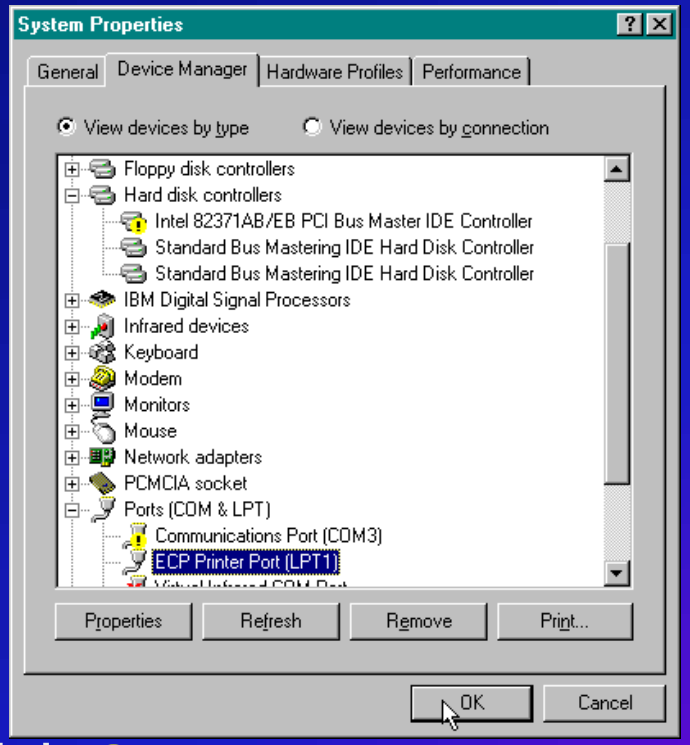
Determine ECP Settings (c)





Record settings for **Interrupt Request** and **Input/Output Range**. Click **OK**.

Click **OK**.

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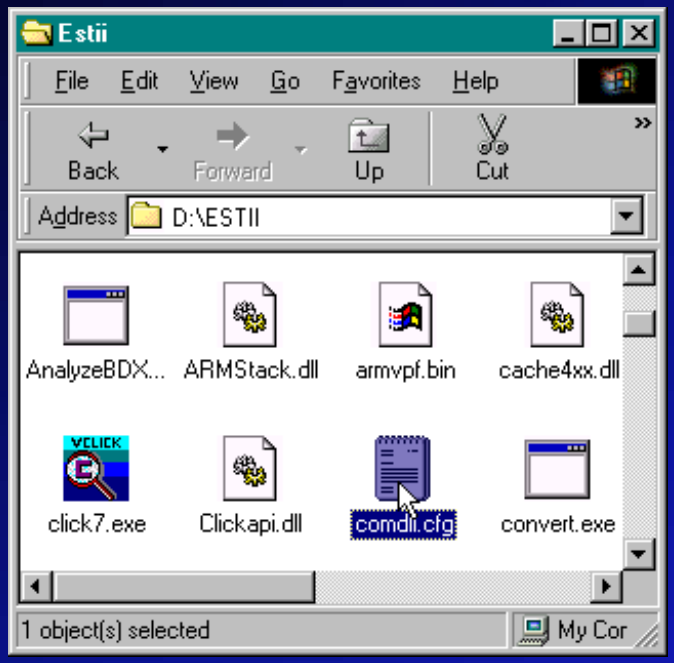
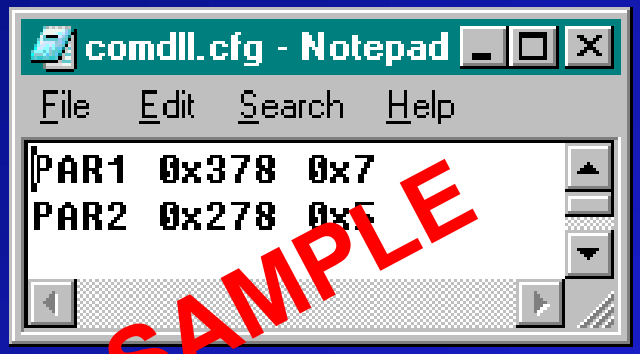
Configure visionPROBE Communications





Open **comdll.cfg** file in the **/Estii** directory.

Modify entries based on your computer's ECP settings. **Save** the file.

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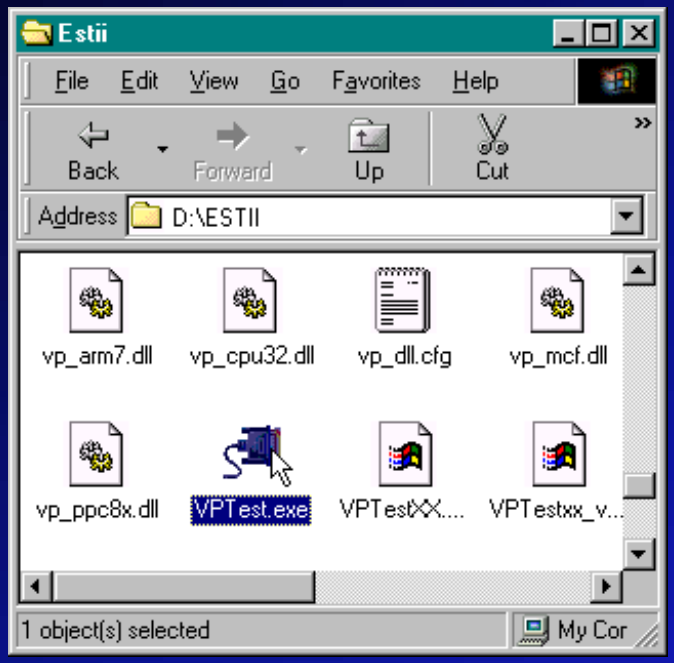
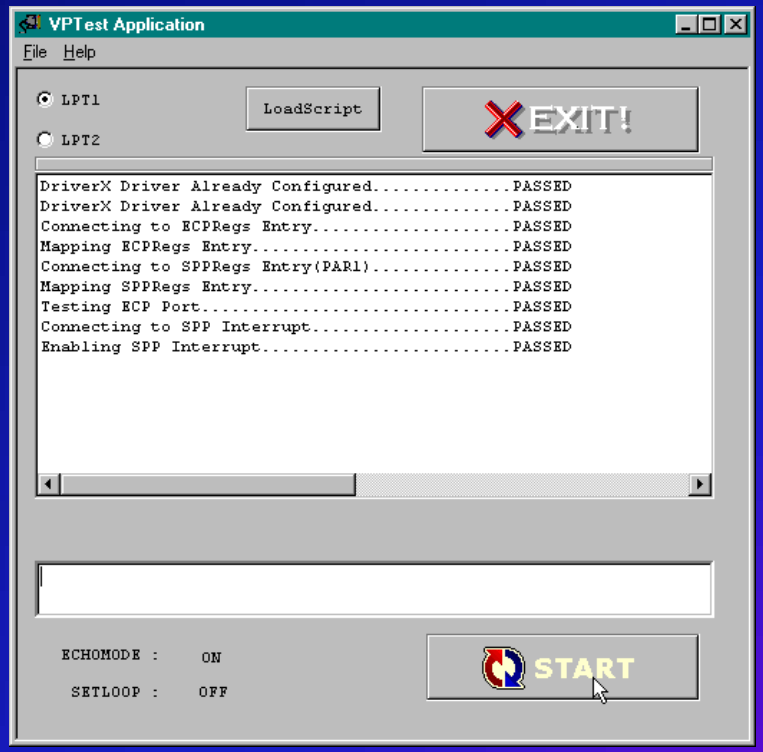
Testing visionPROBE using VPTest.exe (a)





Connect board, cable, supplies.

Double-click **VPTest.exe** in the **/Estii** directory.

Check that all port tests PASSED!. Click **START** to begin probe diagnostics.

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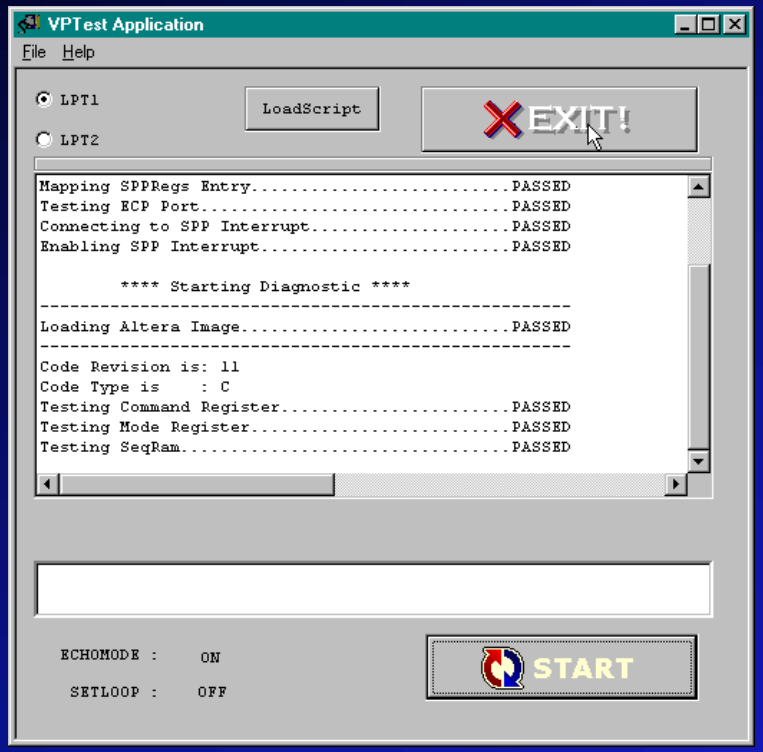
Testing visionPROBE using VPTest.exe (b)



Check that all diagnostic tests PASSED!. Click **EXIT!**.

Remove and re-apply power to visionPROBE!

```
DriverX Driver Already Configured.....PASSED
DriverX Driver Already Configured.....PASSED
Connecting to ECPRegs Entry.....PASSED
Mapping ECPRegs Entry.....PASSED
Connecting to SPPRegs Entry(PAR1).....PASSED
Mapping SPPRegs Entry.....PASSED
Testing ECP Port.....FAILED
   ECP Control Register Bits 0 & 1 != 0x2.
   ECP Control Register Value = 0xff **
!! Unable to Use visionPROBE Without a Valid ECP Port !!
```

What if it fails?

Mostly likely cause is ECP port related.

Recheck your setup.

Use the ***visionPROBE II Hardware Installation Guide***.

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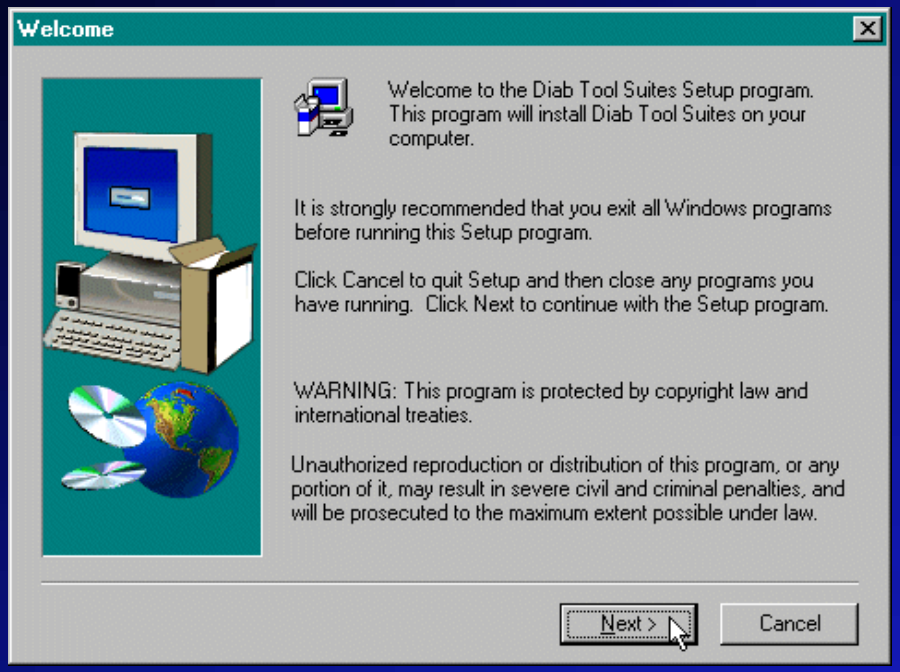
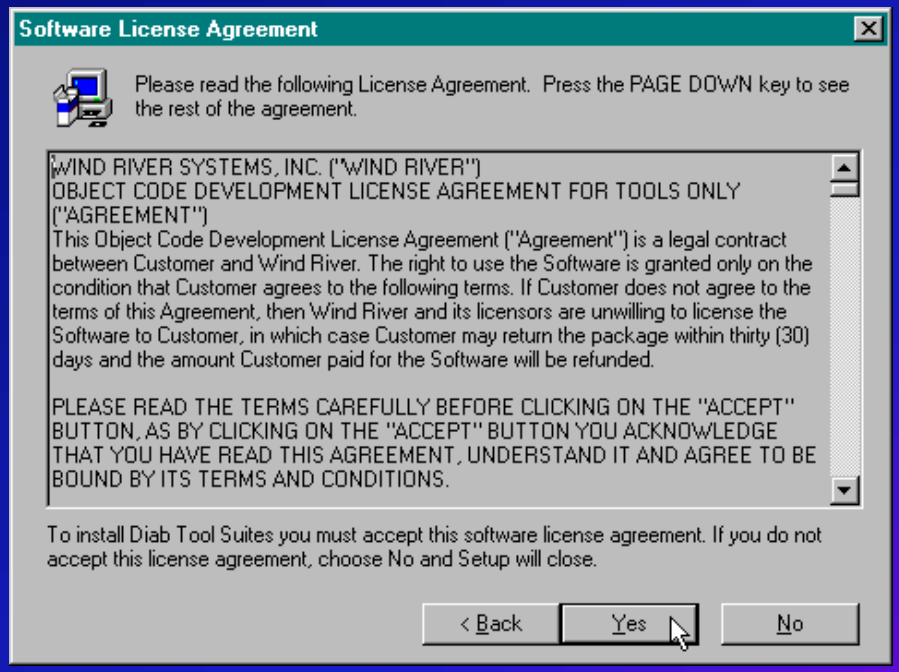
Installing Diab Compiler (a)



Read the welcome screen. Click **Next >**.



Read the license. Click **Yes** to accept the terms.

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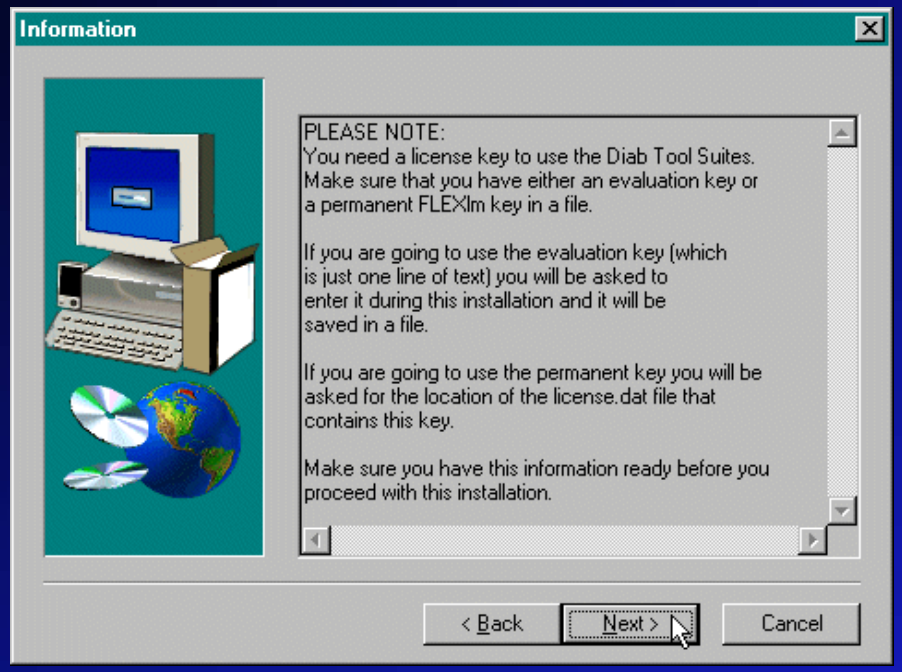
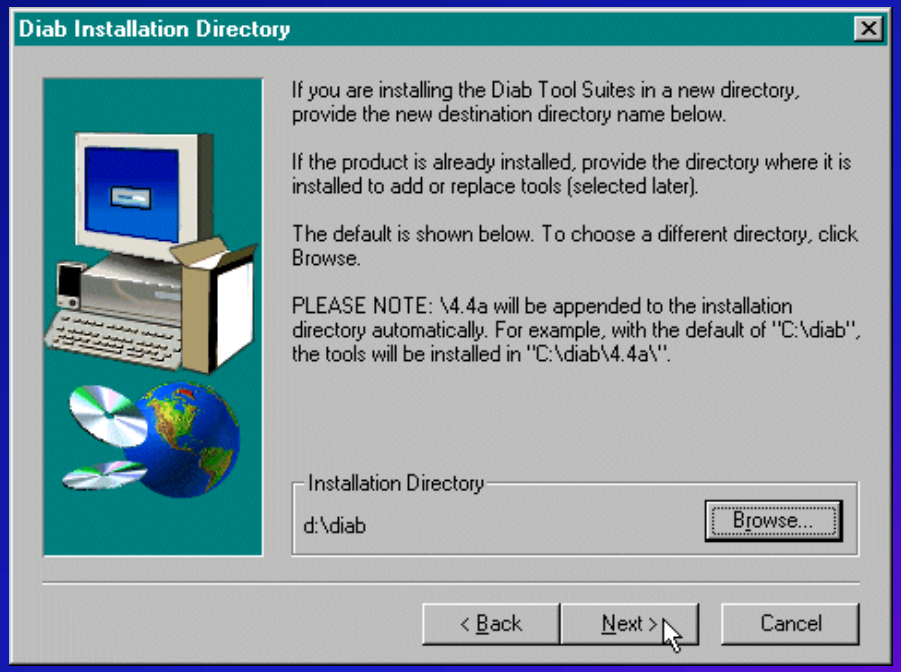
Installing Diab Compiler (b)



Read the information about the FLEXlm license key. Click **Next >**.



Select an installation directory. Click **Next >**.

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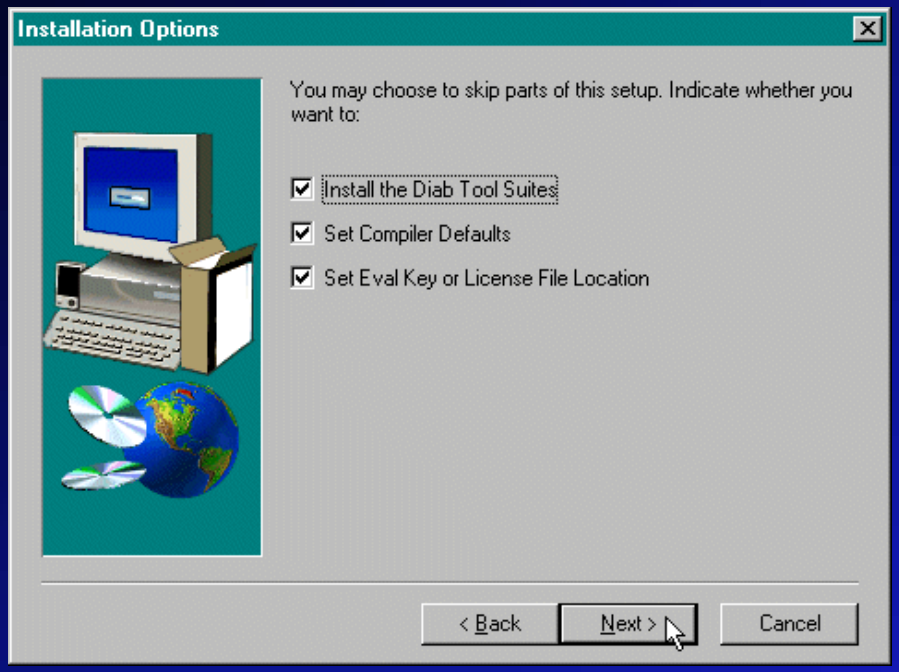
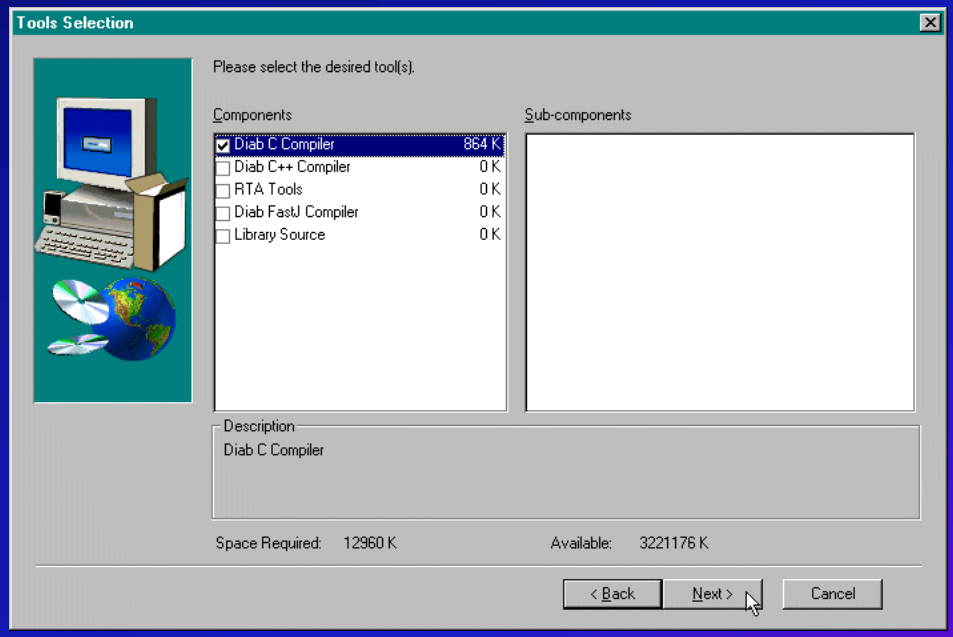
Installing Diab Compiler (c)





Select all options.
Click **Next >**.

Select the **Diab C Compiler** option. Click **Next >**.

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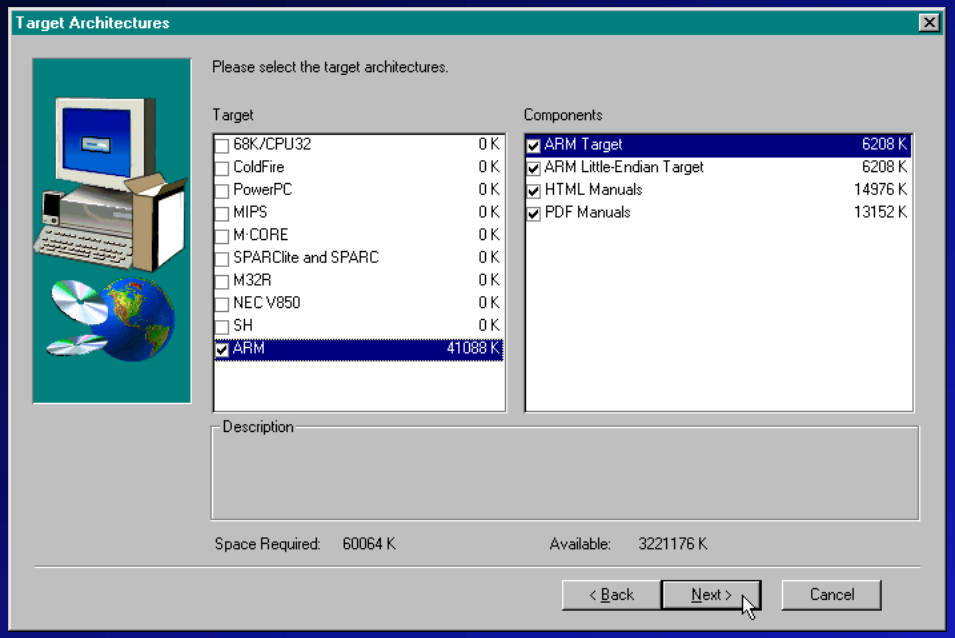
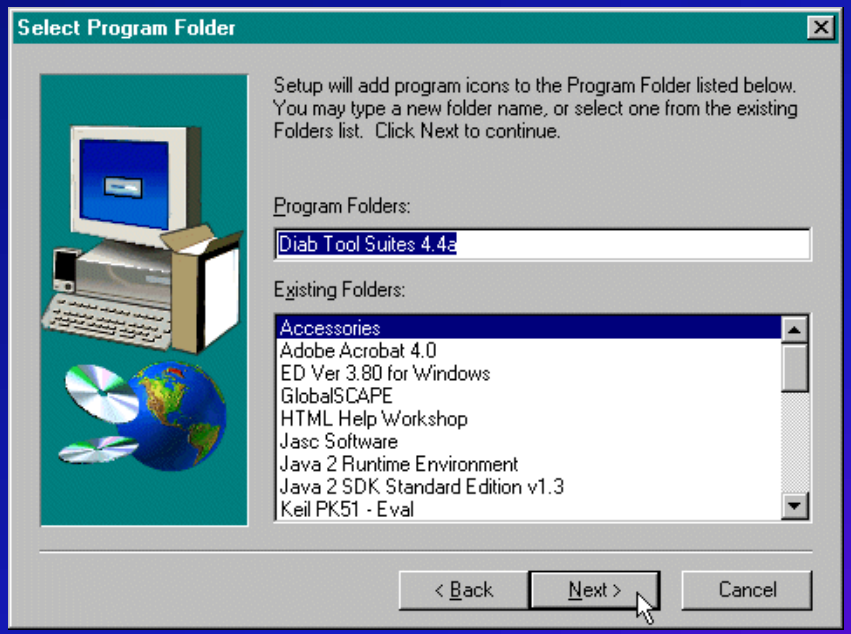
Installing Diab Compiler (d)





Select all options. Click **Next >**.

Select a program Folder. Click **Next >**.

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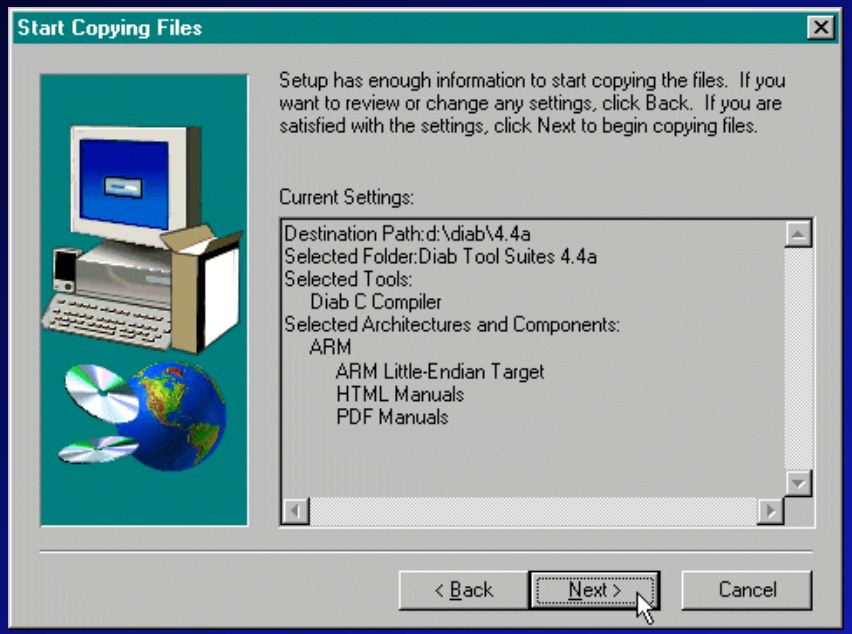
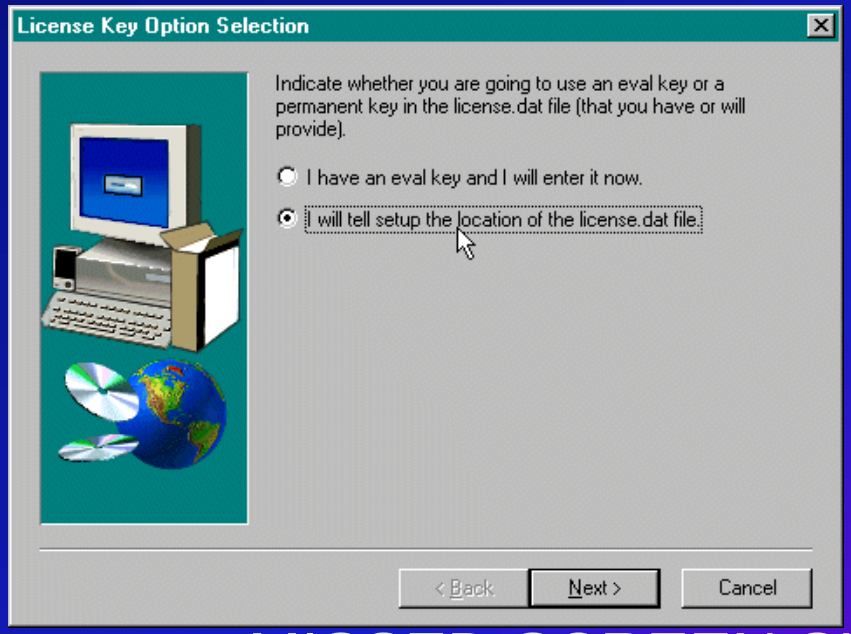
Installing Diab Compiler (e)



Review the installation options.
Click **Next >**.



MISSED SCREEN SHO

Select **I will tell setup ….**
Click **Next >**.

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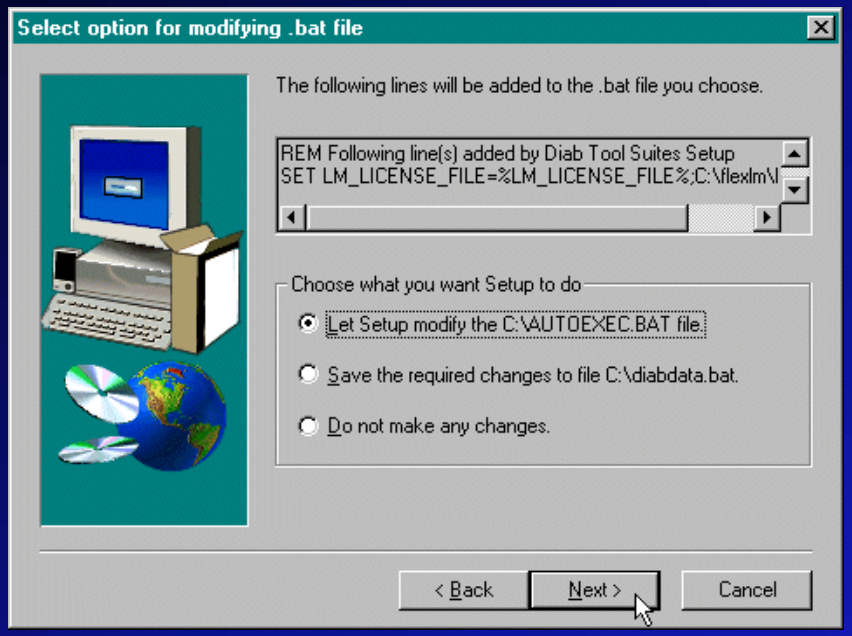
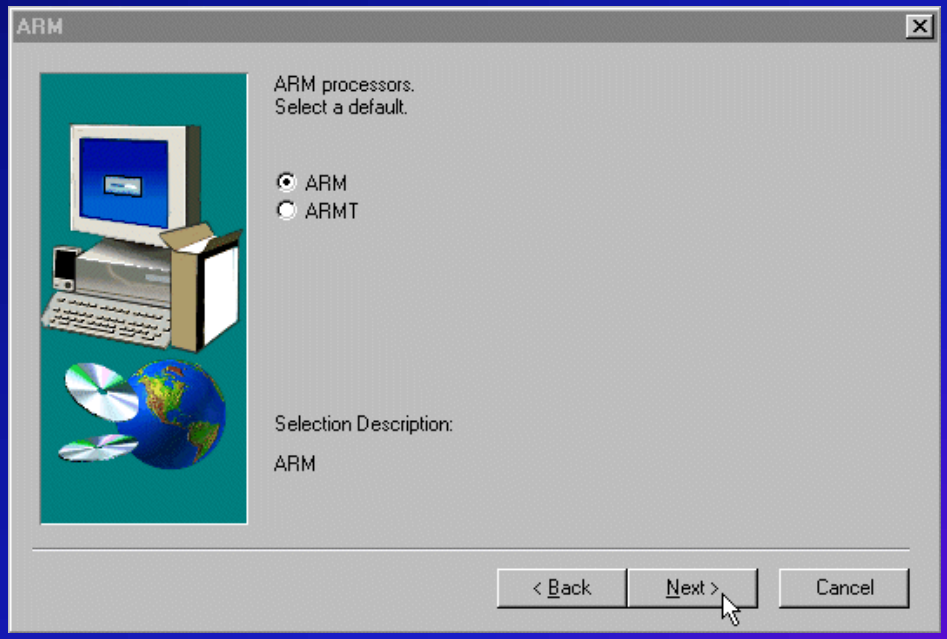
Installing Diab Compiler (f)





Choose **Let Setup modify ….** Click **Next >**.

Select **ARM**. Click **Next >**.

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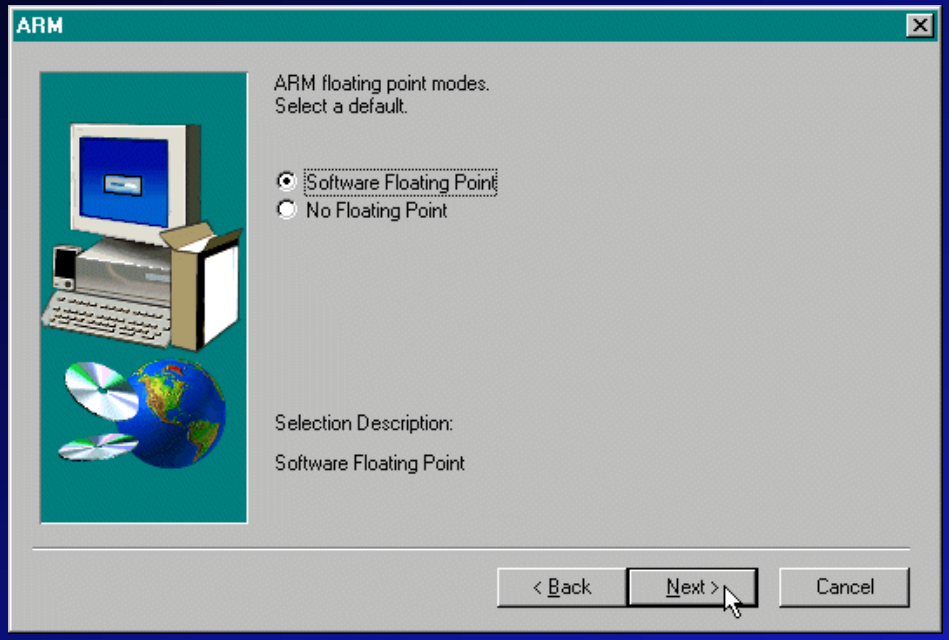
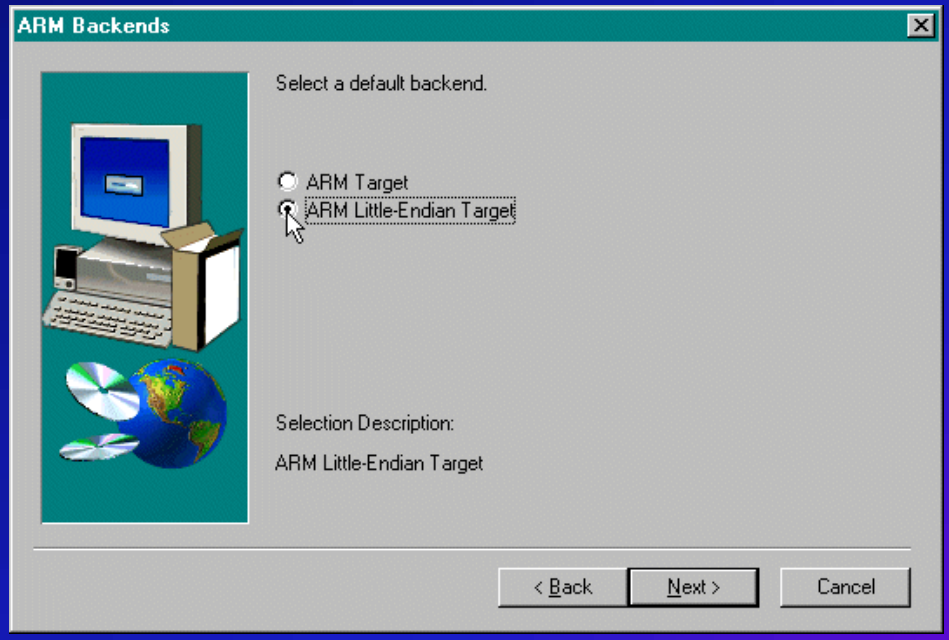
Installing Diab Compiler (g)





Choose **Software Floating Point**. Click **Next >**.

Select **ARM Little-Endian Target**. Click **Next >**.

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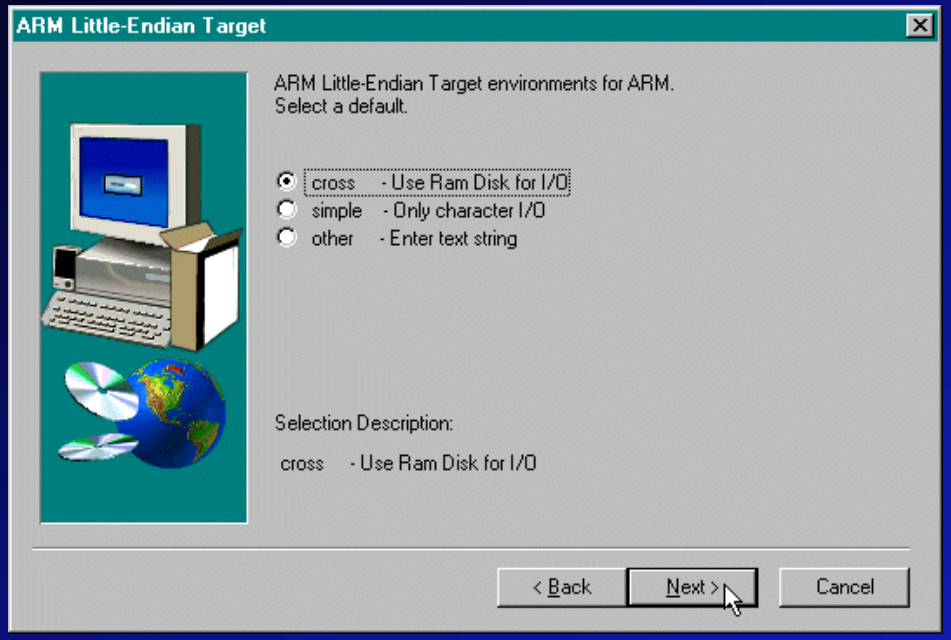
Installing Diab Compiler (h)



Choose **cross**. Click **Next >**.

If other compiler options are desired, use the –t option. Click **Next >**.

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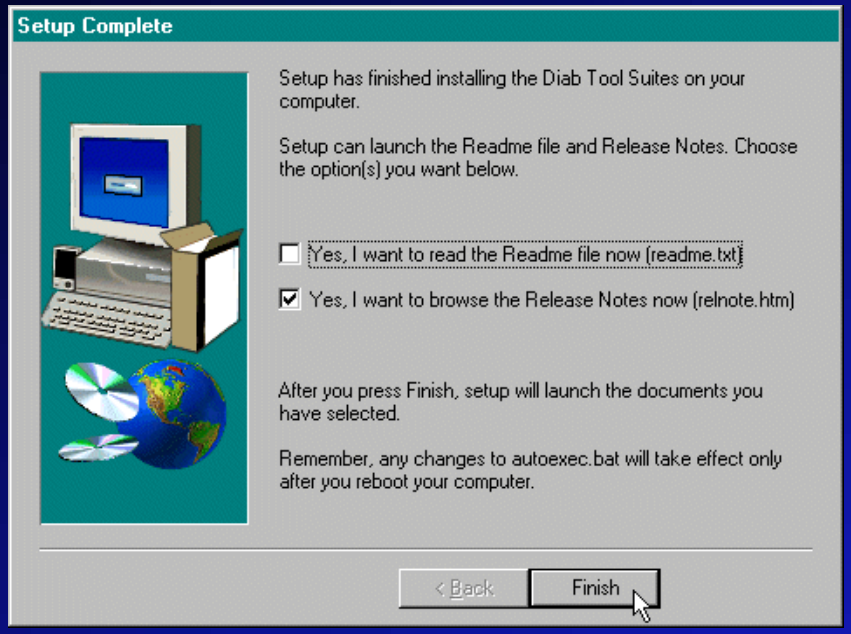
Installing Diab Compiler (i)



All settings defined. Click **Finish** to complete installation.

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Diab Compiler Evaluation

- C/C++ compiler, assembler
- 45-day evaluation version shipped on CD-ROM
- Uses FLEXlm license manager
  - **`SET LM_LICENSE_FILE=c:\flexlm\license.dat`**
- Edit /flexlm/license.dat and enter the following

```
FEATURE DIABEVAL Diab 4.400 28-Feb-2001 0 \
3CAAB01492B635C8B3E3 HOSTID=DEMO ck=32 SN=temp
```

- Without license …

```
fatal error (dcc:1635): License error:FLEXlm
error: No such feature exists -5,357:2 ()
```

- Full version of visionCLICK from WindRiver for additional $2,200 (C), $2,400 (C++)

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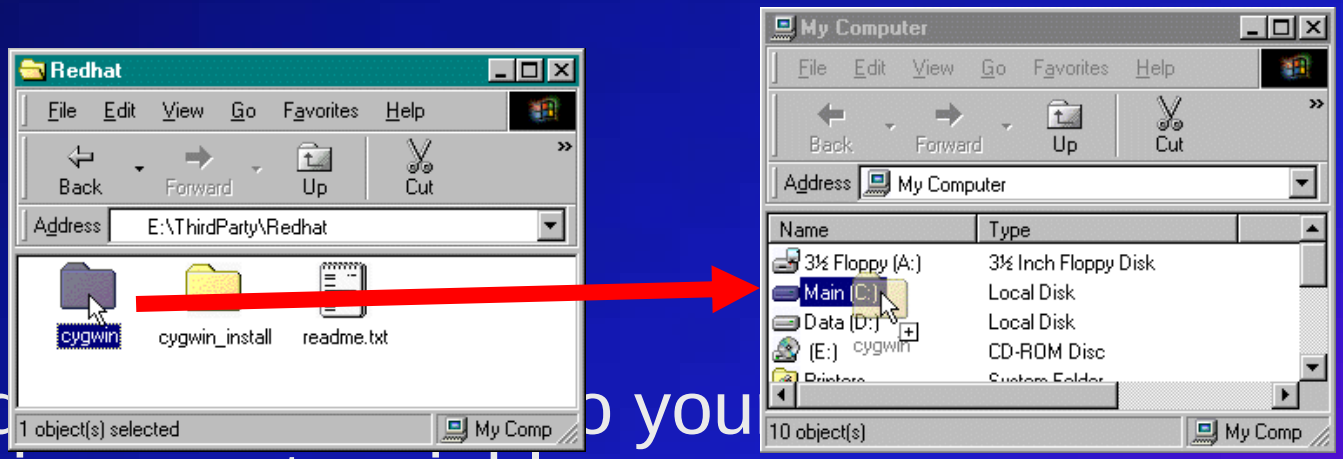
Installing Cygwin

- Cygwin adds support for FastChip command-line Make scripts
- Copy **\ThirdParty\Redhat\cygwin** directory from FastChip CD-ROM to your **C:** drive



- Add[illegible]o you environment variable

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Installation Complete!

PHEW!!!

- Now the fun part begins …

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FastChip Licensing

- Full, Licensed Version
  - No restrictions
  - Use any E5 or A7 device
  - Requires use to license FastChip using the Triscend-supplied key
- Evaluation, Un-licensed Version
  - Default mode after installation
  - Use any device, but can only Bind designs with 256 or less CSL cells

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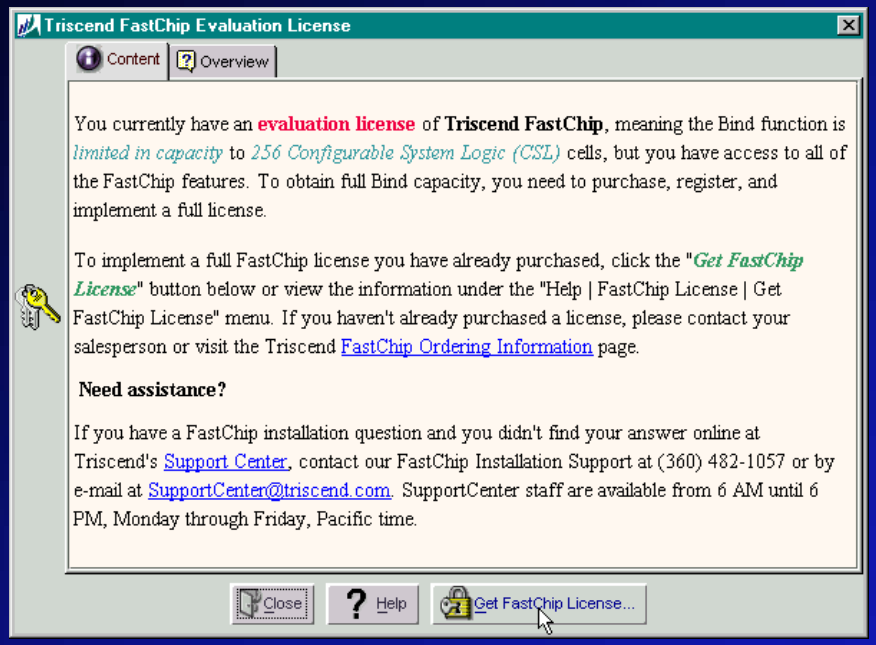
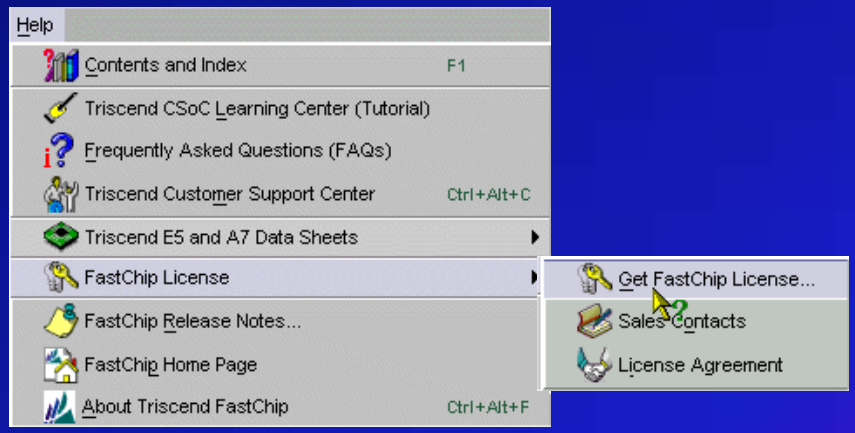
Two Ways to License





Unlicensed version displays a special message every time you start FastChip. Click **Get FastChip License**.

From within FastChip, click **Help → FastChip License → Get FastChip License**.

Triscend®

Connecting to the Triscend License Server

- Licensing is automatic if customer connected to Internet
- Use license number provided with FastChip CE-ROM
- FastChip ID transmitted to Triscend when you click the **Get FastChip License** button

Triscend®

Enter License Information

- Enter license key from CD-ROM label
- Enter your personal contact information

Triscend®

License Server Response

- Triscend replies via E-mail to the address entered
- E-mail contains a small file called **FCLicense.tjr** (about 150 bytes)
- E-mail also describes how to install the *.tjr file.
  - Save the file into FastChip directory
  - **<install path>\Triscend\FastChip**

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Licensing Woes

- Customer installed *.tjr in wrong directory
- Customer does not have Internet access
- Customer cannot connect to Triscend license server
- Customer's firewall security rejects E-mail attachments
- FAE attempted to create license by clicking **Get License** on his machine
  - Use www.triscend.com/products/indexfc2lic.html
- Contact SupportCenter@Triscend.com or http://support.triscend.com

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FastChip A7 Tutorial

- 50+ pages of heart-stopping, action-packed, hands-on adventure
- Covers …
  - FastChip
  - FDL
  - Diab
  - visionCLICK
  - Make files
- Purposely simple (Rio Grande River)
- Soon to be a major motion picture!

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FastChip Tutorial Users

- Part 1
  - Create a new design called ‘MyFirstA7’
  - Covers FastChip and FDL
  - Download to the A7 Evaluation Board
  - Primarily for hardware engineer
- Part 2
  - Use ‘MyFirstA7’ created earlier or ‘MyDesignA7’ from CD-ROM
  - Covers Diab C compiler and visionPROBE software
- Part 3
  - Using FastChip command line and Make files

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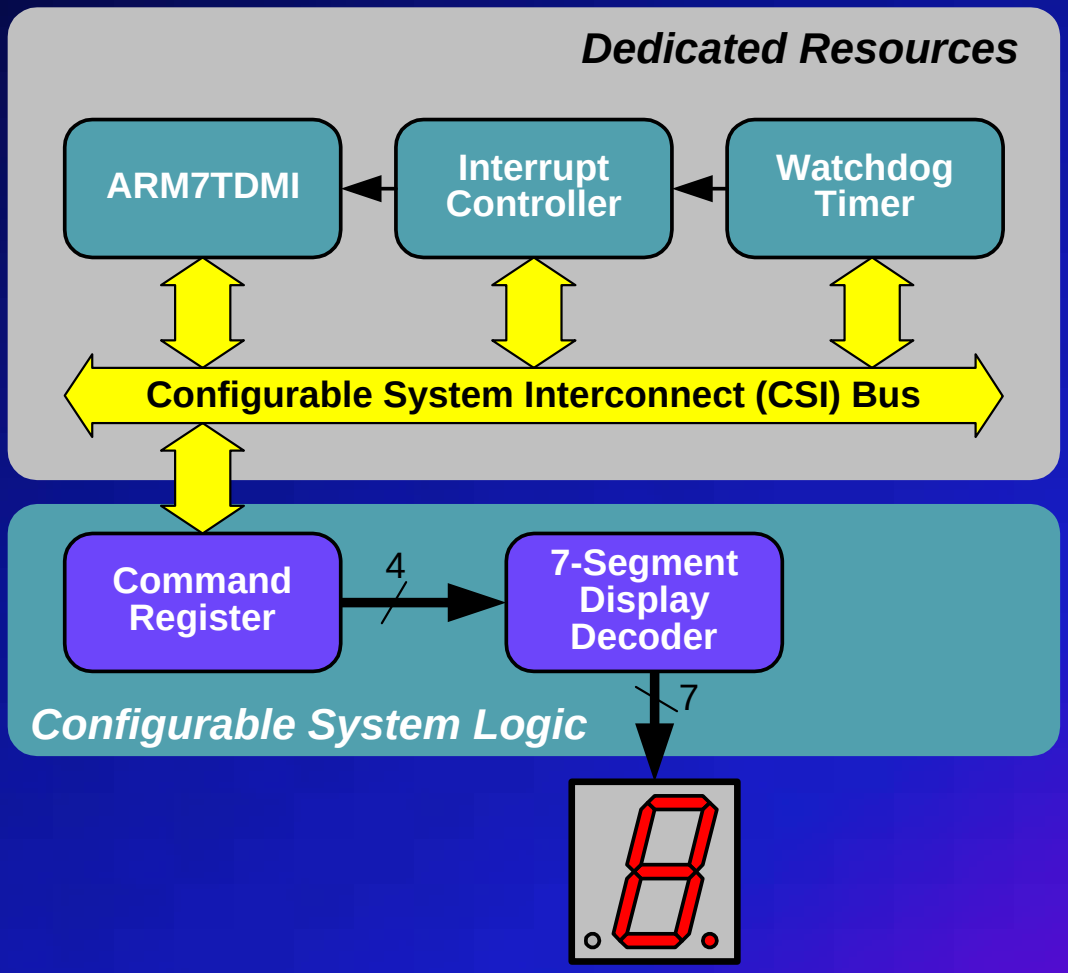
A7 Tutorial CSoC Design



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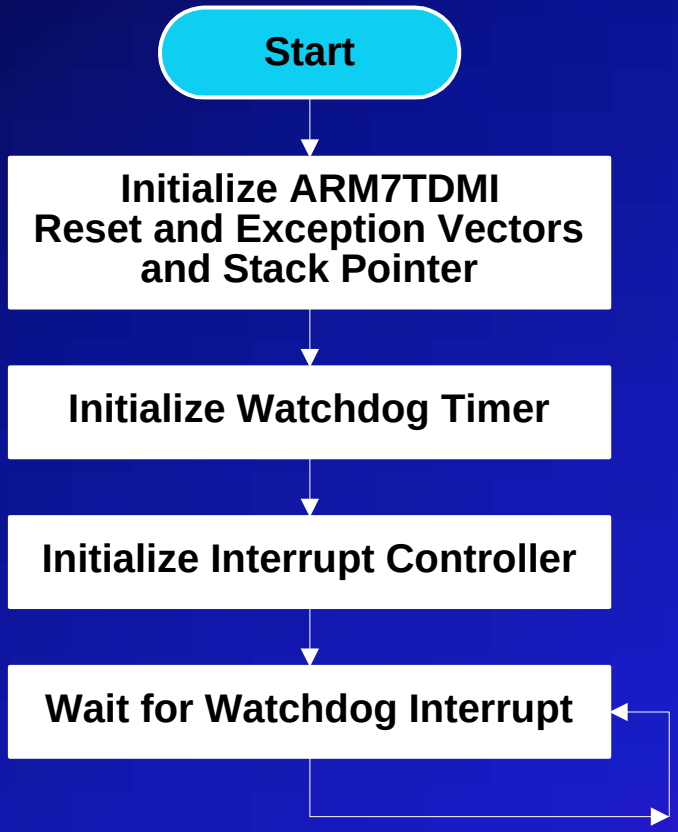
A7 Tutorial ‘C’ Program



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FastChip Display Problem on Thinkpad/NeoMagic

- Small gray boxes appear in FastChip/FDL, corrupting graphics display
- Only on laptops with NeoMagic graphics chipset
- Related to Sun's Java virtual machine
- Next slide describes work-around
- Required each time you start FastChip or FDL

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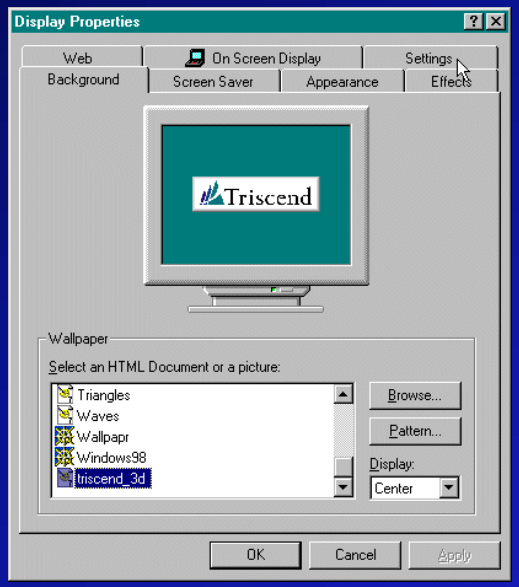
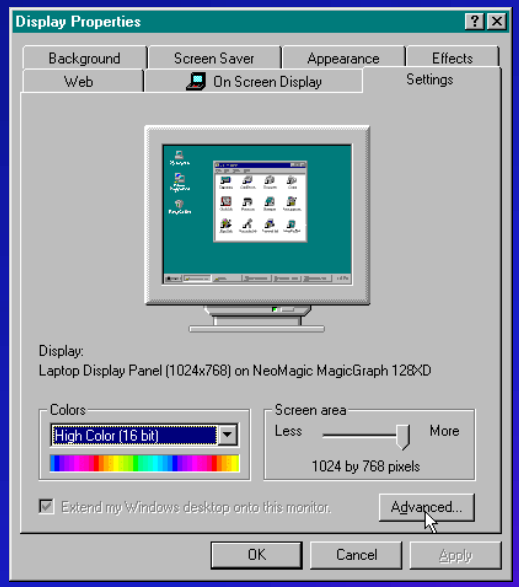
Thinkpad/NeoMagic Workaround (a)

Right click on empty Desktop area. Select **Properties**.



Click **Settings** tab.



Click **Advanced** button.

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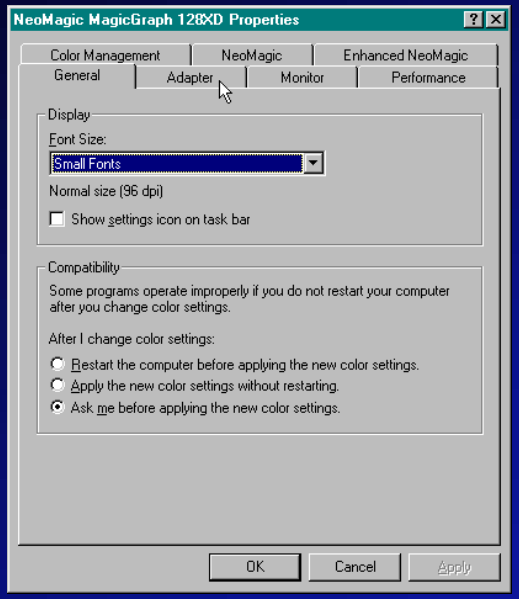
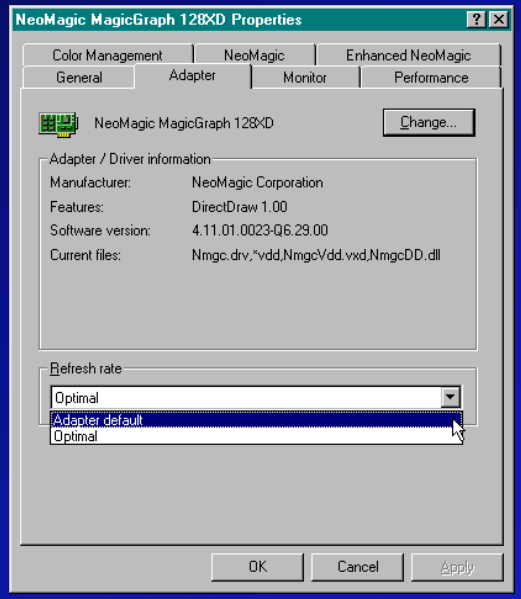
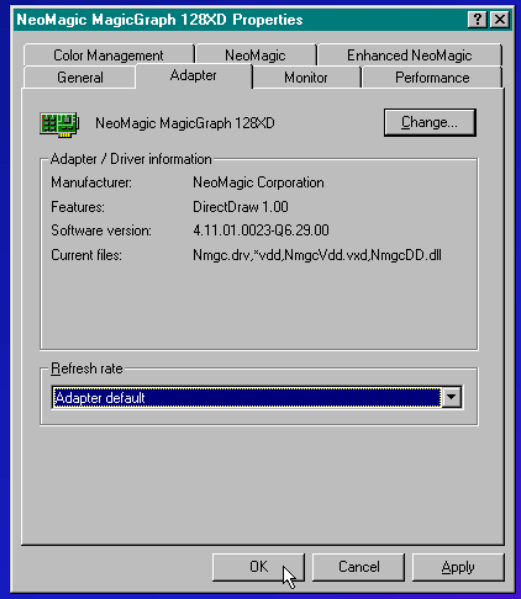
Thinkpad/NeoMagic Workaround (b)



Click **Adapter** tab.



Select any **Refresh rate** setting.



Click **OK**.

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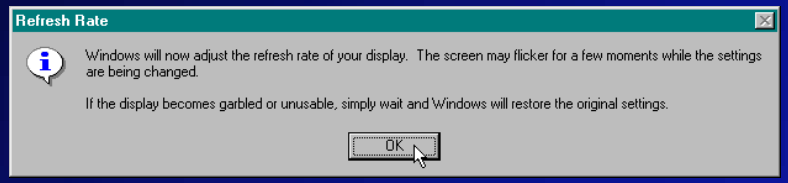
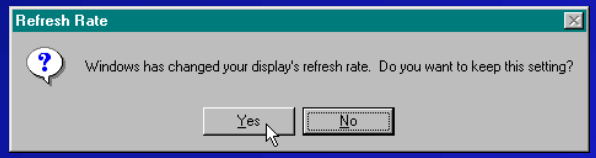
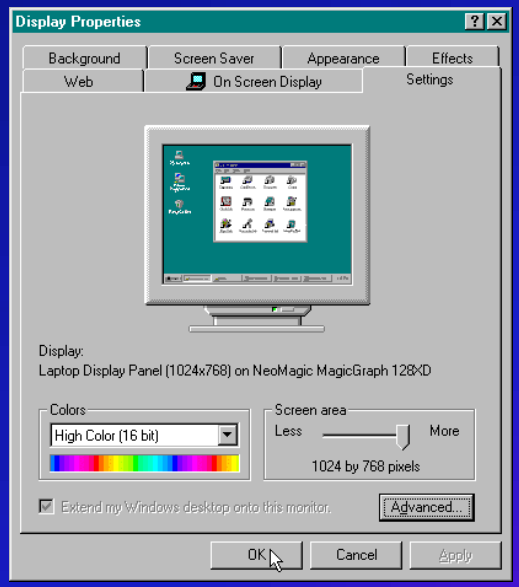
Thinkpad/NeoMagic Workaround (c)



Click **OK**.



Click **Yes**.



Click **OK**.

- Small gray boxes should be gone!

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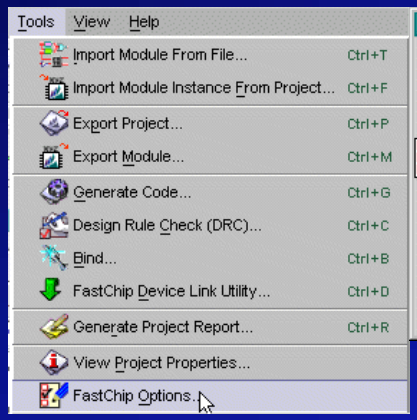
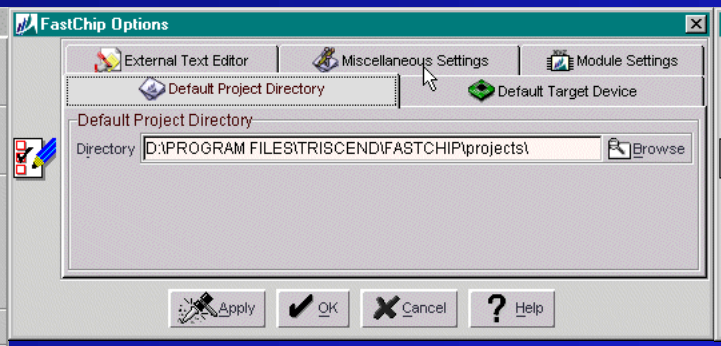
FastChip File Defaults

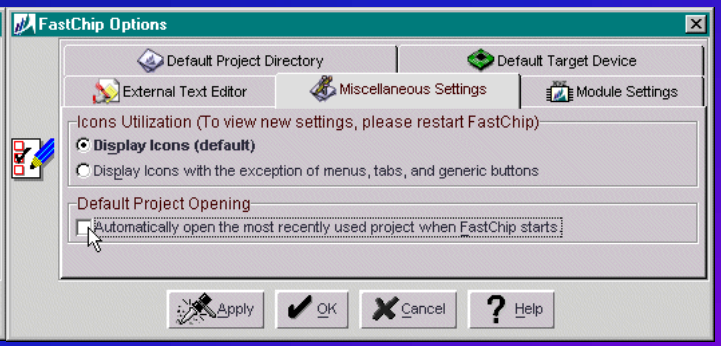
- By default, FastChip loads the last project
- Useful for most customers
- Not always useful for FAEs



Select **Tools → FastChip Options**.



Click **Miscellaneous …** tab.



Uncheck **Automatically open …** option. Click **OK**.

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Project Management

- FastChip start-up behavior
- Migrating a FastChip 1999 design
- Create a new project
- Select a target device
- Add project notes
- Examine resources on target device
- Modify FastChip options
- Changing the target device

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Miscellaneous Management

- Help
- Triscend menu
- Document directory

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FastChip Main Window

- Menu and tool bar
- Dedicated Resources
- CSL Window
- Module Library area
- Resource Estimate
  - Shows pre- or post-Bind resources
- Command Output
- Status Bar
- Control the FastChip layout

Triscend®

Working with Modules

- FastChip module library tree
- Find a module
  - By hierarchy or by list
  - Search capability
- Use online help
- Configure a module
  - Define an address
  - Define connections
- Other module functions
  - Delete, duplicate, export
  - Re-arrange screen layout

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New FastChip Modules

- Modules are now architecture specific
  - E5 or A7
- Arithmetic
  - Divider, Multiplier, Square Root
- Serial I/O
  - New SPI, I2C masters
- Communications
  - HDLC
- Encryption
  - DES (EBC and CBC mode)
  - Triple DES

Triscend®

What are Deprecated Modules?

- Some modules have been improved, updated, enhanced
- Old versions remain
  - Maintain compatibility of customer's design
  - Don't fix it if it ain't broke!
- Deprecated modules issue warning message
- All stored in the Deprecated library directory

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Working with Connections

- Find an existing connection
  - By hierarchy
  - By name
  - Defining buses (multi-bit connections)
- See connectivity from FastChip main window

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Assigning I/O

- Define the Memory Interface Unit (MIU)
  - Configure static memory interface (Flash)
  - Configure SDRAM interface
- Assign Programmable I/O (PIO) pins
- Set electrical characteristics
- Settings saved in **`*.ioc`** file

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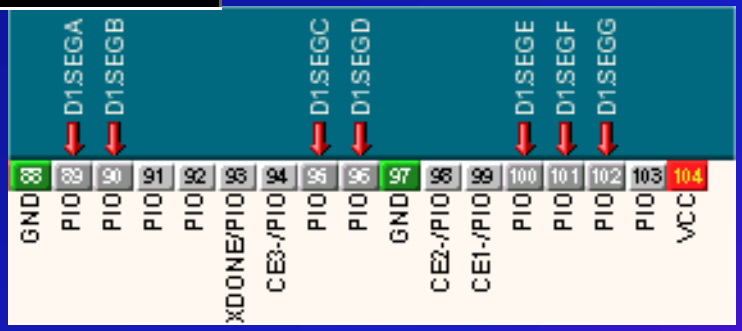
Assign 7-Segment PIO

Module	Pad Name	Pin Number
D1	D1.SEGA	89
	D1.SEGB	90
	D1.SEGC	95
	D1.SEGD	96
	D1.SEGE	100
	D1.SEGF	101
	D1.SEGG	102



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Generate a Header File

- Passes register assignments to your compiler
- #include in ‘C’ source file
- Also include triscend_a7.h header file

Triscend®

Design Rule Check (DRC)

- Verify correctness of design before completing next step
- FastChip executes DRC many times during a design
- Unused sideband signal generate DRC warnings

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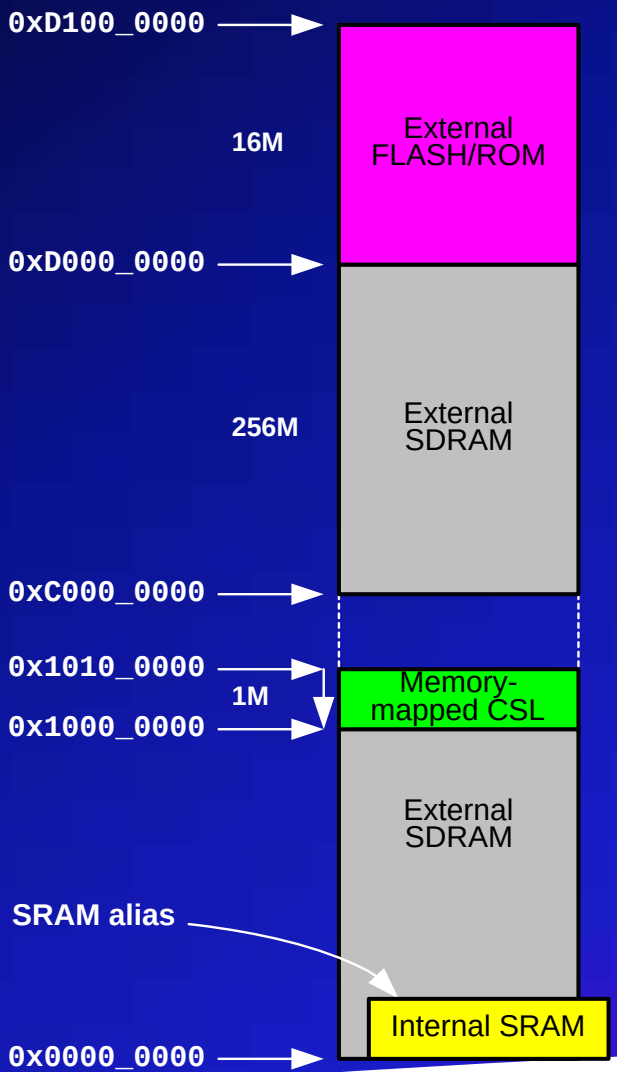
Default A7 Memory Map



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Constraining Addresses

- Define where Selector addresses reside
  ```
  ALLOCATE START=0x1000_0000 SIZE=1M
  DIRECTION=DOWN;
  ```
- Specify address for a specific Selector
  - Requires “FastChip” name
  - See **`*.al`** file
    ```
    ADDRESS RESULT.CMDREG @ 0x100f_fe00;
    ```
- Prohibit a range of addresses
  ```
  PROHIBIT START=0x100f_ff00 SIZE=256;
  ```
- Saved in **`*.adc`** file

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What is Bind?

- Analogous to existing design steps
  - Compile/Link/Load for software development
  - Map/Place/Route for ASIC design
- Very compute and memory intensive
- Executes in minutes to hours, depending on …
  - Computer speed
  - Device size and utilization

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What Does Bind Do?

- Automatically assigns, programs Selectors
- Maps logic to CSL logic resources
- Optimally places CSL cells, Selectors on device
- Routes signal connections between CSL resources
- Computes static timing for delay paths
- Generate CSL programming file

Triscend®

Bind Effort Levels

- Trade off final design quality with faster Bind execution time
- Three effort levels
  - Minimum: Fastest run time, Moderate results
  - Medium:
  - Maximum: Slowest run time, Best results
- Timing-driven mode

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Timing-Driven Bind

- Why timing-driven Bind?
  - Tell Bind your timing requirements
  - Bind attempts to meet your requirements
  - Project report shows any missed requirements
- What are the drawbacks?
  - Significantly slower Bind execution time
  - Current interface is awkward
  - Capabilities are very immature in FC2.1.2

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What is Awkward Today?

- Connections are based on a pin list
- The pin names are hierarchically qualified based on the flattened, mapped netlist
  - Info available in *.m file
  - Must run Bind to create *.m file
- Dig through the netlist to find what you need
- Run times can be geologic!

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How to Process a Design

- Bind it once
- Save the design
- Open the *.m file
- Look for the desired start and end points
- Define your constraints in the *.tic file
- Run Bind in timing-driven mode
- Generate project report to see results

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What Can You Specify? (a)

- *.tic file contains your timing constraints
- CREATE_CLOCK
  - Specify clock net
  - Specify clock period (WARNING: no decimal points allowed. 12.5 ns = 12500 ps
  - Duty cycle
- SET_MAX_DELAY
  - From and To points
  - Worst delay allowed

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What Can You Specify? (b)

- Hierarchically qualified pin names required for From and To points
- Pin macros make it easier
  - ALL_INPUT_PINS - all .i pins of input pads
  - ALL_OUTPUT_PINS - all .o pins of output pads
  - ALL_CLOCK_PINS(<clkNet>) - all clock pins of registers directly clocked by net <clkNet>
  - ALL_SETUP_PINS(<clkNet>) - all non-clock input pins of registers clocked by net <clkNet>
  - ALL_SOURCE_PINS(<Net>) - pins that drive the net <Net>
  - ALL_LOAD_PINS(<Net>) - pins that are loads on the net <Net>

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Try It, You Might Like It

- GOAL: Define maximum clock-to-output time from BusClock to any output pad at 40 MHz (25 ns period)
- From `*.m` file
  - net RESULT.clock;
- Create `*.tif` file constraint
  - set_max_delay 25ns
    -from ALL_CLOCK_PINS(RESULT.clock)
    -to ALL_OUTPUT_PINS

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A Slightly Harder Example

- GOAL: Specify delay from RESULT register to 7-Segment LED outputs to 30 ns
- From `*.m` file
  - busclk RESULT.bclk (.o=RESULT.clock);
  - pad D1.SEGA (.o=D1.sega, …
- Create `*.tif` file constraint
  - set_max_delay 30 ns
    -from RESULT.bclk.o
    -to D1.SEG*.o

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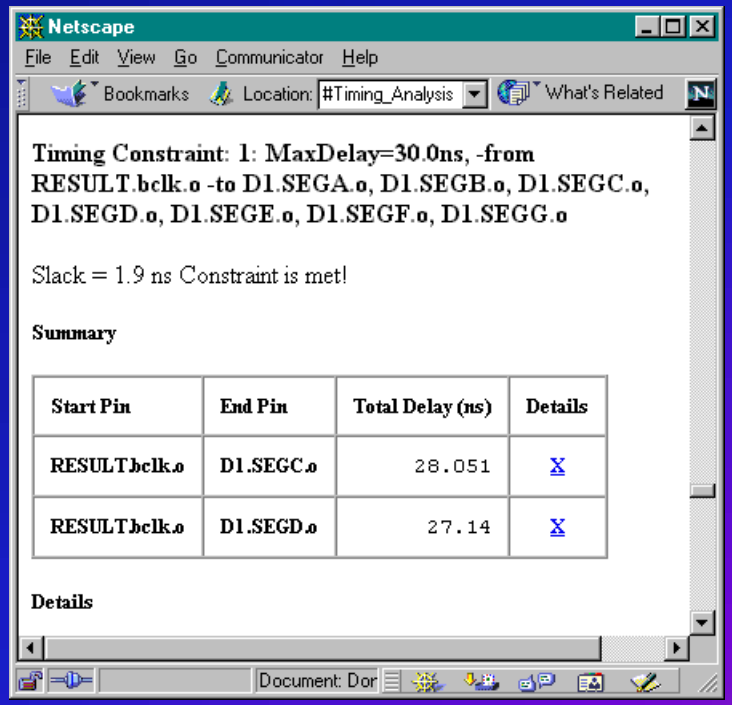
See the Results

- Run Bind
  - Use Timing-Driven mode
  - Specify *.tic constraints file
- Generate Project Report
- Click on Timing Analysis



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More on Constraints

- Limited information in online Help
- FastChip_Constraint_Files.pdf in \Docs directory
  - Address constraints
  - Timing constraints
- Somewhat useful today
- Difficult to use today
- May not cover all paths
- May include paths you don’t care about

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Obtaining Project Information

- Generate Project Report
  - CSL utilization
  - Modules used
  - Connectivity
  - I/O Pinout
  - Address Assignments
  - Timing Analysis (Lite)

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Export for Simulation

- Entire design
  - Requires Triscend Bus Functional Model (BFM) to simulate CSI bus traffic
  - More on BFM on Friday
- Individual module
  - Includes parameterization
- Supports popular simulation netlists
  - Verilog
  - VHDL/Vital
  - Can include post-Bind timing

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FastChip Device Link (FDL)

- Separate executable from FastChip
- Create a CSoC configuration image
  - CSL personality (Bind bitstream, *.csl)
  - Compiled processor code (.Hex)
  - Output to Triscend *.cfg or standard .Hex file
- Download
- Debug
  - Any memory-mapped register (CPU, Selector, RAM)
  - CSL logic nodes

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Why a Separate FDL?

- FastChip 1999 required entire project for download
  - Required high-end machine in lab
  - Exposed entire project
- FDL offers …
  - Design security, just ship *.csl or *.hex file
  - Lower system requirements in lab
  - Enhanced debugging interface
  - Low-resource command-line interface

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More of FDL

- Debugger uses file created by Bind
  - Cross-reference file (*.xref)
  - Memory address for resources in the design
- FDL Configuration creates its own report file
  - Configuration report file (*.cfr)
  - MIU and configuration register settings
  - Very useful for E5

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FDL Exercises

- Create a configuration image for internal SRAM
- Download to internal RAM
- Monitor and control registers and internal resources
- Set breakpoints

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FastChip Import

- Allows customer to create custom CSL logic using 3rd party tools
  - Schematics: OrCAD, ViewDraw
  - Synthesis: FPGA Express, Synplicity
- Import Heartbeat module and complete new project
  - Place on pin 103
  - Bind
  - Configure for Flash
  - Download to Flash

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Yahoo!

- Your board should now show an incrementing value on the LED!
- Save this design for tomorrow's training!

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