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Special Report: PC-based data acquisition systems

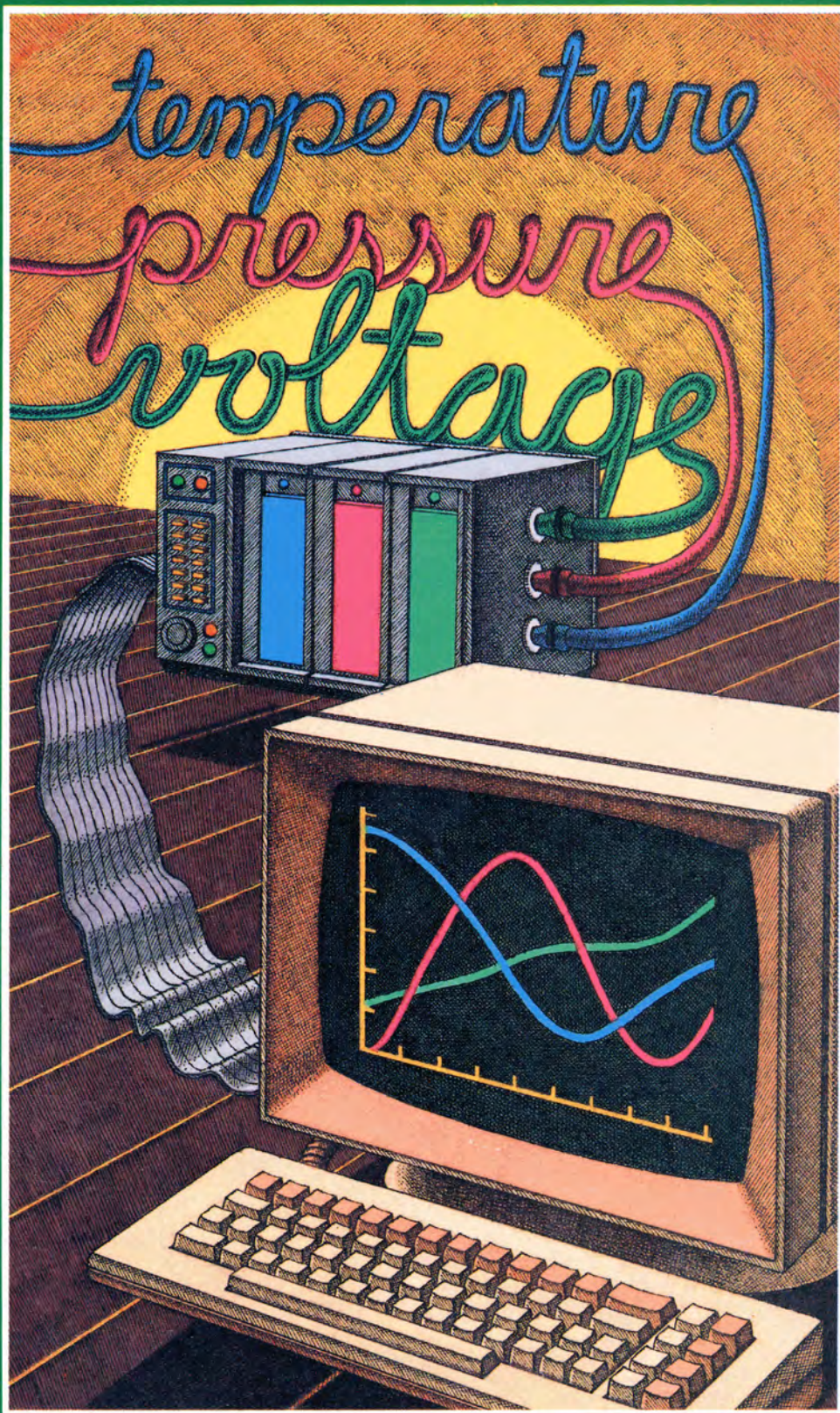
Product Probing:

- Voltage regulator ICs
- Alphanumeric displays
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Directory of dynamic RAMs

Application solutions:

Selecting portable scopes, building an ADC with a DAC, refining logic analysis, and designing bubble memory boards



Once a difficult task, bubble memory design is now a question of layout

Bubble memory is no longer cloaked with mystery. Board designers can get top reliability simply by focusing on the interaction among the subsystem's various signals.

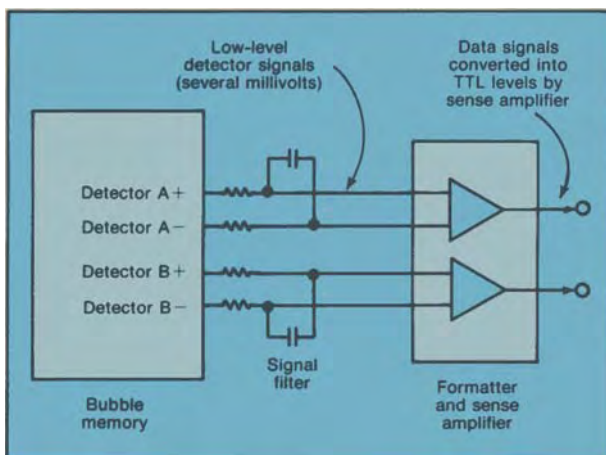
The characteristics of magnetic bubble memories suit them to a wealth of demanding applications, especially systems that demand consistent and maintenance-free operation. Their solid-state nature boosts system reliability, as it makes them resistant to shock and vibration and virtually immune to airborne particles, the primary sources of failures in tapes and disks. Add to those traits the compact size of bubbles, as well as their operation at extreme temperatures, -40° to $+85^{\circ}\text{C}$ and soon -55° to $+85^{\circ}\text{C}$. Magnetic technology guarantees permanent storage without batteries, and unlike other nonvolatile memories, they offer unlimited reading and writing.

Once difficult to add to a system, most bubble memories incorporate sophisticated support components that simplify the design of highly integrated nonvolatile storage systems. Subsystems of this sort present no limitations on size or structure, leaving system designers free to build a mass-storage system to their specifications.

Except for the memory controller, all parts in the subsystem are lumped together in a bubble storage unit. The design engineer need worry only about the interface between the controller and the host microprocessor. Fortunately, the interface resembles that

of any standard peripheral controller, for instance, one for a floppy disk or for direct memory access. The electrical connections between the controller and the bubble storage unit are the responsibility of the memory maker, since that section remains virtually unchanged from system to system (see "Dissecting the System," p.159).

Although the designer may be free from many of the customary interface headaches, the board layout of a bubble memory system still requires careful consideration. The most critical concerns revolve around the placement and width of the traces between the bubble detector and the sense amplifier. The signals,



1. The low-level detector signal paths should be as short as possible. This minimizes signal loss and also reduces noise received from higher-level signal paths nearby. The differential output of the detector and inputs to the amplifier also reduces noise.

Steven Knapp, Intel Corp.

Steven K. Knapp is the application engineer for Intel's military bubble memory component systems. Before joining Intel, he worked as a researcher at MIT's Lincoln Laboratory. He holds a BS from MIT.

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several millivolts in amplitude, must be protected from noise. The detector lines carry low-level data signals to the sense amplifier, which determines their binary state and converts them into TTL-level signals. Reducing spurious noise on the detector's traces reduces the risk of generating erroneous data.

Some simple rules can help designers isolate the detector's low-level signals from the coil driver's high-current switching transients. First, the connections between the detector's outputs and the sense amplifier's inputs should be as short and direct as possible. Long signal traces respond like antennas, receiving noise from higher-level signal paths. A shorter path also prevents any significant signal loss. The detector's differential output pair, serving as the input to the sense amplifier (Fig. 1), further reduces noise. And since each output is a differential pair, these signal traces should be about the same length, so that both sides of the signal path have balanced resistance.

Second, digital logic signals must never cross or encroach on the detector traces. The low amplitude of the detector lines means that a high-speed logic line could easily induce noise and cause data errors if the two are laid out too closely. Consequently, the designer should avoid running digital logic signals parallel to the detector traces on the circuit board. In all cases, a 0.5-in. separation should be maintained between these lines. Even in multilayer designs, logic traces should not run below the detector traces.

Third, the input traces to the X and Y coil drivers

should not only be separate from the detector signals but also should be kept as short as possible. These high-current drive lines switch at frequencies up to 100 kHz. By keeping these signals apart from the detector's outputs, the designer can eliminate much of the switching noise appearing on those outputs.

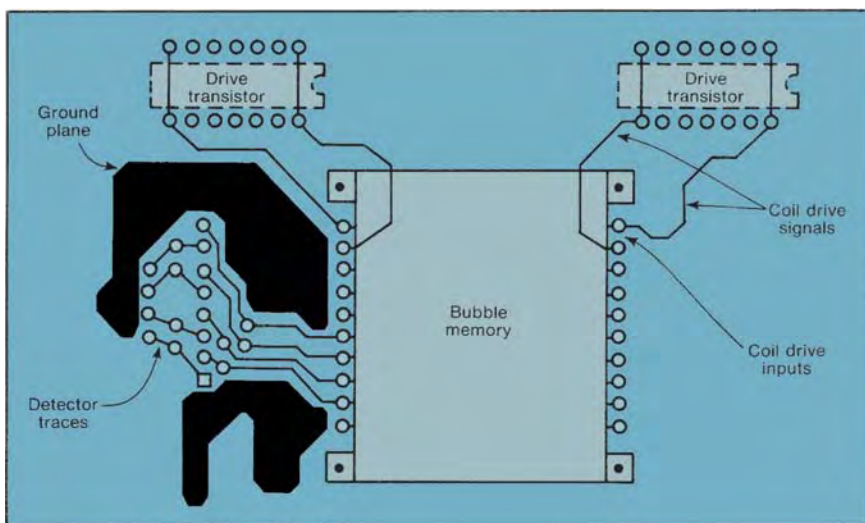
As for shortening the input traces, placing the drivers near the memory's coil input pins is the best method. In addition, with their large currents, the coil drivers should have wide conductor lines, at least 0.1 to 0.2 in. Last, by having the coil drive signals form a loop of minimum enclosed area, the transmitted noise falls further (Fig. 2).

Shielding against noise

Overall, most noise problems can be solved by electrically isolating the detector's small output signals from the rest of the system. Ground shielding around the detector traces usually does the trick.

To create a ground plane between the bubble memory and the sense amplifier, the designer has a choice of techniques, depending on whether a multilayer or a two-layer circuit board is being used. A multilayer board is generally recommended for bubble memory designs, since it proves more reliable for two or more bubble memories. A two-layer board, on the other hand, is better suited to single-bubble systems, which have a less complicated trace layout than a multibubble system.

With a two-layer board, one layer should be dedicated to routing the detector lines, and the second



2. The coil drive signals should be routed in a loop as near the drive inputs to the bubble memory and as far away from the detector traces as possible to reduce noise.

layer should be used as a local ground plane beneath those signals. Furthermore, the detector layer should have a ground plane surrounding the low-level detector signals (Fig. 3). The ground plane physically and electrically isolates the detector signals

from the other board.

An ideal structure, a four-layer circuit board, takes a different tack. By routing the detector traces in a ground plane sandwiched between other planes, a coaxiallike shield is formed around the low-level

Dissecting the system

Data within a bubble memory device is arranged serially in the form of loops. However, to aid in standard system design, a controller assimilates the serial data stream from a bubble memory and converts it into a byte-wide data path for the host processor.

Although the internal architecture of bubble memory renders the memory slower than RAM chips, it nevertheless makes it two to three times faster than a disk drive and thousands of times faster than a tape drive. Since individual data bits correspond to magnetic bubbles within a long, serial loop, read or write access times depend on bubbles traveling through the storage loop and on the serial input or output track required to write or read data.

The typical memory system, using 1 Mbit or 4 Mbit bubble memory devices, consists of a number of components: a controller, a current-pulse generator, a bubble detector, a formatter and sense amplifier, a coil predriver, X and Y coil drive transistors, and of course, the magnetic bubble memory (see the figure). Housing the unit is a relatively large IC package encased by a mu-metal shield.

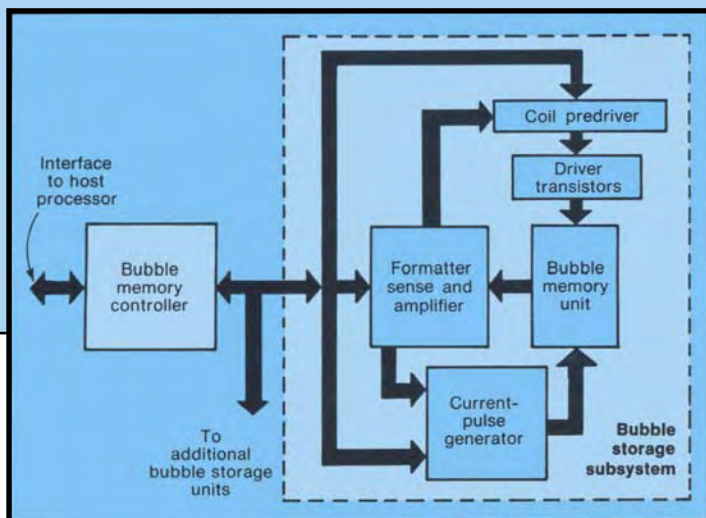
The controller, a VLSI chip, sets up a complete bidirectional interface between the host and the storage unit. Data from the subsystem is transferred in pages from the controller over a byte-wide data bus. Page sizes range from 32 to 64 bytes; as such, a page is similar to a disk drive's sector.

Since bubble memory is considered off-line bulk storage rather than on-line executable storage,

requested information is downloaded into executable storage through the controller. The controller requires a certain amount of its own software for proper operation; generally its code is about 500 bytes long. The controller, on receiving a command from the host processor, generates the proper timing and control signals for the subsystem's remaining support circuitry.

After the controller comes the current-pulse generator. Alternatively known as a function generator, this chip creates the precision current waveforms necessary for moving data into or out of the memory. To read the memory, a detector circuit within the memory unit must sense the magnetic bubbles. The formatter and sense amplifier chip then takes the low-level output signals of the detector and converts them into TTL-level signals. It also initiates the generation of the magnetic bubbles and handles additional tasks like formatting data, correcting errors, and mapping the redundancy built into the bubble memory. (In some systems, the latter three jobs are assigned to the controller.)

The coil predriver circuit works in conjunction with the controller to generate direction signals for the X and Y coil drive transistors. Both drivers act like analog switches that produce the high-current drive waveforms, usually 50 to 100 kHz. When the phrases of those waveforms are combined, the signals create a rotating magnetic field as they pass through the internal coils. In this manner, the data within the memory can be accessed and rotated.



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signals (Fig. 4). In some designs, that method may consume too much space and time. As a remedy, one of the dc power planes can serve as a shield plane. If the power supply has sufficient capacity, the dc power plane resembles an ac ground plane.

Some precautions should be taken about the ground planes, regardless of the number of board layers. A designer must take care that components not involved in the bubble detection mechanism (parts other than the bubble memory and the formatter-sense amplifier) do not share a branch with the localized ground planes. Problems can arise in the detector traces if a ground return path from a noisy component flows through the local detector ground shield.

After completing the board's layout, the designer should move on to the power system. The bubble memory subsystem typically requires only two dc operating voltages: +5 V and +12 V. If cost-consciousness rules the design, engineers should skimp anywhere but here. A high-quality power supply goes a long way toward maintaining the reliability of the memory system.

Safeguards against loss in supply voltage are particularly important. In some cases the power supply itself generates a TTL-level signal indicating that dc power is about to go down. In addition, all nonvolatile memory systems have a power-fail circuit that protects information during power transitions. With bubble memory, in particular, the power-fail circuit must ensure that all housekeeping tasks are completed before system power goes down. Moreover, it guarantees that no extraneous data is entered before

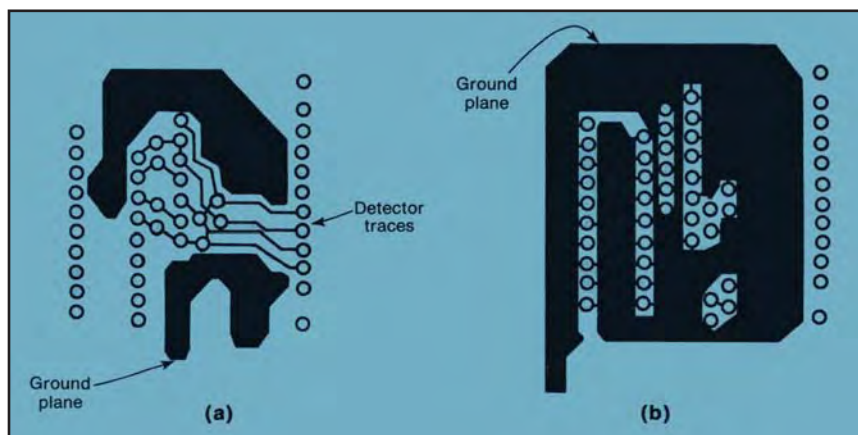
the support components are ready for power-up. Otherwise, the memory contents could get "scrambled."

To give the power-fail circuit enough time to complete its task, the supply's maximum power decay rate, as specified by the memory manufacturer, must allow support components to shut down the system in an orderly fashion once a power failure is imminent, thereby keeping data intact. If the power decays too quickly, the support circuits will not get enough power to shut down correctly. The power-fail circuit uses the internal capacitance of the power supply to deliver the requisite power. Most times, the internal capacitance is large enough to satisfy the decay rate specification.

Specifying the supply

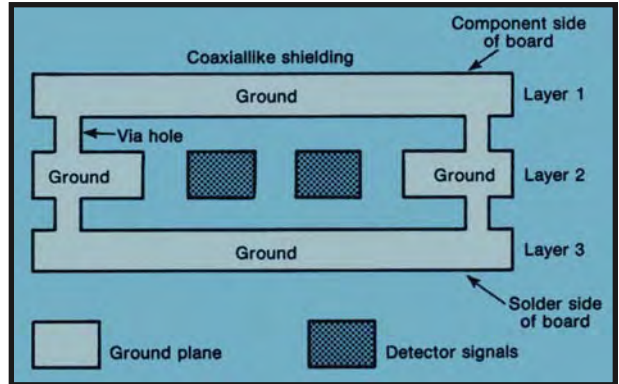
An overvoltage protection circuit—also called a crowbar—can have a bad effect on power decay. In a crowbar supply, an overvoltage condition triggers a silicon controlled rectifier, which almost instantly pulls down the supply low enough to prevent component damage. The protection circuit, if triggered, can violate the power decay specification and lead to potential data loss. Therefore, overvoltage protection measures must be eliminated or at least prevented until the bubble memory's circuitry has shut down the system in an orderly manner. Since a majority of crowbar conditions are caused unnecessarily by noise and voltage spikes on the ac power line, these should be avoided. Adding filters to the ac line will prevent the overvoltage circuit from triggering.

Placing power capacitors around each of the drive transistors and around each bubble memory creates



3. Ground planes should surround detector tracer traces shielding them from noise. In this two-layer board the ground plane is much smaller on the solder side (a) than the component side (b).

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4. A cross sectional view of a multilayer board illustrates the coaxial-like shielding effect provided by the ground planes. A dc power plane can be substituted for a ground plane since it will act as ac ground.

a current reservoir. The drive coils can absorb current from that reservoir or dump current into it. Without these capacitors, board inductance and resistance can cause a voltage drop and a potential power-fail condition.

The power capacitors actually perform another function, too. The drive coils require an almost linear current ramp to drive the rotating magnetic field correctly. Even with the small amount of inductance (L) and resistance (R) on the board, the linear current ramp will take on the form of an LR current curve, thus driving the field incorrectly. Surrounding the bubble memory's coil driver with capacitors minimizes undetermined inductance and resistance from the circuit board.

Although the access times for a bubble memory may not seem challenging, clock tolerances are still important. The bubble memory controller provides all the critical timing and control signals. The chip, in turn, uses the system clock as a timing reference. That clock ensures that all system operations happen at the correct instance and in the proper sequence; an unstable clock can corrupt the integrity of the stored data. Further, the clock must start at its specified frequency and not in one of its overtones.

As with any system, the reliability of a bubble memory subsystem is directly proportional to the reliability of each element in the system.