A Configurable System-on-Chip Device Facilitates Customization and Reuse

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Agenda

• Embedded System Challenges
• Industry Trends
• The Next Logical Step: A Configurable System-on-Chip
• Technical Challenges
  – System communication, device structure
  – Debugging
  – Maintaining hardware/software design flows
• Summary/Questions
The Embedded System Challenge

COMPROMISE!

Time to Market
Performance
Cost
Size
Power
Features
Industry Trends

- Advanced process technologies enable cost-effective system-on-a-chip designs and multi-million-gate FPGAs
- ASIC/FPGA densities now outstrip the capabilities to easily verify a design
- Adaptability is a desirable attribute
- Integrating system logic (memory, CPU) is expensive in FPGA logic
The Next Logical Step ...

- Configurable System-on-Chip (CSoC)
  - Pre-verified processor sub-system
  - Embedded programmable logic

- Industry-Standard Processor
- Programmable Logic
- Dedicated High Speed System Bus
- Dedicated User Memory

Embedded System Applications:
- Telecom
- Datacom
- Internet Appliance
- Networking
- Wireless
- Mobile Internet
- High End Consumer
- Industrial Control
- Many Others
Configurable System-on-Chip

- Pre-verified, configurable system integrated on a single chip
- Leverages standard logic design and processor development tools
- Leverages the design advantages of both processors and programmable logic
- Fast time-to-market for embedded systems
- System-on-a-chip for the masses
Triscend E5 Configurable System-on-Chip

- Power Control
- Clock and Crystal Oscillator Control
- Power-On Reset
- Bus Arbiter

- Memory Interface Unit
- Address Mappers
- Two-channel DMA Controller
- JTAG Interface

- 8032 "Turbo" Microcontroller
- Configurable System Logic (CSL) Matrix

- Configurable System Interconnect (CSI) bus
- Two-channel DMA Controller
- Hardware Breakpoint Unit
- Byte-wide System RAM

- PIO

8051/52 Compatible
Configurable System-on-Chip Technical Challenges

• Communication between the system and programmable logic functions
  – Connecting to the data and address bus
  – Decoding/controlling bus transactions
  – Register intimacy
  – Debugging a system with both processor and programmable logic

• Maintain standard development flows
  – Leverage available compilers, debuggers
  – Leverage existing logic design tools
Two-Chip Solution: CPU+FPGA/ASIC

• I/Os between devices
  – Many pins required, even for basic 8-bit interface
  – Adds delay to critical path
  – Extra power consumption and EMI in two-chip solution

• Distributing address/data on-chip
  – Uses programmable interconnect
  – Adds delay to critical path
  – Variable delays in some architectures
  – Some devices provide bidirectional bussing

![Diagram of processor with I/O connections](image_url)
Triscend Approach: CSI Bus Socket
(Configurable System Interconnect)

- Distributes bus signals to embedded program-mable logic
- No I/O required
- Predictable, synchronous timing
- Forward compatible with future device families
- Contention-free bussing
- Wait-state control
- DMA access
- Integrated debugging
Selector

• Fast address decoding
  – Any address range
  – Access type
    • Code
    • Data
    • Special Function Register (SFR)

• Decode delay is constant (less than 5 ns after clock)
DMA Control Register
(alternate Selector function)

Configurable System Logic

DMA Control Register

DMA Channel 1

DMA Channel 0

REQSEL

ACKSEL

Request

Acknowledge

Request

Acknowledge
CSL Cell Structure

- CSL cell perform various functions
  - Logic
  - Arithmetic
  - Memory
  - Bus
  - Sequential

- Intimate connection to the CSI system bus

CSL Cell = LUT+FF
- **CSL** = Configurable System Logic
- **CSI** = Configurable System Interconnect
Configurable System-on-Chip Debugging Capabilities

Access to all address mapped and other key processor resources

Breakpoint unit snoops the internal bus, providing complex runtime control features

Commands from 3rd party debuggers translated to JTAG instructions

All sequential and combinatorial logic nodes have complete observability

8032 RAM
Test and Control
CSI Bus
Configurable System Logic
Triscend CSoC Design Flow

Triscend FastChip™
Development Software

System
Configuration

System Test
and Debug

Device
Programming

Program
Development

Instruction
Simulation

In-System
Debug

Designer’s
standard tool flow

Triscend Soft Module
Library

Source
Code Library

Capture or
Synthesis

Functional
Simulation

3rd Party
EDA Tools

Netlist

Program
Development Tools

Triscend CSoC Design Flow
FastChip Development System

“Soft” Module Library

Dedicated Resources

“Soft” peripherals dragged into CSL matrix

Resources Used Indicators
Summary

- Advanced process technologies enable Configurable System-on-Chip devices
- High-density, cost-effective, and flexible
- Ideal for fast time-to-market for embedded systems applications
- On-chip communication, development flow, and debugging were top development challenges
- More to come ...
# Comparing 8052-class MCUs

<table>
<thead>
<tr>
<th>Feature</th>
<th>Average 8052</th>
<th>Dallas 80C320</th>
<th>Philips XA-GA</th>
<th>Triscend E5</th>
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<tr>
<td>8051/8052 binary compatible</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Yes</td>
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<tr>
<td>Max. Frequency</td>
<td>24 MHz</td>
<td>33 MHz</td>
<td>30 MHz</td>
<td>40 MHz</td>
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<td>Instruction cycle (clocks)</td>
<td>12</td>
<td>4</td>
<td>3</td>
<td>4</td>
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<tr>
<td>16-bit Timer/Counters</td>
<td>3</td>
<td>3</td>
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<td>3+</td>
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<td>Watchdog Timer</td>
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<td>Yes</td>
<td>Yes</td>
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<tr>
<td>UARTs</td>
<td>1</td>
<td>2</td>
<td>2</td>
<td>1+</td>
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<td>Interrupts</td>
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<td>13</td>
<td>38</td>
<td>12+</td>
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<td>Data Pointers</td>
<td>1</td>
<td>2</td>
<td>-</td>
<td>2+</td>
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<td>Wait-state support</td>
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<td>Yes</td>
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<td>PIO pins</td>
<td>32</td>
<td>32</td>
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<td>60 to 316</td>
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<td>256</td>
<td>256</td>
<td>512</td>
<td>256</td>
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<td>On-chip MOVX RAM</td>
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<td>N/A</td>
<td>8K to 64K</td>
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<td>DMA channels</td>
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<td>Maximum address space</td>
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<td>1M/16M</td>
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<td>On-chip debug hardware</td>
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<td>Yes</td>
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Programmable I/O (PIO)

- Output Enable
- Output
- Input
- Registered Input
- Clock Enable
- Clock

Flip-flops in I/O pads for improved setup, clock-to-output performance

4 mA or 12 mA drive
3.3 V outputs, 5 V-tolerant

Optional pullup resistor, pulldown resistor, or bus follower

BusMinder™

Drive Strength

Input Hysteresis

Delay Zero Hold Time
Comparing Logic Capacity

LUT+FF Pairs

- Triscend CSL cell = 1 LUT4+FF pair
- Xilinx CLB = 2 LUT4+FF pair
- Altera FLEX LE = 1 LUT4+FF pair
- Atmel logic cell = 1 LUT4+FF pair