S211

A Configurable System-on-Chip Device Facilitates Customization and Reuse

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Agenda

- **Embedded System Challenges**
- **Industry Trends**
- **The Next Logical Step: A Configurable System-on-Chip**
- **Technical Challenges**
  - System communication, device structure
  - Debugging
  - Maintaining hardware/software design flows
- **Summary/Questions**

The Embedded System Challenge

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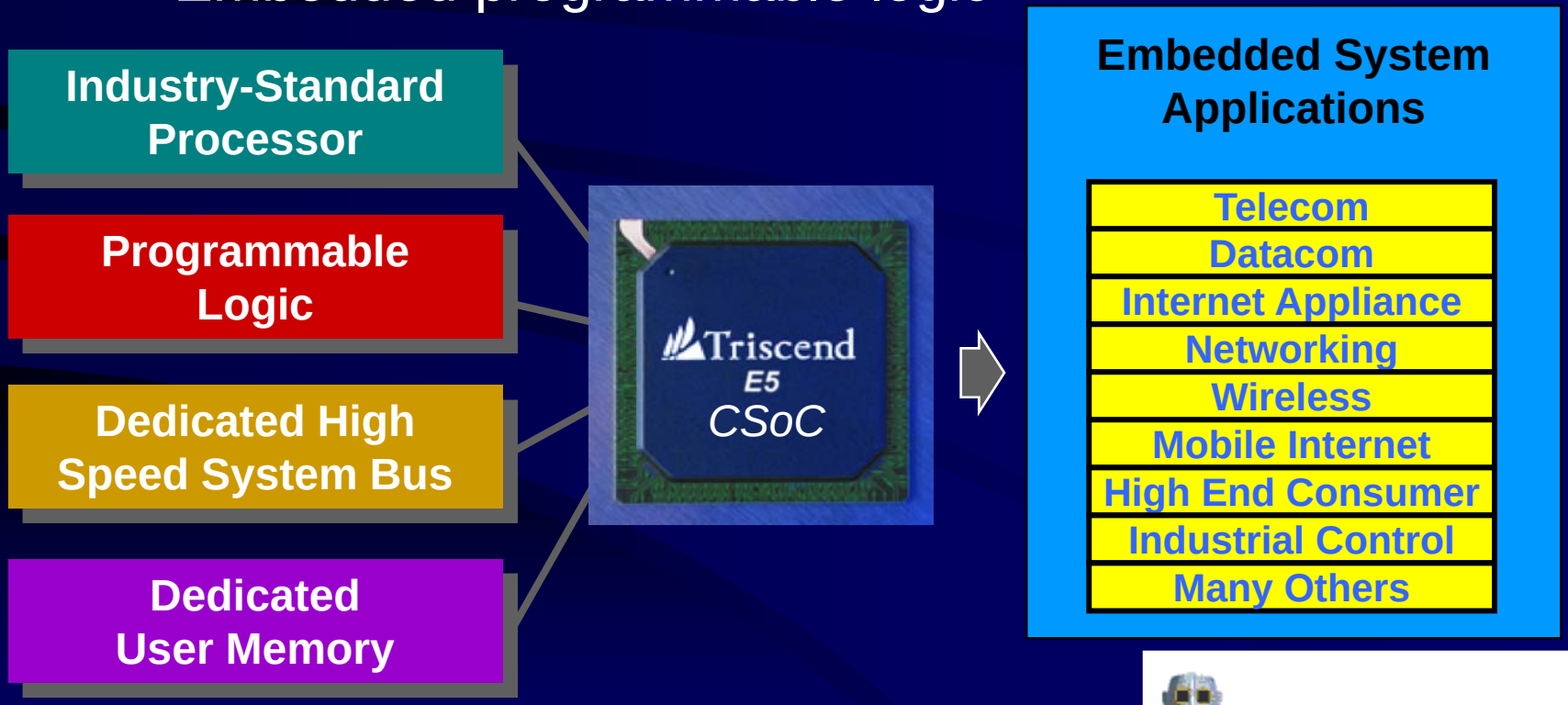
Industry Trends

- Advanced process technologies enable cost-effective system-on-a-chip designs and multi-million-gate FPGAs
- ASIC/FPGA densities now outstrip the capabilities to easily verify a design
- Adaptability is a desirable attribute
- Integrating system logic (memory, CPU) is expensive in FPGA logic

The Next Logical Step ...

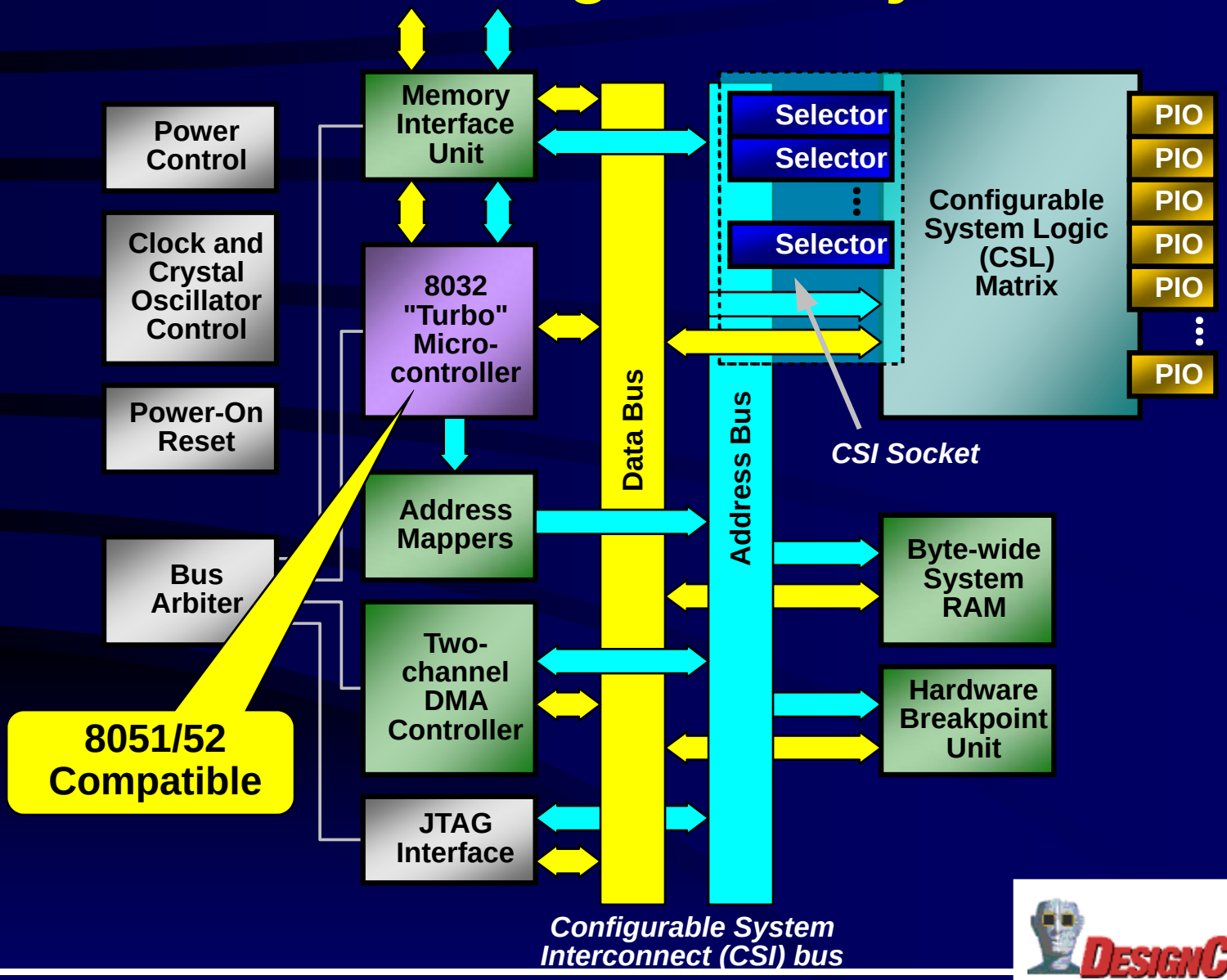
- **Configurable System-on-Chip (CSoC)**
  - Pre-verified processor sub-system
  - Embedded programmable logic



Configurable System-on-Chip

- Pre-verified, configurable system integrated on a single chip
- Leverages standard logic design and processor development tools
- Leverages the design advantages of both processors and programmable logic
- Fast time-to-market for embedded systems
- System-on-a-chip for the masses

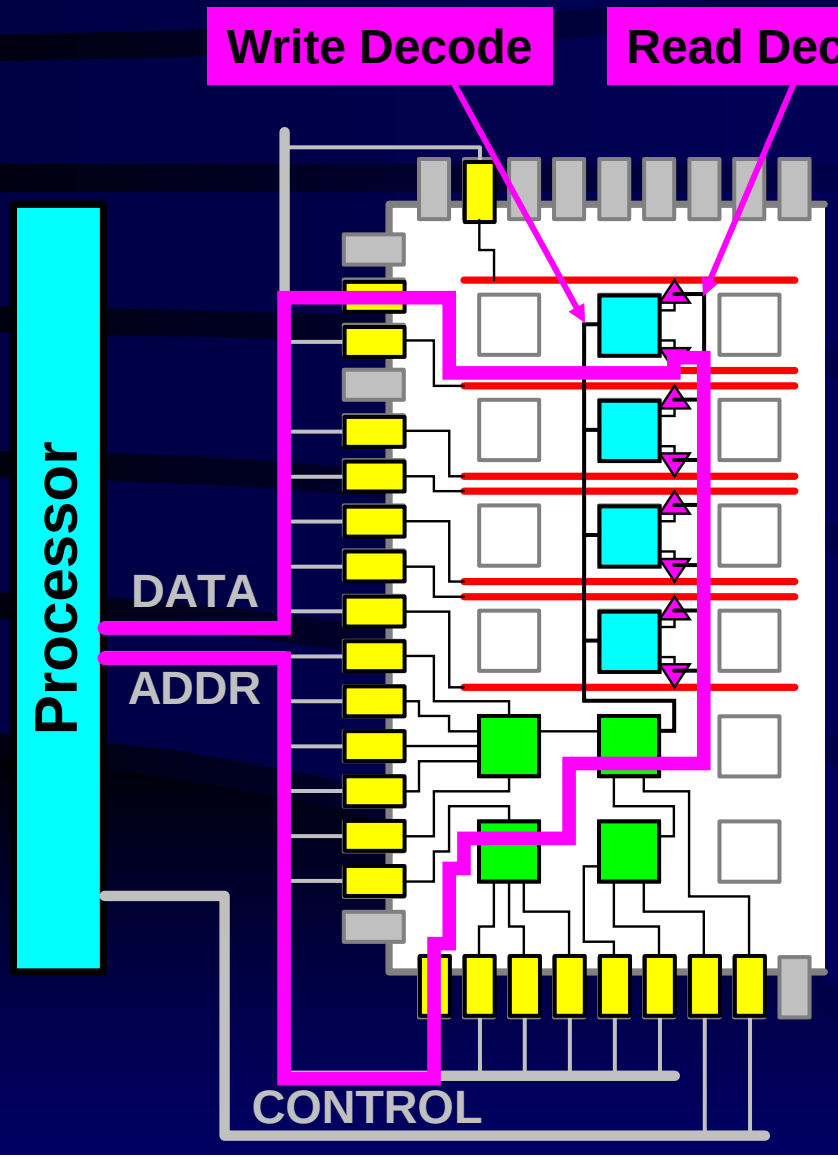
Triscend E5 Configurable System-on-Chip



Configurable System-on-Chip Technical Challenges

- Communication between the system and programmable logic functions
  - Connecting to the data and address bus
  - Decoding/controlling bus transactions
  - Register intimacy
  - Debugging a system with both processor and programmable logic
- Maintain standard development flows
  - Leverage available compilers, debuggers
  - Leverage existing logic design tools

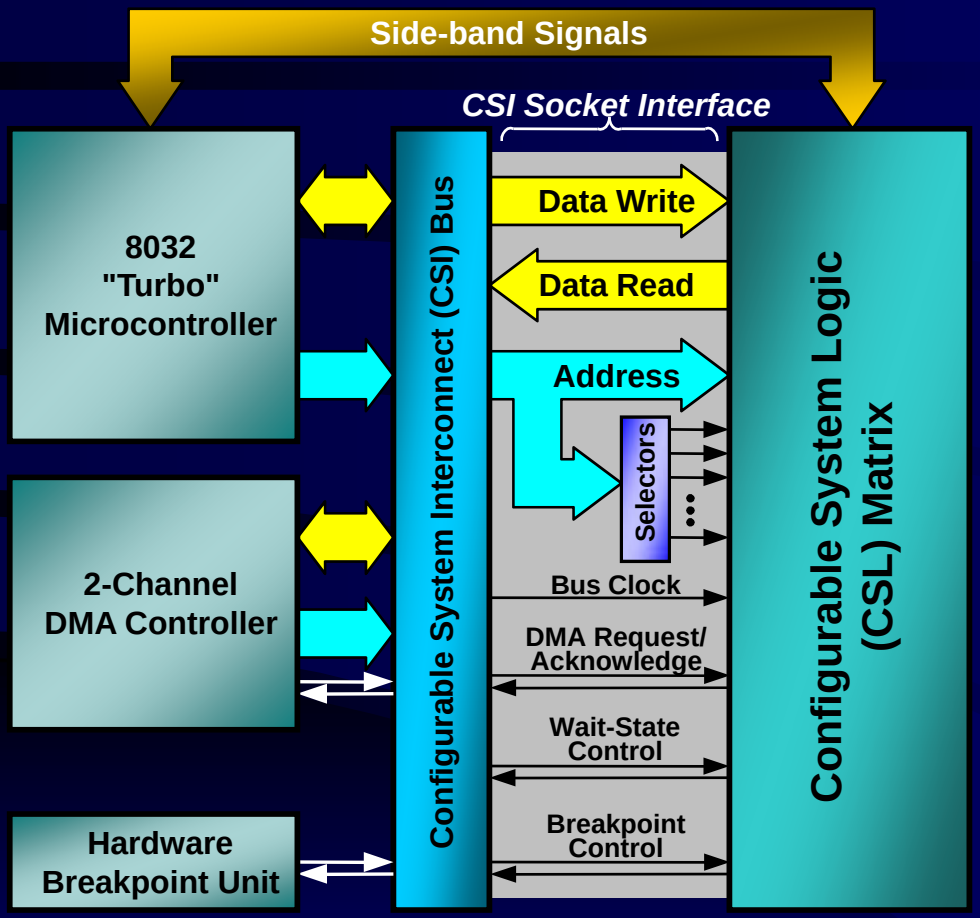
Two-Chip Solution: CPU+FPGA/ASIC



- **I/Os between devices**
  - Many pins required, even for basic 8-bit interface
  - Adds delay to critical path
  - Extra power consumption and EMI in two-chip solution
- **Distributing address/data on-chip**
  - Uses programmable interconnect
  - Adds delay to critical path
  - Variable delays in some architectures
  - Some devices provide bidirectional bussing

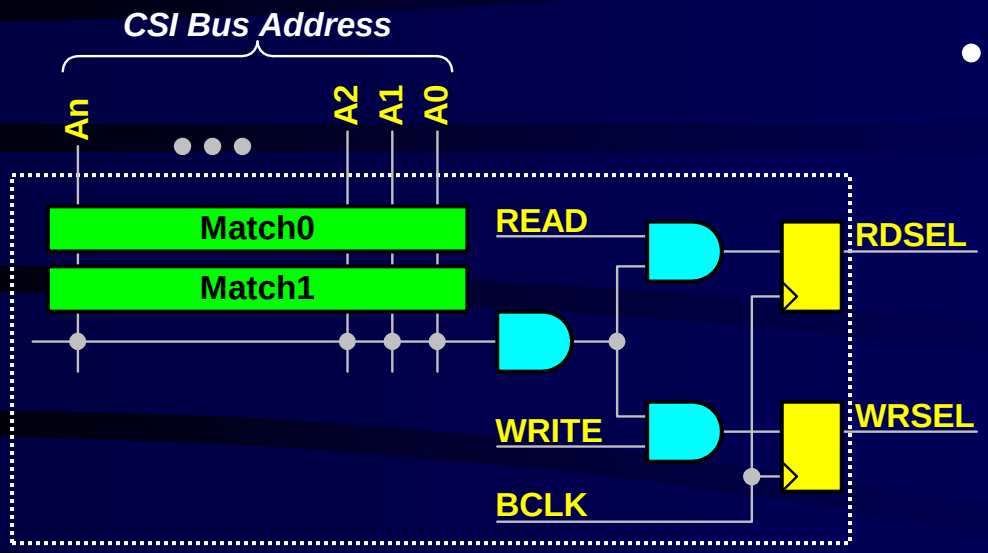
Triscend Approach: CSI Bus Socket

(Configurable System Interconnect)



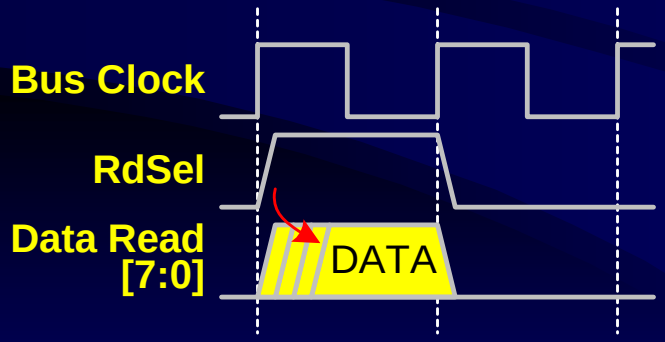
- Distributes bus signals to embedded program-mable logic
- No I/O required
- Predictable, synchronous timing
- Forward compatible with future device families
- Contention-free bussing
- Wait-state control
- DMA access
- Integrated debugging

Selector



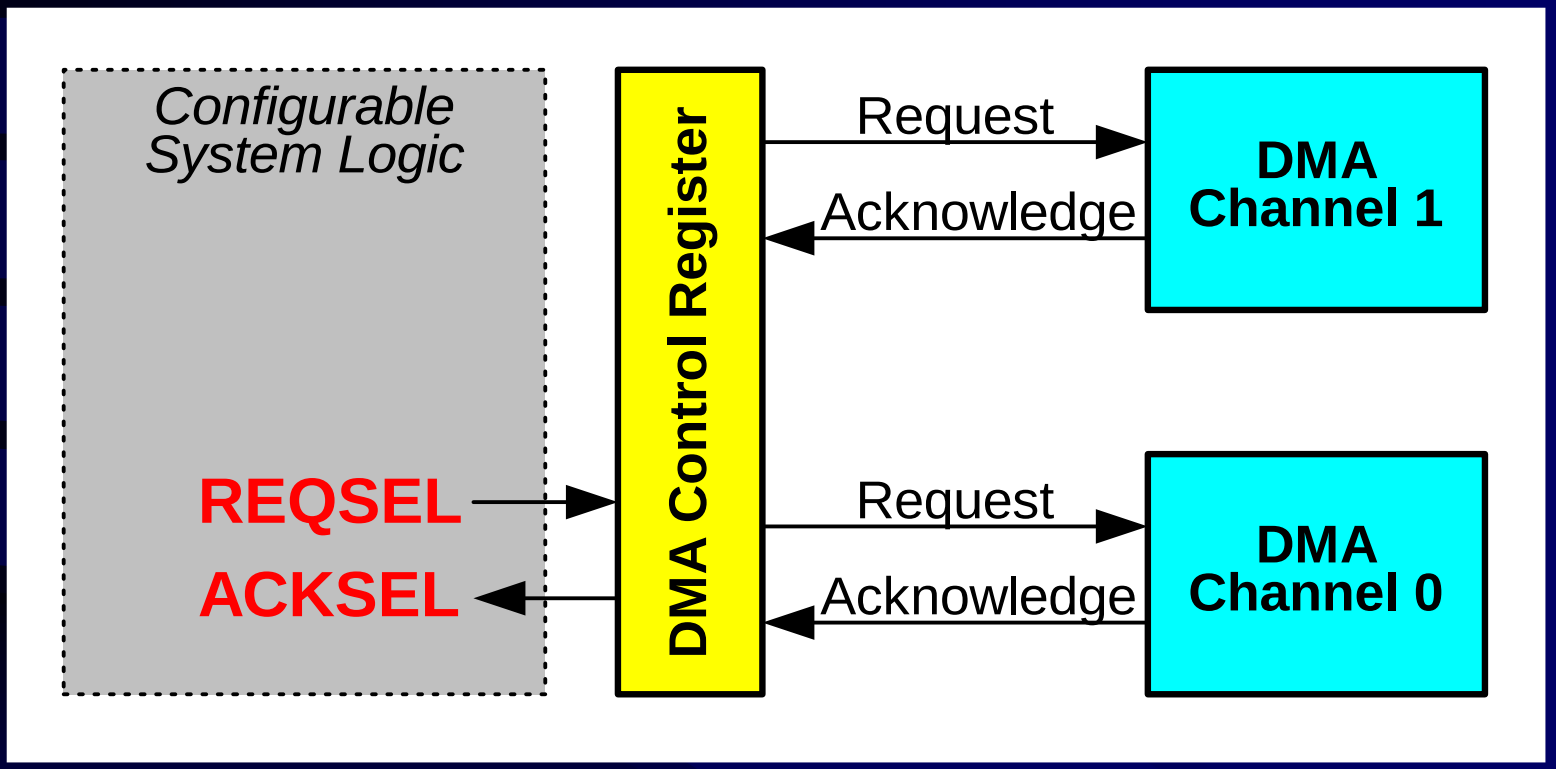
- **Fast address decoding**
  - Any address range
  - Access type
    - **Code**
    - **Data**
    - **Special Function Register (SFR)**

Device	Selectors
TE502	16
TE505	32
TE512	72
TE520	128
TE532	200

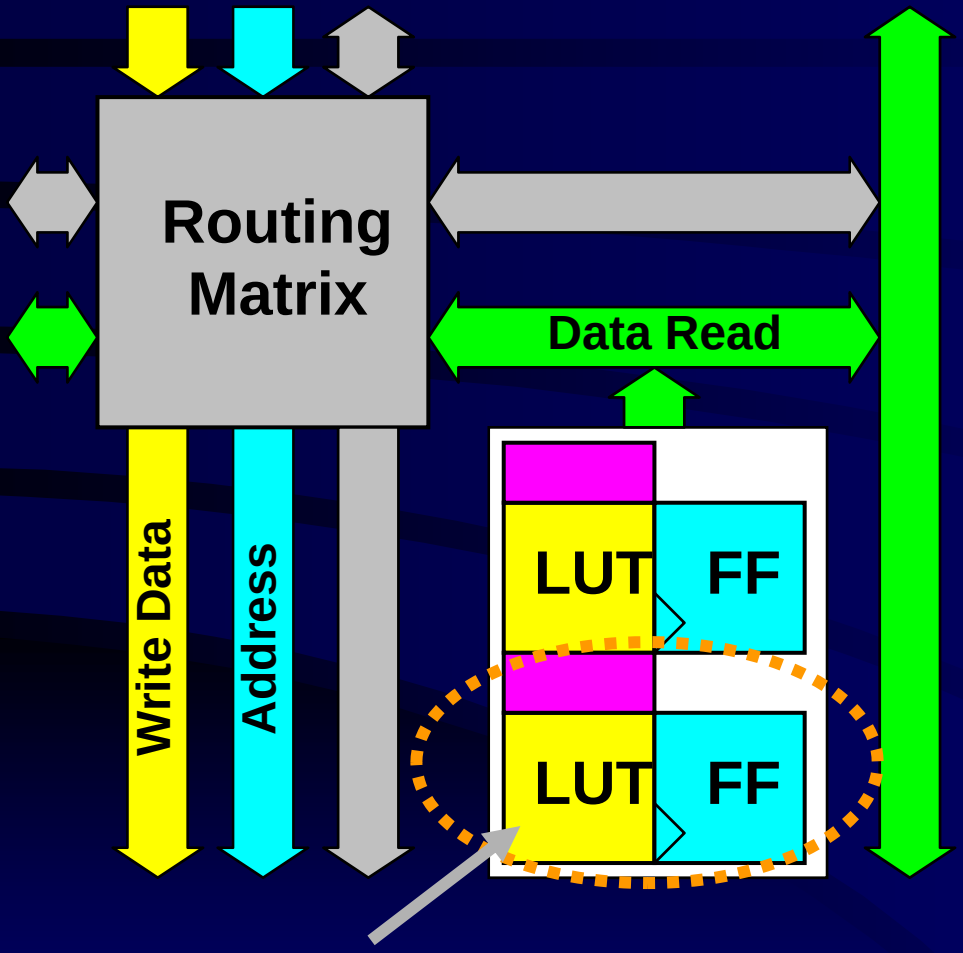


- **Decode delay is constant (less than 5 ns after clock)**

DMA Control Register (alternate Selector function)

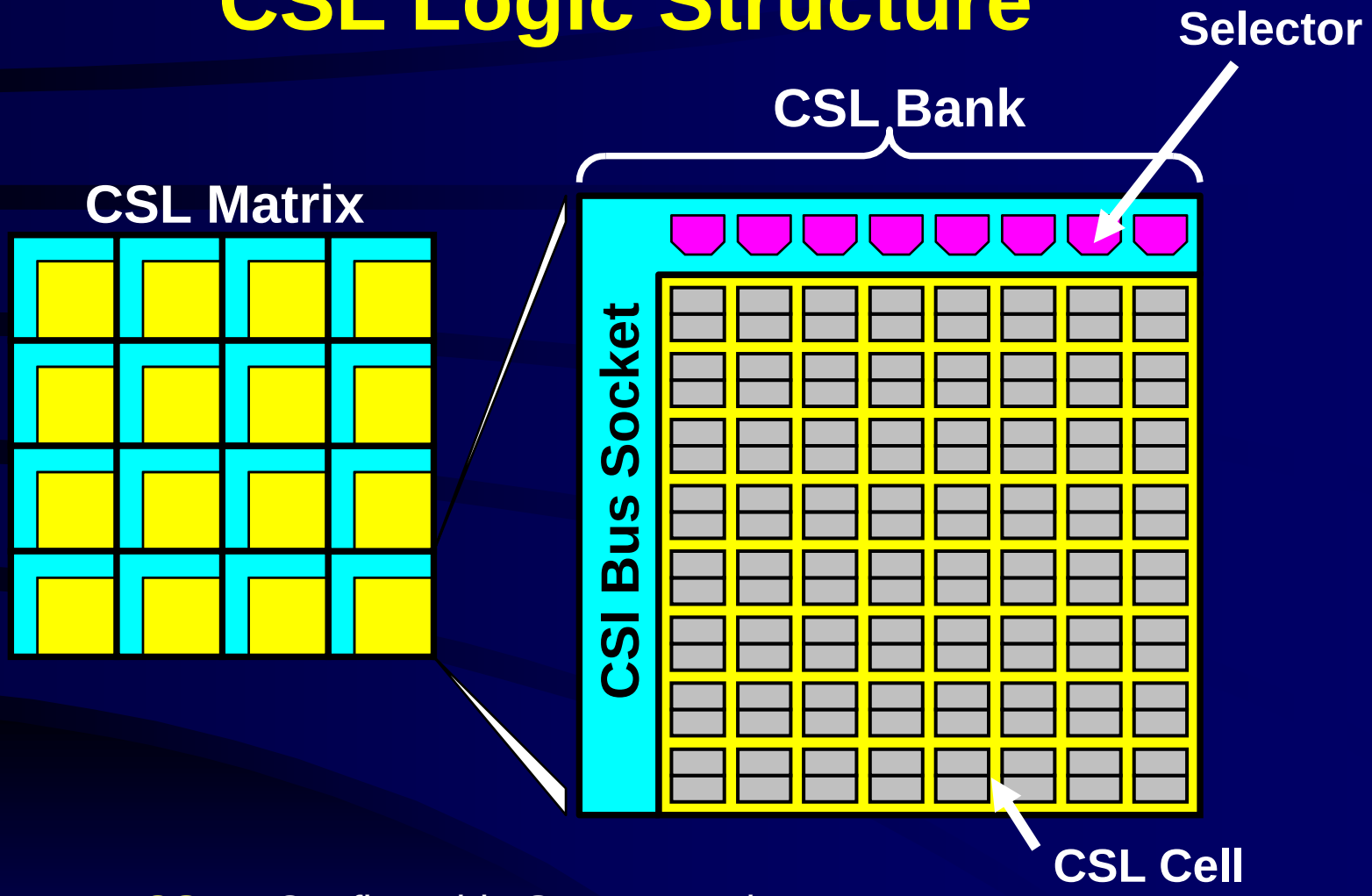


CSL Cell Structure



- **CSL cell perform various functions**
  - Logic
  - Arithmetic
  - Memory
  - Bus
  - Sequential
- **Intimate connection to the CSI system bus**

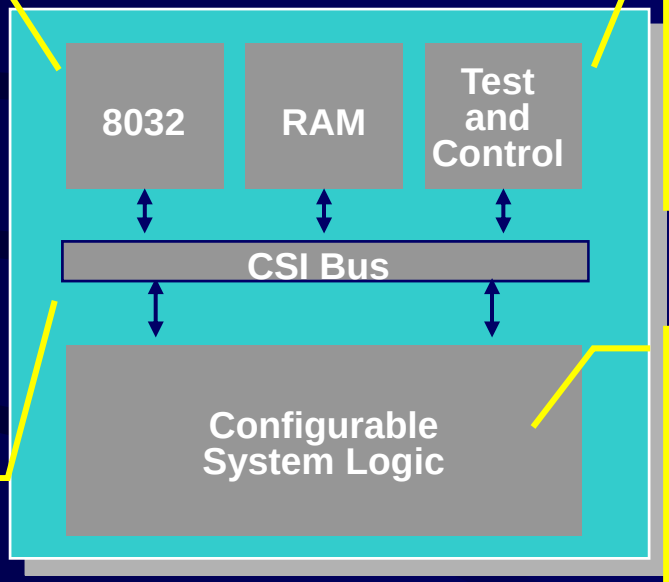
CSL Logic Structure



- **CSL** = Configurable System Logic
- **CSI** = Configurable System Interconnect

Configurable System-on-Chip Debugging Capabilities

Access to all address mapped and other key processor resources

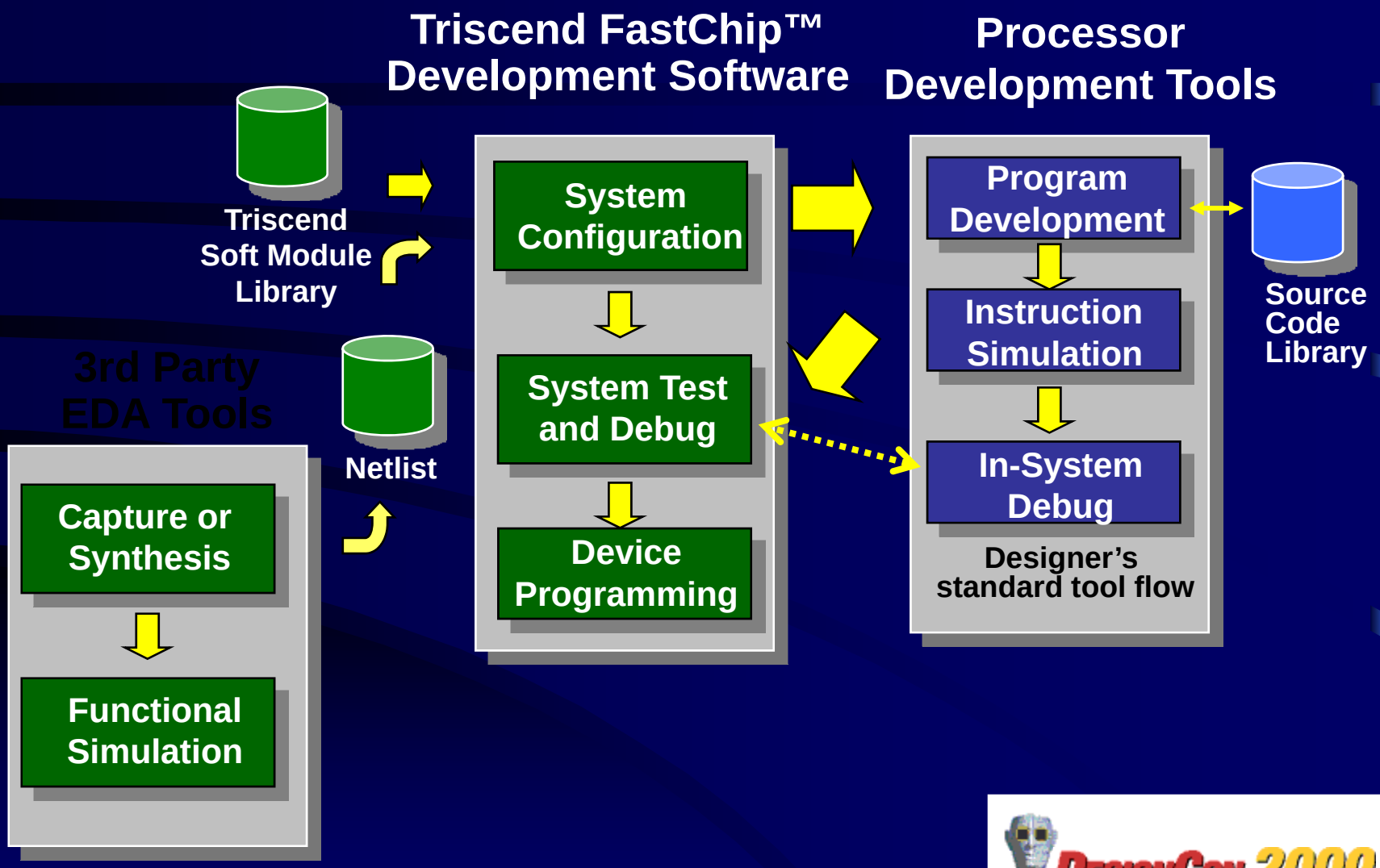


Commands from 3rd party debuggers translated to JTAG instructions

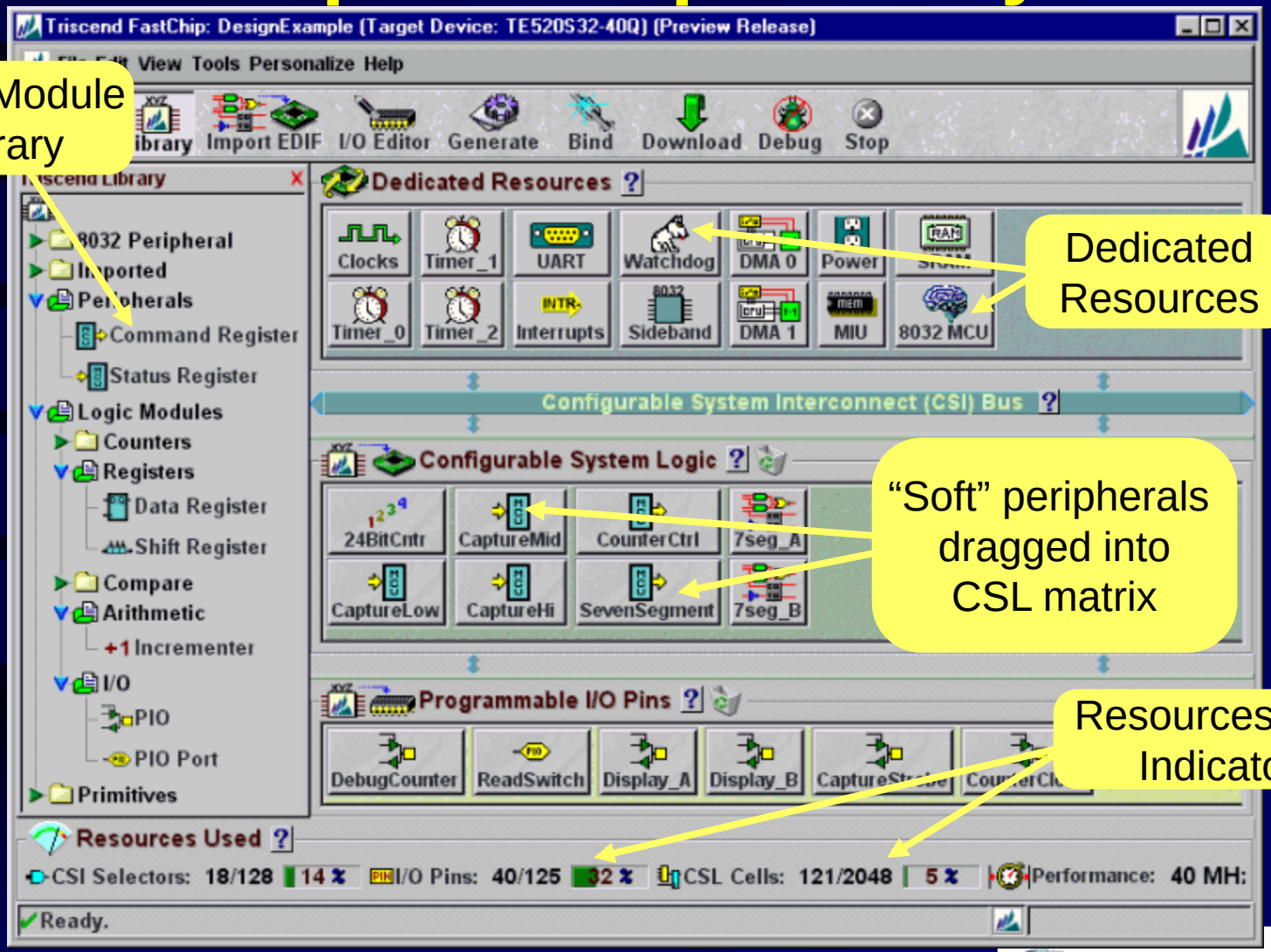
Breakpoint unit snoops the internal bus, providing complex runtime control features

All sequential and combinatorial logic nodes have complete observability

Triscend CSoC Design Flow



FastChip Development System



"Soft" Module Library

Dedicated Resources

"Soft" peripherals dragged into CSL matrix

Resources Used Indicators

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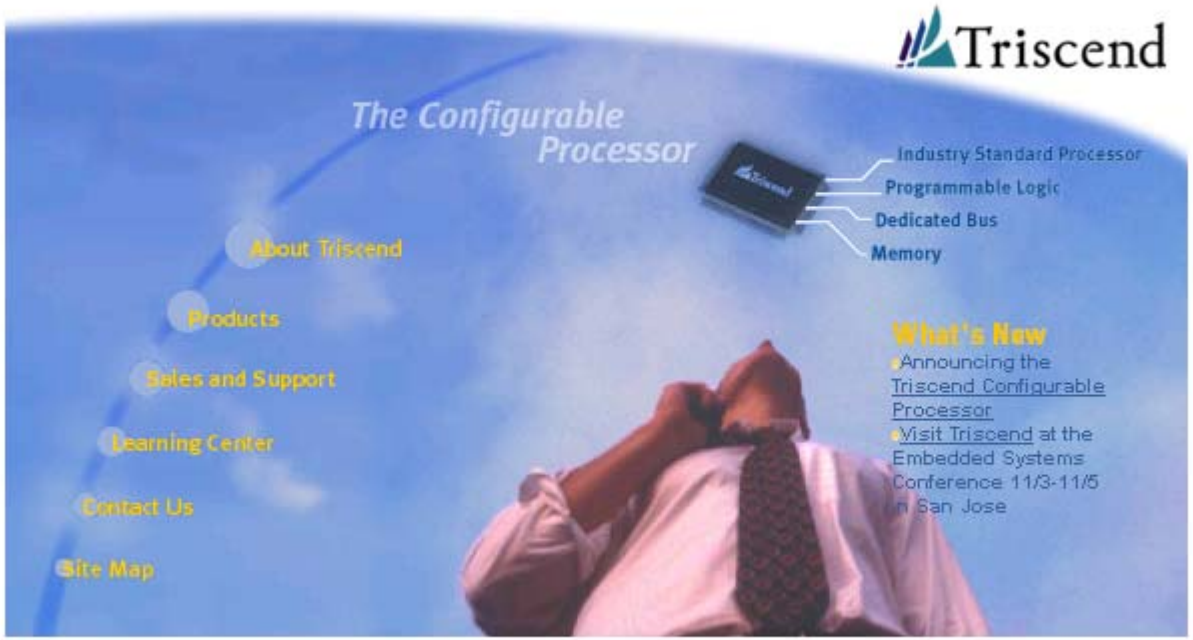
Summary

- Advanced process technologies enable Configurable System-on-Chip devices
- High-density, cost-effective, and flexible
- Ideal for fast time-to-market for embedded systems applications
- On-chip communication, development flow, and debugging were top development challenges
- More to come ...

For More Information



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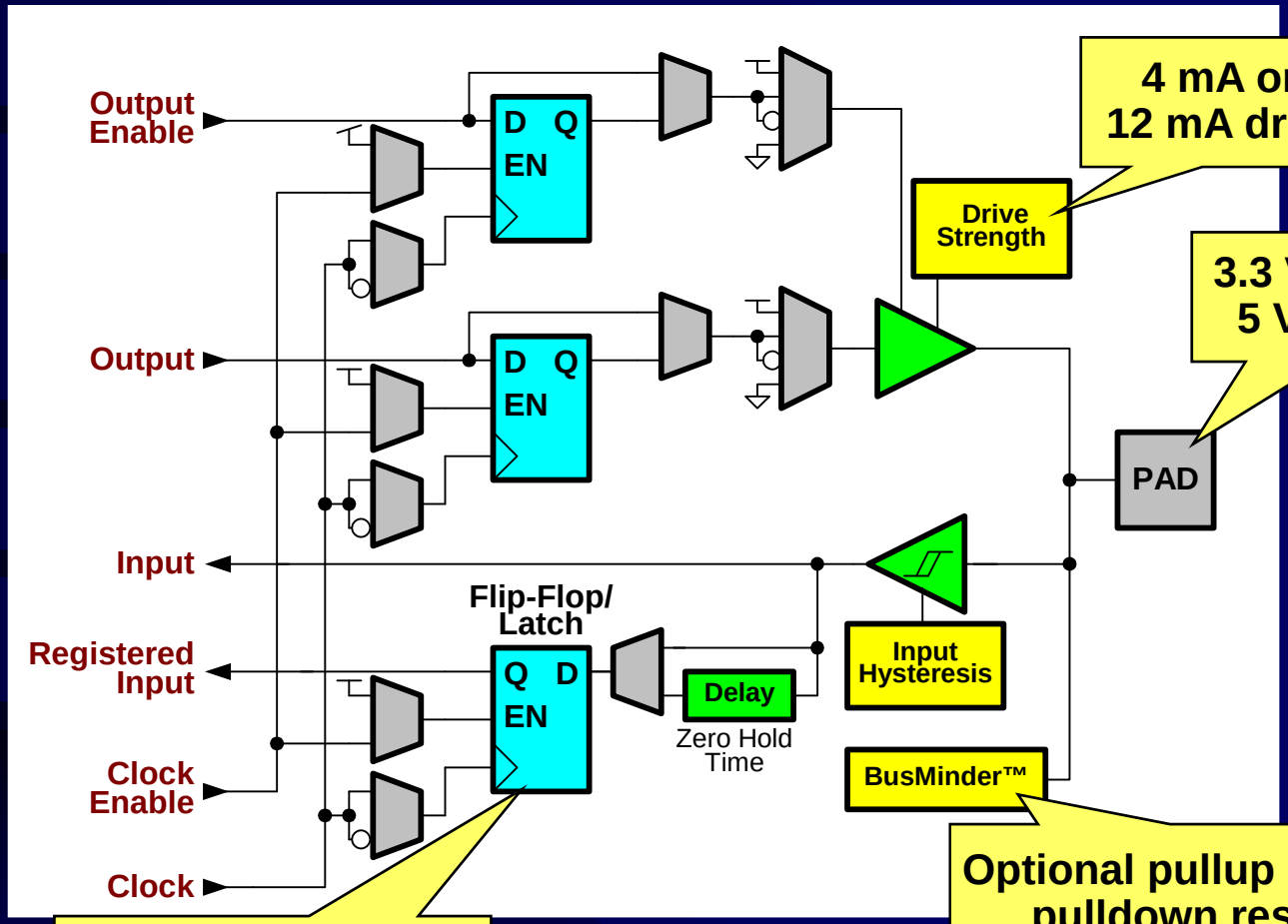
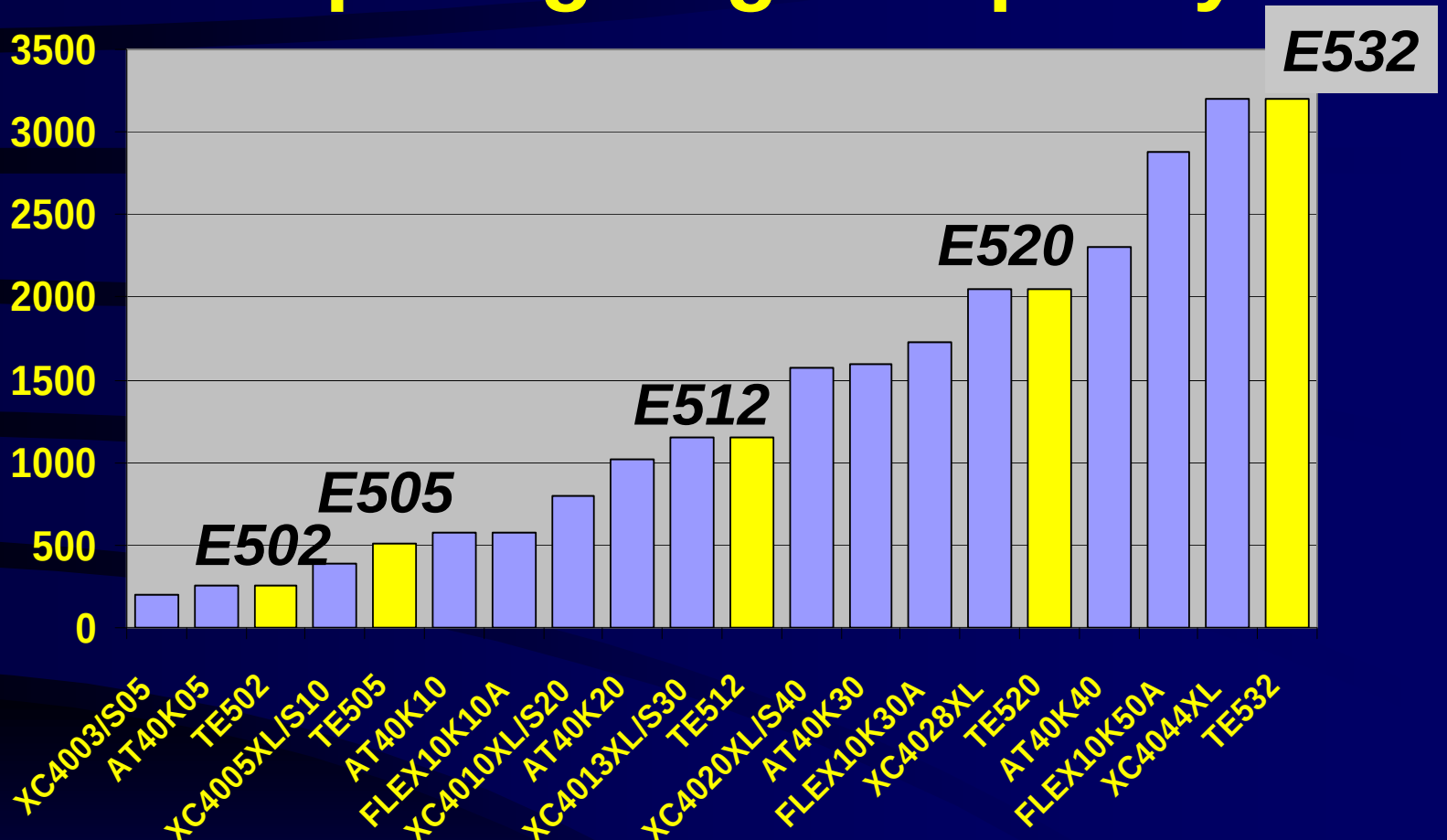
Comparing 8052-class MCUs

Feature	Average 8052	Dallas 80C320	Philips XA-GA	Triscend E5
8051/8052 binary compatible	Yes	Yes	No	Yes
Max. Frequency	24 MHz	33 MHz	30 MHz	40 MHz
Instruction cycle (clocks)	12	4	3	4
16-bit Timer/Counters	3	3	3	3+
Watchdog Timer	N/A	Yes	Yes	Yes
UARTs	1	2	2	1+
Interrupts	7	13	38	12+
Data Pointers	1	2	-	2
Wait-state support	N/A	N/A	Yes	Yes
PIO pins	32	32	32	60 to 316
On-chip internal RAM	256	256	512	256
On-chip MOVX RAM	N/A	N/A	N/A	8K to 64K
Glue-less memory interface	N/A	N/A	N/A	Yes
DMA channels	N/A	N/A	N/A	2
Maximum address space	64K	64K	1M/16M	64K/16M
On-chip debug hardware	N/A	N/A	Yes	Yes

Programmable I/O (PIO)



Comparing Logic Capacity



- Triscend CSL cell = 1 LUT4+FF pair
- Xilinx CLB = 2 LUT4+FF pair
- Altera FLEX LE = 1 LUT4+FF pair
- Atmel logic cell = 1 LUT4+FF pair