Class 330

Configurable Embedded Systems:
Using Programmable Logic to Compress Embedded System Design Cycles

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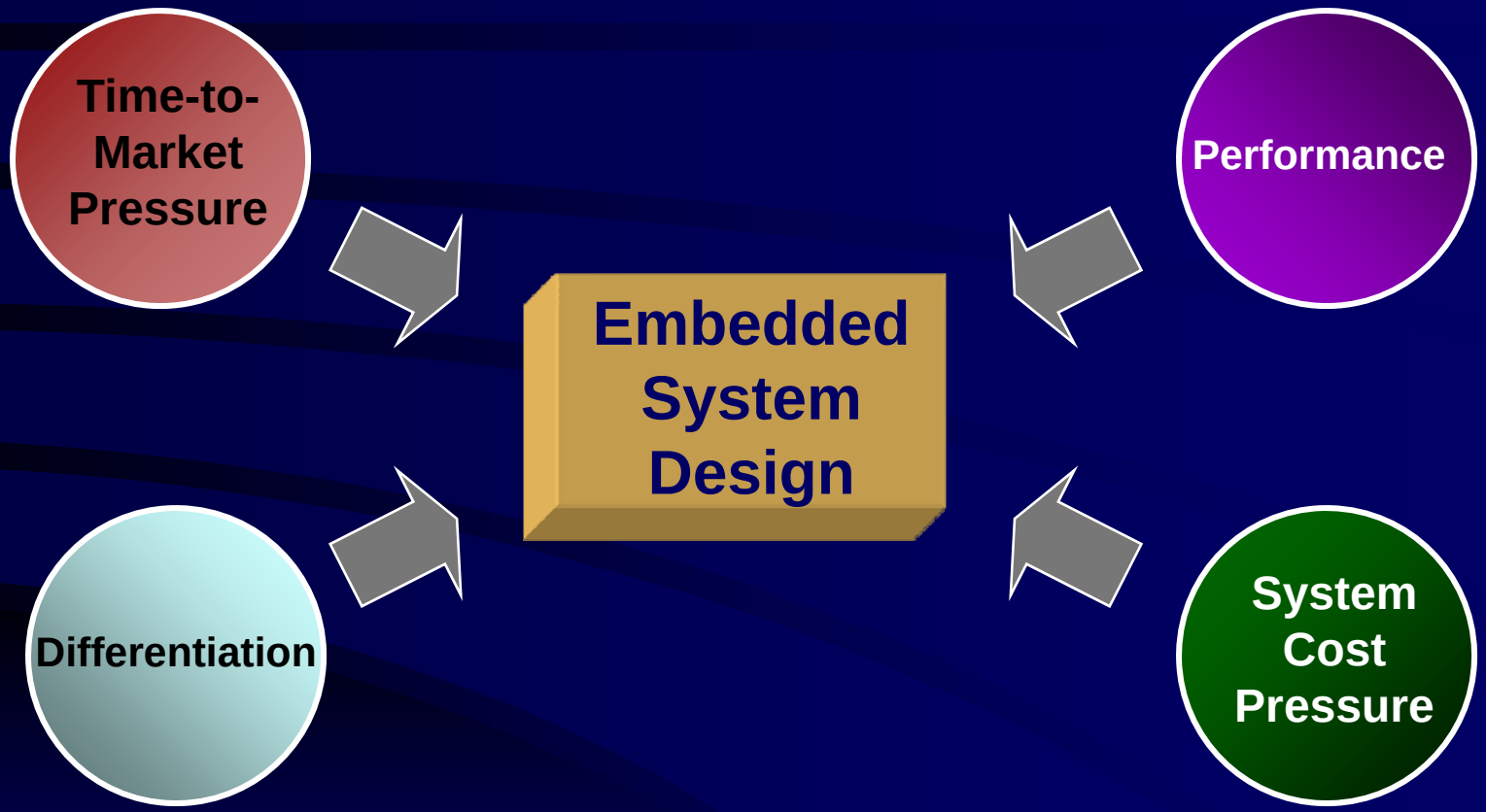
Agenda

- Forces Shaping Embedded Design
- Types of Design Solutions
- Programmable Technologies
- Technical Challenges

Key Forces Shaping Embedded Systems



Why 'Configurable'?

- Time-to-Market
  - Fast iterations
  - Fast in-system, real-time debugging
  - Fast component availability
- Adaptability
  - During design and debug
  - In the field
  - In the application
- Performance
  - Match the architecture to the problem
  - Fast response to real-time events
  - Parallel operations
- Increased Differentiation

Types of Design Solutions

- Stand-Alone Processor
- Processor Derivative
- Processor + ASIC
- Processor + Programmable Logic
- Custom Processor in Programmable Logic
- Custom Processor in ASIC
- Configurable Processor
- System on a Chip

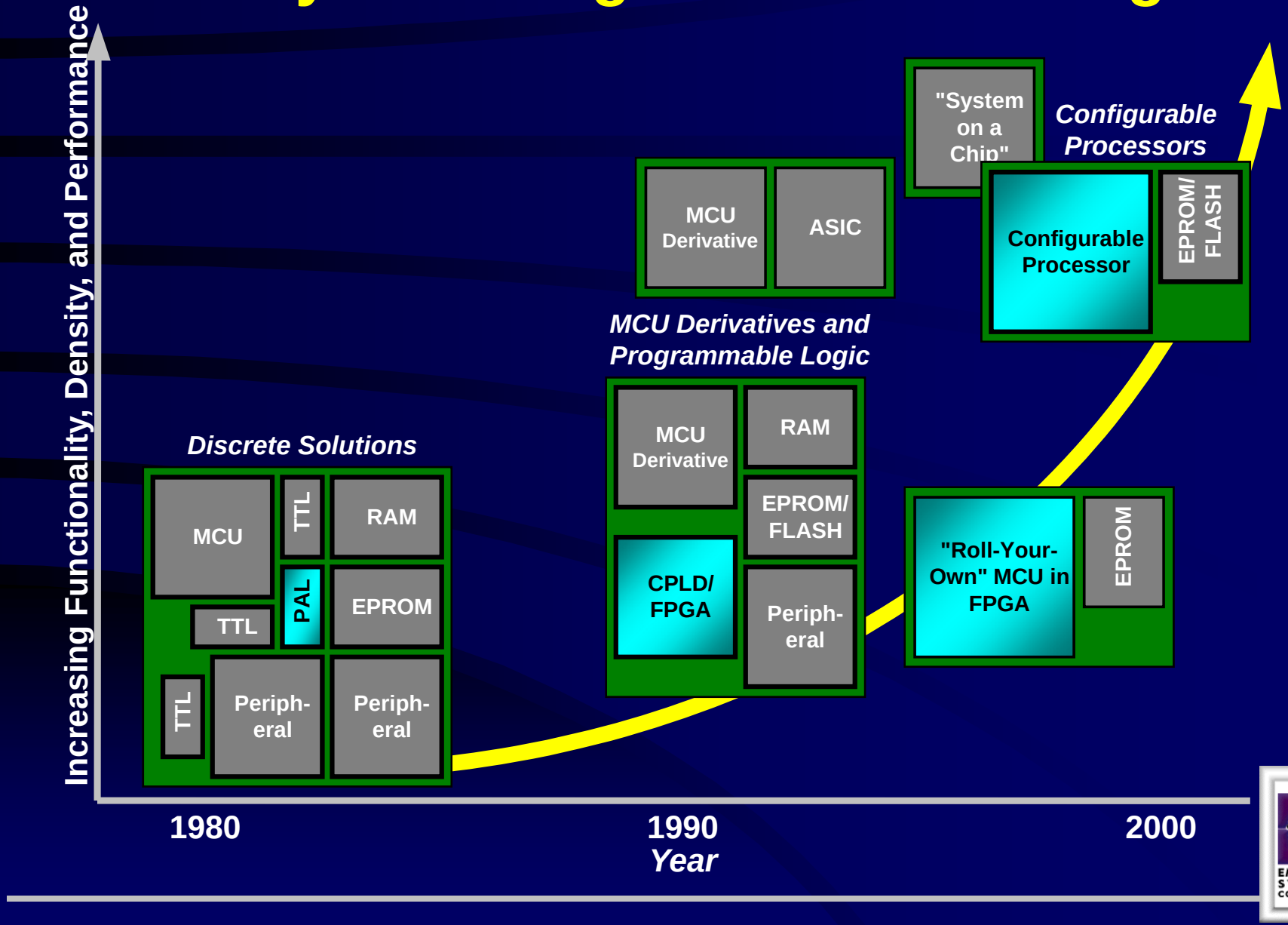
Embedded System Solutions

Hardware Customization	*Custom Logic*	*Configurable Logic (off the shelf)*
Instruction Set	System on a chip Processor + ASIC	“Roll your own” in FPGA Configurable processor (on-chip accelerator)
Peripheral Set. System Architecture	System on a chip Processor + ASIC	Processor + FPGA Configurable processor
I/O, Interface, Decoding	Processor + ASIC	Processor + CPLD/FPGA Configurable processor
None	-	Stand-alone processor or derivative

Highest Customization

Fast Time-to-Market

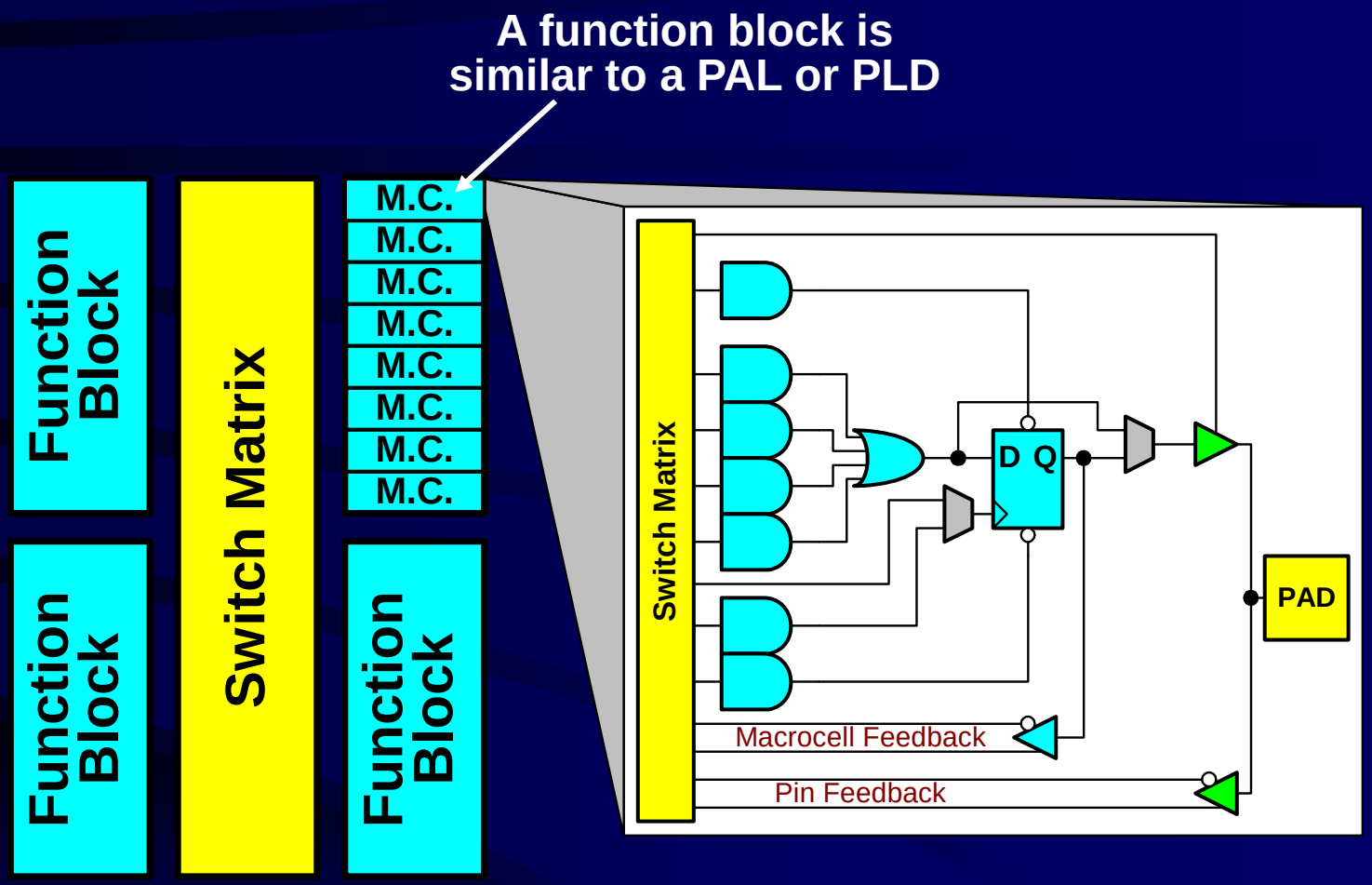
History of Configurable Technologies



Today's Configurable Technologies

- Complex Programmable Logic Devices (CPLD)
- Field Programmable Gate Arrays (FPGA)
- Hybrid Devices
  - Processor interface
  - Programmable logic
- Configurable Processors
  - Integrated processor
  - Programmable logic
  - Dedicated on-chip bus
  - On-chip memory

What is a CPLD?

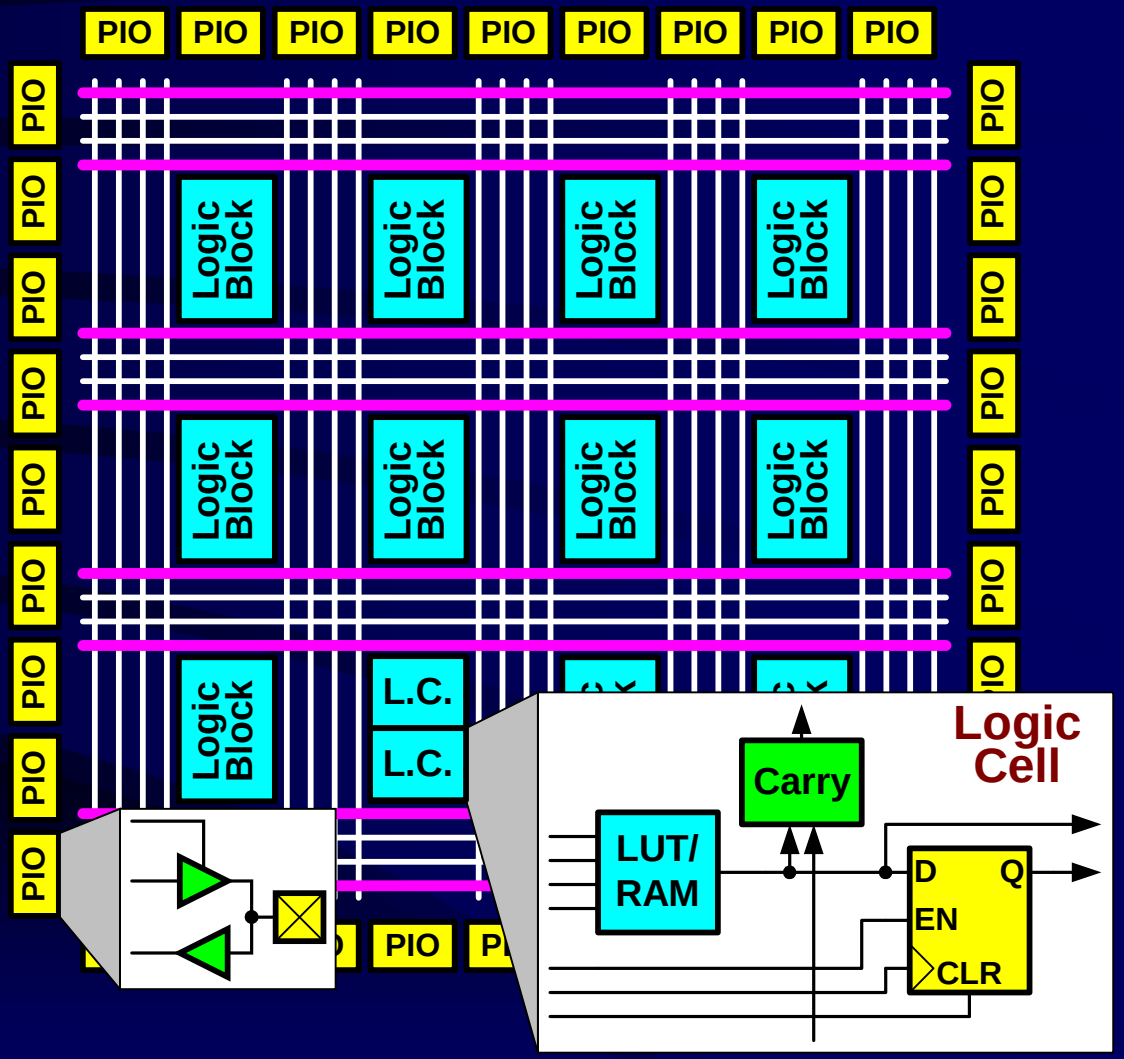


CPLD Vendors

Company	*CPLDs*	*PLDs/PALs*
Altera	MAX	Classic
Xilinx	XC9500	-
Vantis	MACH	PAL
Lattice	pLSI, GALs	GAL
Cypress	Flash 370, PAL	PAL
Atmel	ATF, ATV	ATF
TI	-	PAL
Philips	CoolRunner	-
ICT	-	PEEL

See also: www.optimagic.com/summary.html

What is an FPGA?



FPGA Vendors

Architecture	Process Technology: Static Memory	Anti-Fuse	Flash
Coarse-grained	**Altera** (FLEX) **Xilinx** (Spartan, 4KX, Virtex) **Lucent** (ORCA) **Atmel** (AT40K) **Vantis** (VF1) **DynaChip**	**QuickLogic** (pASIC)	
Fine-grained	**Atmel** (AT6000)	**Actel** (ACT, MX, SX)	**Gatefield**

See also: www.optimagic.com/summary.html

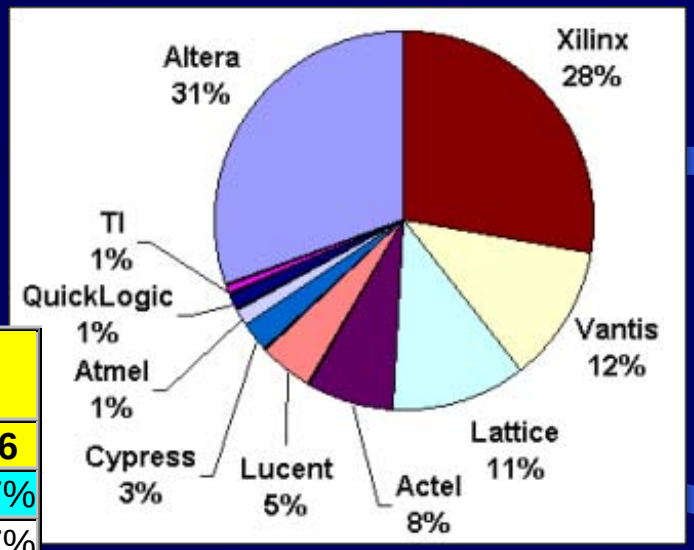
Comparing CPLDs and FPGAs

	CPLDs	*FPGAs*
Key Attributes	Fast pin-to-pin delay Predictable timing Wide fan-in Easy to use	Very high density Lots of I/Os and flip-flops Generally lower power Advanced features (RAM)
Typical Applications	Bus interfaces Complex state machines Fast memory interfaces Wide decoders PAL-device integration	Logic consolidation Board integration Replace obsolete devices Simple state machines Complex controllers
Design Timing	Usually fixed, PAL-like Fast pin-to-pin delays	Application dependent High internal performance
Process Technology	EPROM (OTP) EEPROM (some ISP) FLASH (some ISP)	SRAM (ISP) Anti-fuse (OTP) EEPROM (ISP)
Power Consumption	0.5-2.0W static (some "zero power") 0.5-4.0W dynamic	Very low static Dynamic consumption is application dependent, 0.1-2W typical

See also: www.optimagic.com/faq.html

Programmable Logic Market Data

(Reference)



Ranking	*Vendor*	*Revenues* (millions)		*'96-'97 Change*	*Market Share*	
		1997	*1996*		1997	1996
1	**Altera**	$ 631	$ 497	27%	31%	27%
2	**Xilinx**	$ 574	$ 509	13%	28%	27%
3	**Vantis**	$ 243	$ 248	-2%	12%	13%
4	**Lattice**	$ 237	$ 220	8%	11%	12%
5	**Actel**	$ 156	$ 150	4%	8%	8%
6	**Lucent**	$ 97	$ 91	7%	5%	5%
7	**Cypress**	$ 52	$ 68	-24%	3%	4%
8	**Atmel**	$ 31	$ 27	15%	1%	1%
9	**QuickLogic**	$ 29	$ 25	16%	1%	1%
10	**TI**	$ 18	$ 23	-22%	1%	1%
TOTAL		**$ 2,068**	**$ 1,858**	11%		

Source:
Electronic Buyer's News, 30-MAR-98
The Programmable Logic Jump Station

See also: www.optimagic.com/market.html

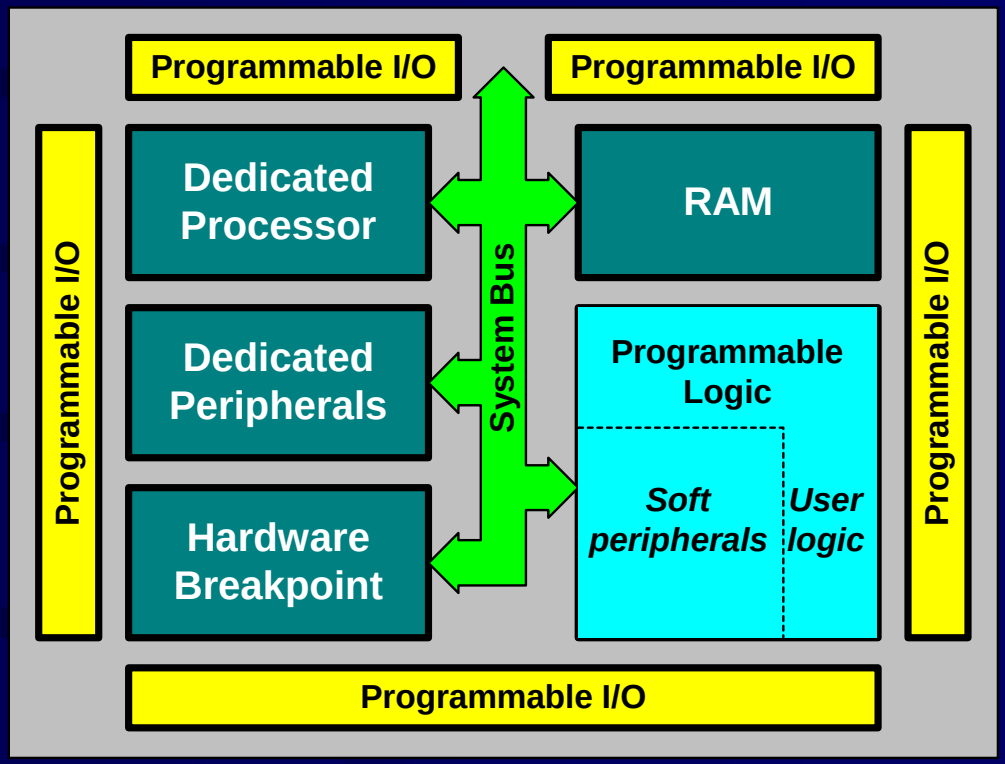
EMBEDDED SYSTEMS CONFERENCE

Hybrid Devices

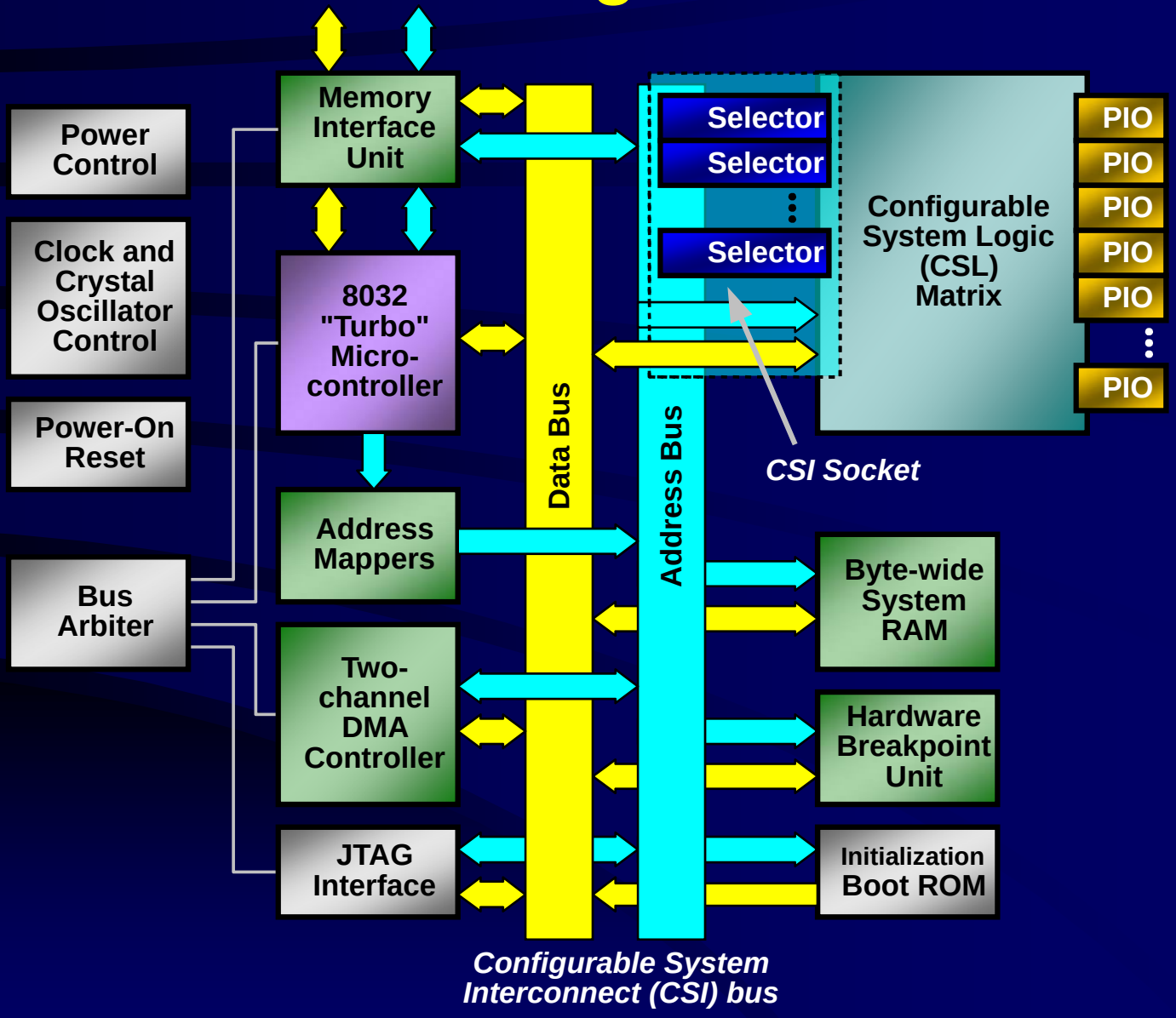
- **WSI Programmable System Device (PSD)**
  - 8- or 16-bit MCU interface
  - CPLD-style macrocells
  - on-chip memory
- **Lucent ORCA 3 and 3+ FPGAs**
  - Motorola/IBM PowerPC interface
  - Limited Intel 960 interface
  - Limited connectivity to FPGA array

What Is a Configurable Processor?

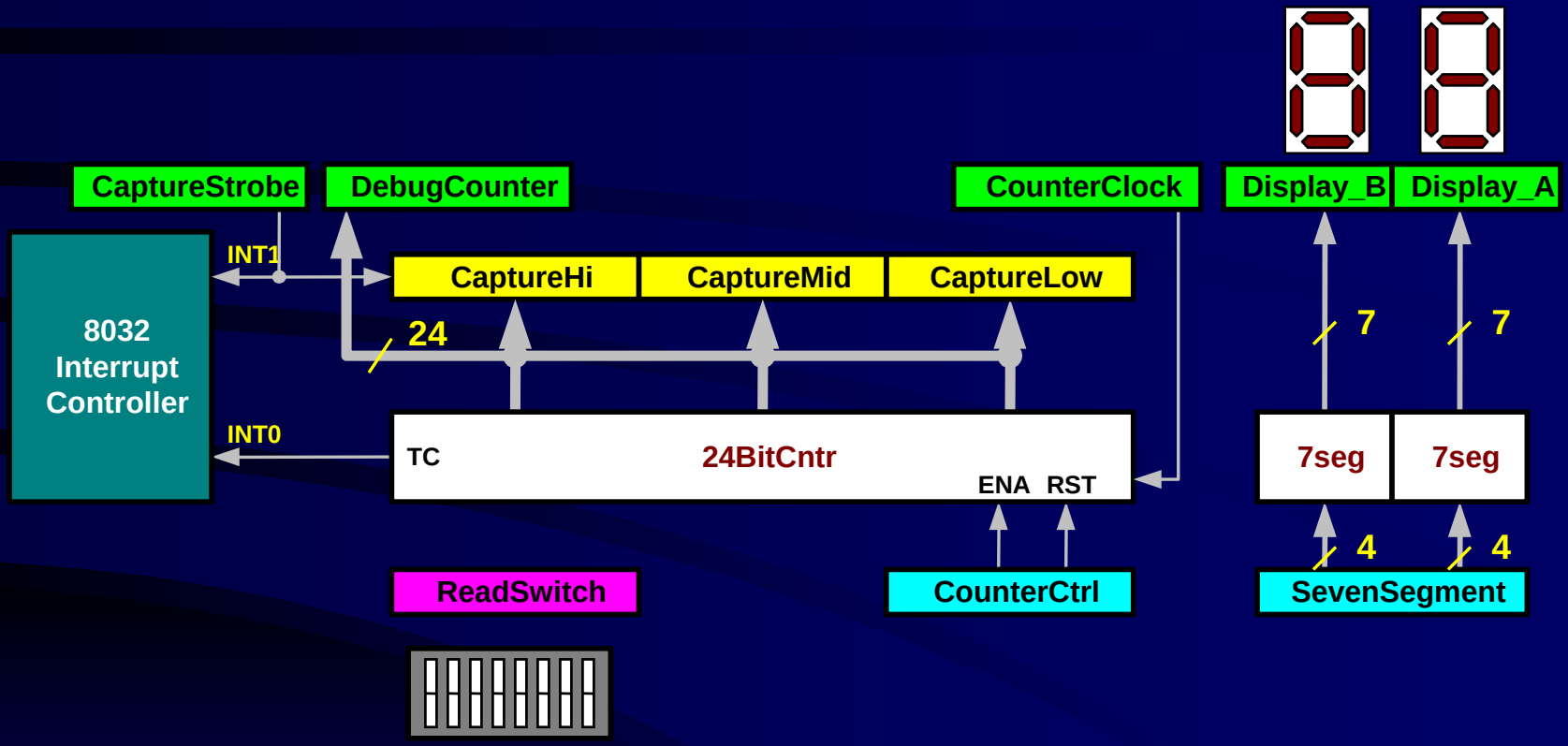
- Industry-standard processor
- Dedicated bus
- Programmable Logic
  - Soft peripherals
  - User-defined functions
  - Hardware acceleration
- On-Chip Memory



Triscend E5 Configurable Processor



Case Study: Our Own Derivative



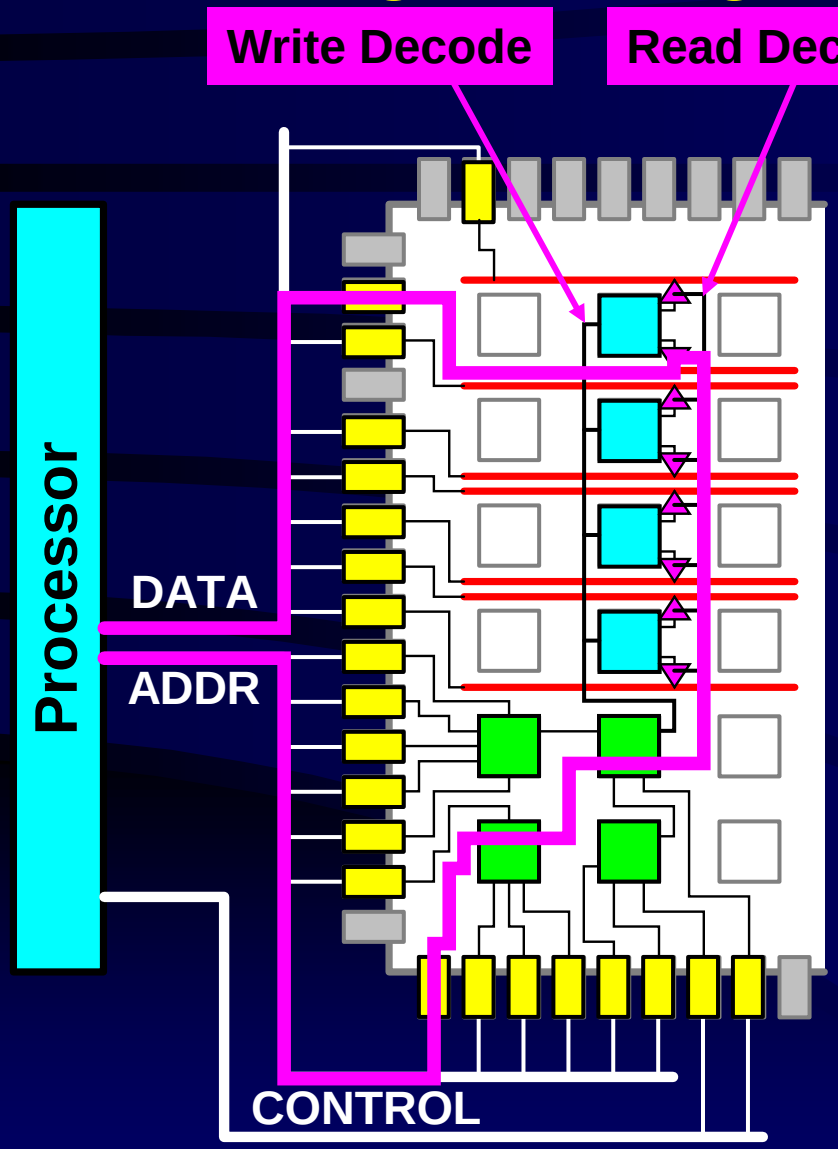
Case Study: Technical Challenges

- Communication between the processor and programmable logic functions
- Maintaining a standard development flow
- Debugging a system with both processor and programmable logic

Communication between the Processor and Programmable Logic

- Routing data and address bus
- Decoding/controlling bus transactions
- Register intimacy
- Debugging

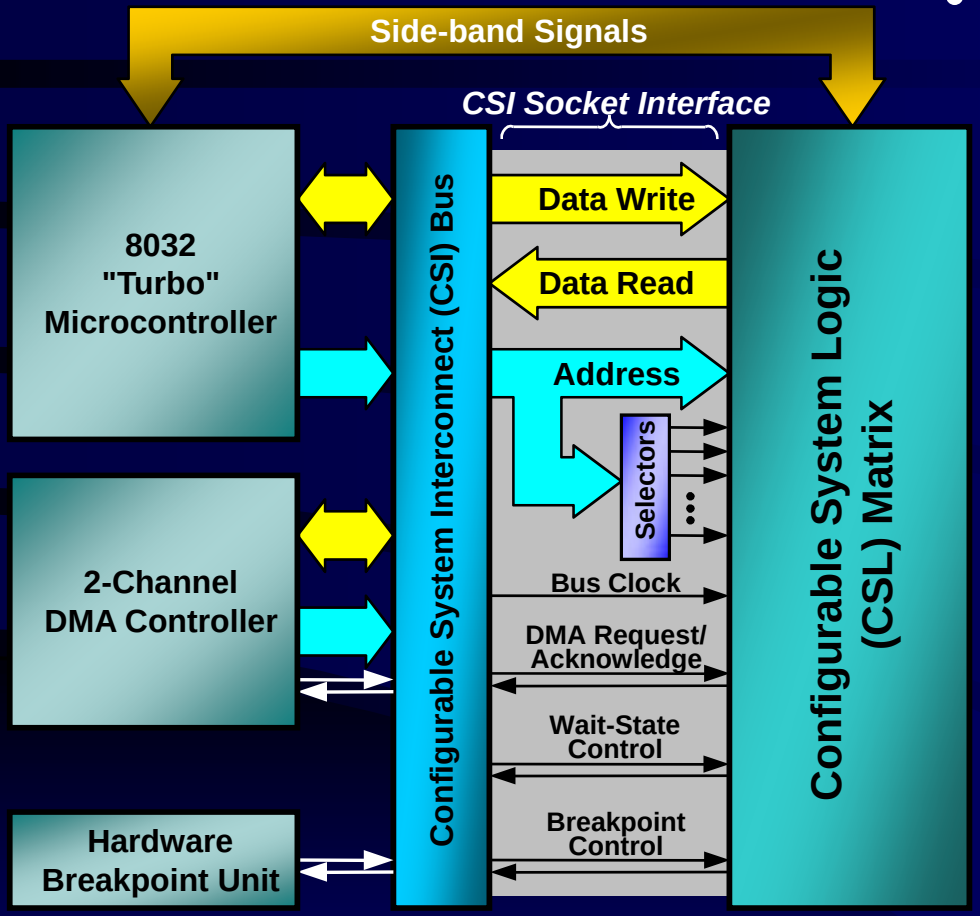
Routing Bus Signals: FPGA Example



- I/Os between devices
  - Many required, even for basic 8-bit interface)
  - Adds delay to critical path
  - Extra power consumption and EMI in two-chip solution
- Distributing address/data on-chip
  - Uses programmable interconnect
  - Adds delay to critical path
  - Variable delays in some architectures
  - Some devices provide bidirectional bussing

Another Approach: CSI Bus Socket

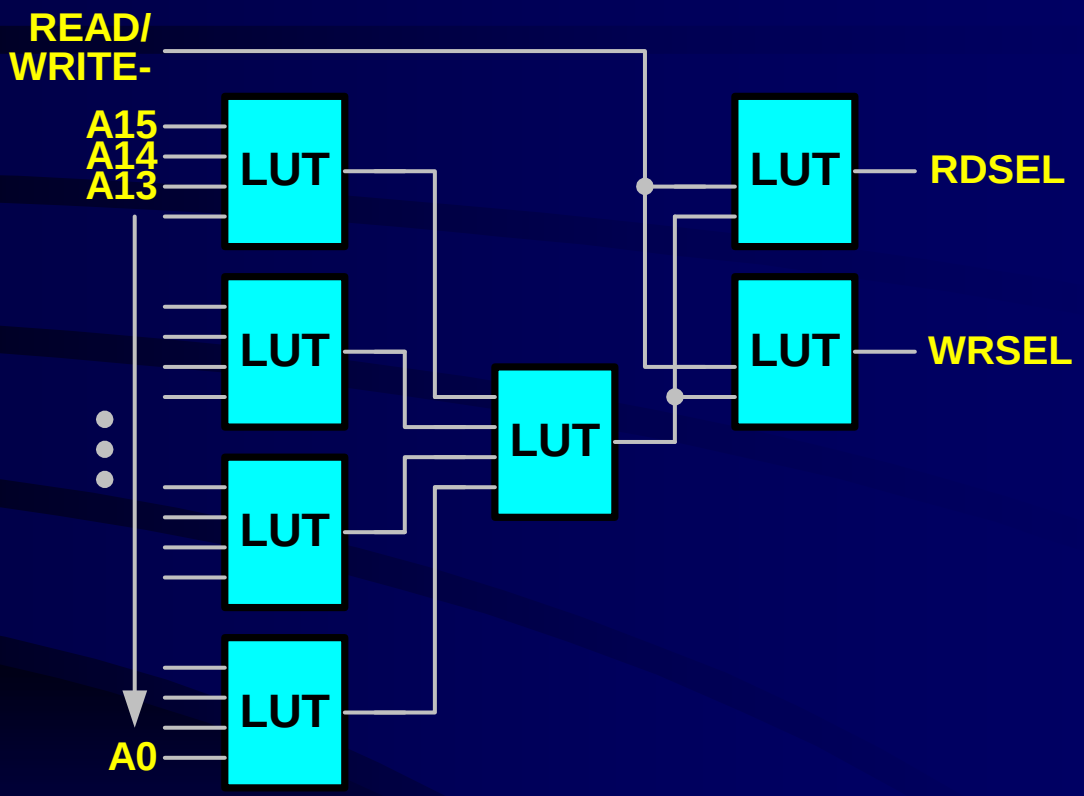
(Configurable System Interconnect)



- **Distributes address and data to CSL matrix**
  - No additional I/O required
  - Dedicated address decoding
  - Predictable, synchronous timing
  - Forward compatible with future configurable processors
  - Wait-state control
  - Contention-free bussing

Decoding Bus Transactions

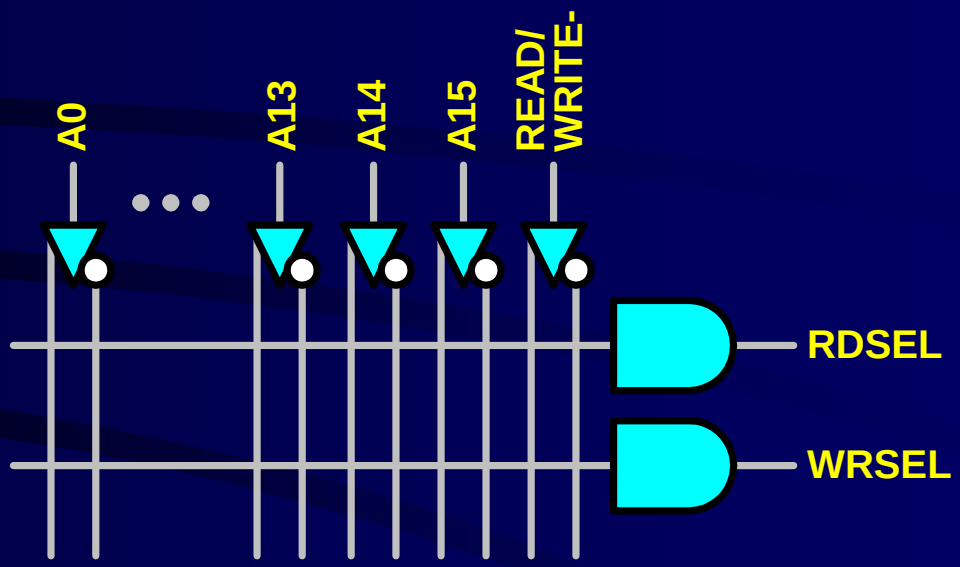
FPGA Style



- Decode delay is fan-out and routing dependent

Decoding Bus Transactions

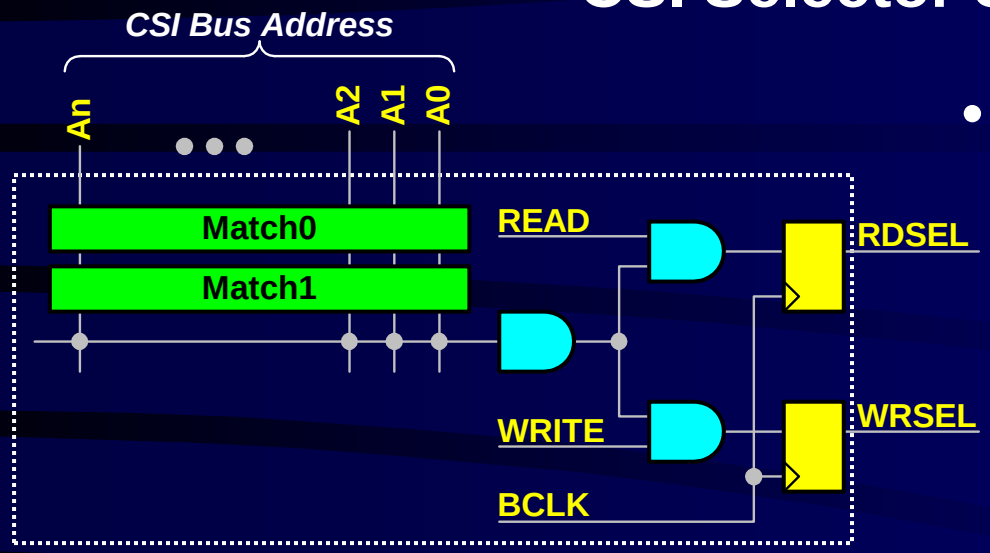
CPLD/PSD Style

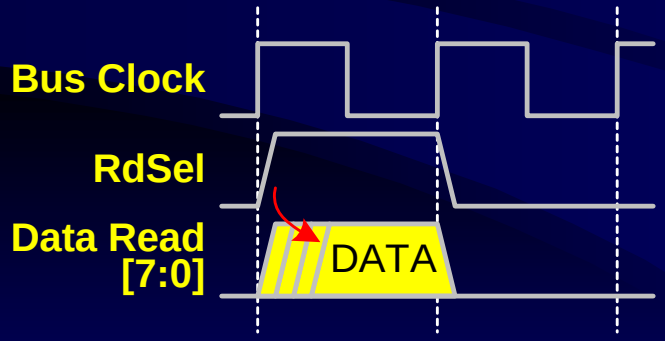


- Decode delay is constant

Decoding Bus Transactions

CSI Selector Style





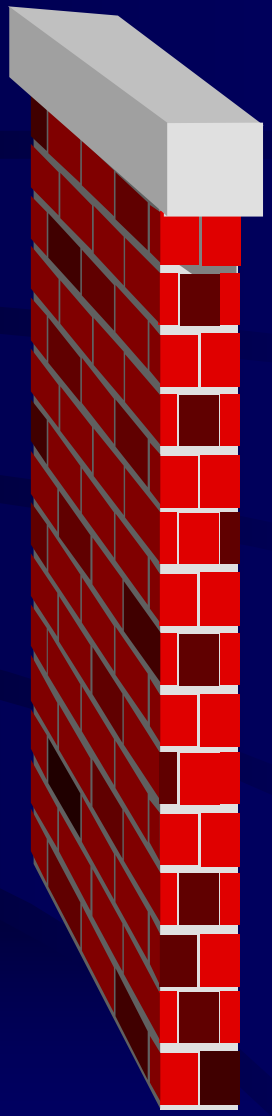
- Decode delay is constant (less than 5 ns after clock)

- **Fast address decoding**
  - Any address range
  - Access type
    - Code
    - Data
    - Special Function Register (SFR)
  - Three modes
    - Selector
    - Chip Select
    - DMA Control Register
  - Up to 200 selectors in a single device

Connecting the Two Development Worlds

Hardware Development

- Design and “soft” module libraries
- Passing register addresses to compiler/assembler
- Vendor place and route software
- Device programming support
- System-wide in-system debugging support

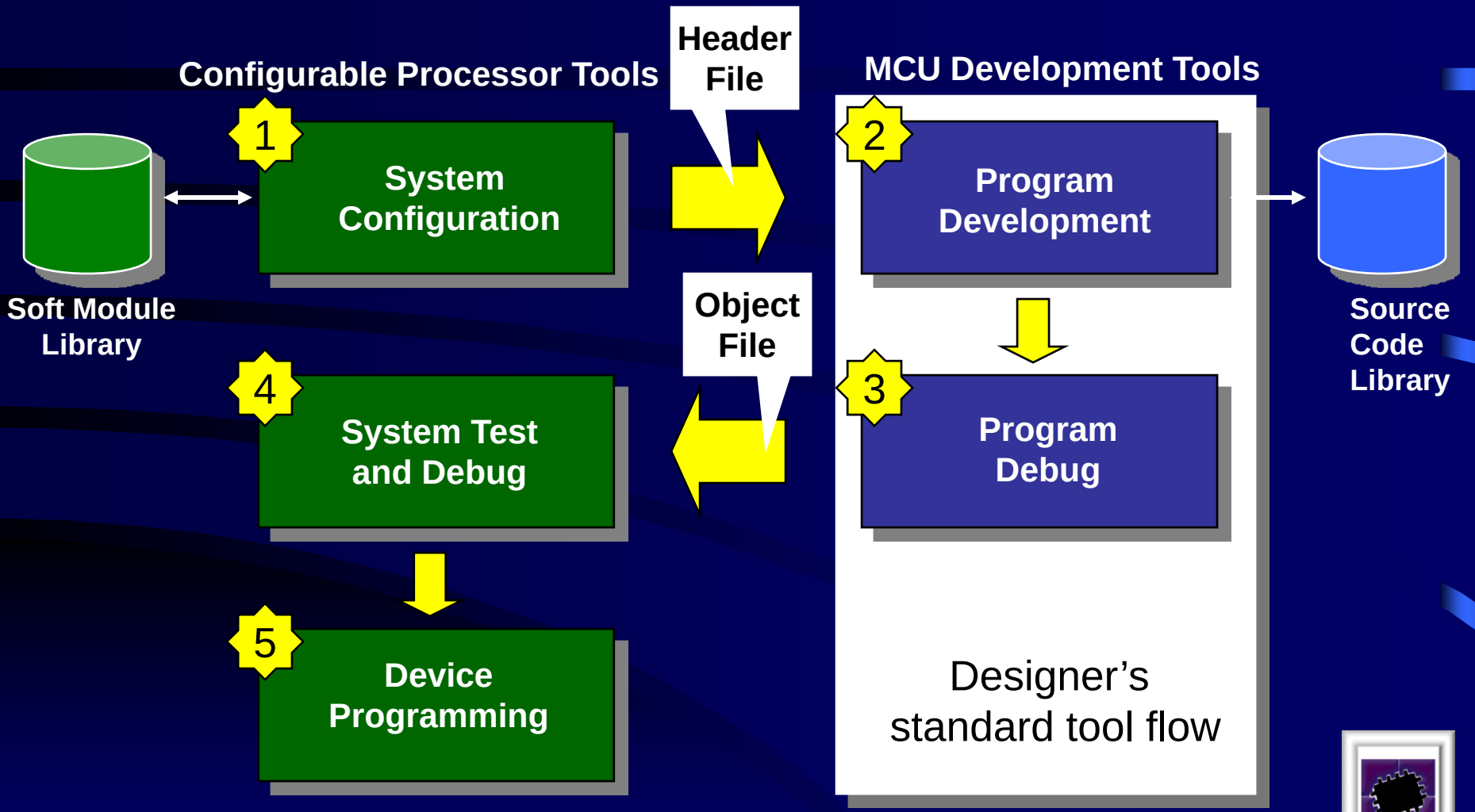


Software Development

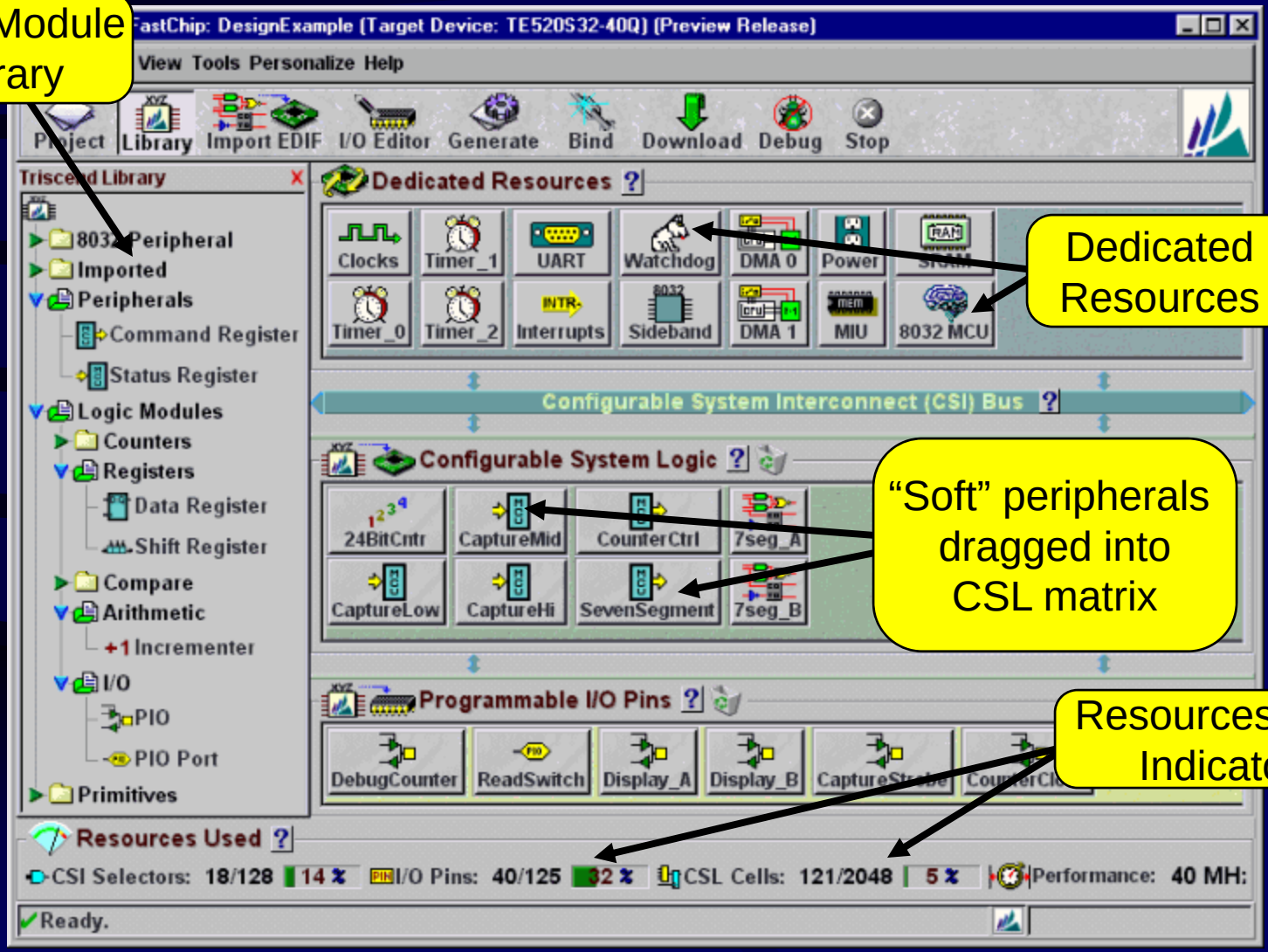
- Compiler/assembler support
- Function libraries
- Instruction-set simulator
- System-wide in-system debugging support

EMBEDDED SYSTEMS CONFERENCE

Preserving Existing Tool Flow



Case Study Design: FastChip Software



Real-Time, In-System Debugging

- Difficult in most ASIC or system-on-a-chip designs
  - Must rely on simulation before completing design
- Most debuggers only support the processor
  - Monitor bus activity
  - Monitor processor registers
  - Break on event and single-step
- Additional debugging desired for programmable logic functions
  - Monitor the state of logic and flip-flops in “soft” peripherals
  - Monitor or force a breakpoint from programmable logic

Summary

- **Configurable embedded systems offer potential benefits:**
  - **Faster time to market**
  - **Higher performance compared to discrete solutions**
  - **Higher product differentiation**
- **Configurable processors are a new class of single-chip programmable devices designed for embedded systems applications**
  - **Industry-standard processor**
  - **Dedicated, high-performance internal bus**
  - **Programmable logic, connected to internal bus**
  - **On-chip, high-density memory**

Looking for More?

- 

(Booth 5010)
  - Applications engineers available for questions
  - Software demonstrations throughout the day
  - CD-ROM with on-line tutorial and FastChip preview release
  - Visit www.triscend.com
- **Roll Your Own RISC**
  (Wednesday, 8:30, Class 402)
- **Prototyping Embedded Microcontrollers in FPGAs**
  (Wednesday, 4:00, Class 470)
- **An Introduction to FPGA Design**
  (Thursday, 8:30 and 10:30, Classes 509 and 529)

Questions?