Configurable Embedded Systems:
Using Programmable Logic to Compress Embedded System Design Cycles

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www.triscend.com
Agenda

- Forces Shaping Embedded Design
- Types of Design Solutions
- Programmable Technologies
- Technical Challenges
Key Forces Shaping Embedded Systems

- Time-to-Market Pressure
- Performance
- System Cost Pressure
- Differentiation

Embedded System Design
Why 'Configurable'? 

• **Time-to-Market**
  – Fast iterations
  – Fast in-system, real-time debugging
  – Fast component availability

• **Adaptability**
  – During design and debug
  – In the field
  – In the application

• **Performance**
  – Match the architecture to the problem
  – Fast response to real-time events
  – Parallel operations

• **Increased Differentiation**
Types of Design Solutions

- Stand-Alone Processor
- Processor Derivative
- Processor + ASIC
- Processor + Programmable Logic
- Custom Processor in Programmable Logic
- Custom Processor in ASIC
- Configurable Processor
- System on a Chip
<table>
<thead>
<tr>
<th>Hardware Customization</th>
<th>Custom Logic</th>
<th>Configurable Logic (off the shelf)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Instruction Set</td>
<td>System on a chip Processor + ASIC</td>
<td>“Roll your own” in FPGA Configurable processor (on-chip accelerator)</td>
</tr>
<tr>
<td>Peripheral Set, System Architecture</td>
<td>System on a chip Processor + ASIC</td>
<td>Processor + FPGA Configurable processor</td>
</tr>
<tr>
<td>I/O, Interface, Decoding</td>
<td>Processor + ASIC</td>
<td>Processor + CPLD/FPGA Configurable processor</td>
</tr>
<tr>
<td>None</td>
<td>-</td>
<td>Stand-alone processor or derivative</td>
</tr>
</tbody>
</table>

**Highest Customization** | **Fast Time-to-Market**
History of Configurable Technologies

1980
- MCU
- TTL
- PAL
- EPROM
- Peripheral
- Peripheral

1990
- MCU Derivative
- CPLD/FPGA
- RAM
- EPROM/FLASH
- Peripheral

2000
- "System on a Chip"
- "Roll-Your-Own" MCU in FPGA
- Configurable Processor
- EPROM/FLASH
- Configurable Processors

Discrete Solutions

Increasing Functionality, Density, and Performance
Today's Configurable Technologies

• Complex Programmable Logic Devices (CPLD)
• Field Programmable Gate Arrays (FPGA)
• Hybrid Devices
  – Processor interface
  – Programmable logic
• Configurable Processors
  – Integrated processor
  – Programmable logic
  – Dedicated on-chip bus
  – On-chip memory
What is a CPLD?

A function block is similar to a PAL or PLD
### CPLD Vendors

<table>
<thead>
<tr>
<th>Company</th>
<th>CPLDs</th>
<th>PLDs/PALs</th>
</tr>
</thead>
<tbody>
<tr>
<td>Altera</td>
<td>MAX</td>
<td>Classic</td>
</tr>
<tr>
<td>Xilinx</td>
<td>XC9500</td>
<td>-</td>
</tr>
<tr>
<td>Vantis</td>
<td>MACH</td>
<td>PAL</td>
</tr>
<tr>
<td>Lattice</td>
<td>pLSI, GALs</td>
<td>GAL</td>
</tr>
<tr>
<td>Cypress</td>
<td>Flash 370, PAL</td>
<td>PAL</td>
</tr>
<tr>
<td>Atmel</td>
<td>ATF, ATV</td>
<td>ATF</td>
</tr>
<tr>
<td>TI</td>
<td>-</td>
<td>PAL</td>
</tr>
<tr>
<td>Philips</td>
<td>CoolRunner</td>
<td>-</td>
</tr>
<tr>
<td>ICT</td>
<td>-</td>
<td>PEEL</td>
</tr>
</tbody>
</table>

See also: [www.optimagic.com/summary.html](http://www.optimagic.com/summary.html)
What is an FPGA?
FPGA Vendors

<table>
<thead>
<tr>
<th>Architecture</th>
<th>Static Memory</th>
<th>Anti-Fuse</th>
<th>Flash</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coarse-grained</td>
<td>Altera (FLEX)</td>
<td>QuickLogic (pASIC)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>Xilinx (Spartan, 4KX, Virtex)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Lucent (ORCA)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Atmel (AT40K)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Vantis (VF1)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>DynaChip</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Fine-grained</td>
<td>Atmel (AT6000)</td>
<td>Actel (ACT, MX, SX)</td>
<td>Gatefield</td>
</tr>
</tbody>
</table>

See also: www.optimagic.com/summary.html
# Comparing CPLDs and FPGAs

<table>
<thead>
<tr>
<th>Key Attributes</th>
<th>CPLDs</th>
<th>FPGAs</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Fast pin-to-pin delay</td>
<td>Very high density</td>
</tr>
<tr>
<td></td>
<td>Predictable timing</td>
<td>Lots of I/Os and flip-flops</td>
</tr>
<tr>
<td></td>
<td>Wide fan-in</td>
<td>Generally lower power</td>
</tr>
<tr>
<td></td>
<td>Easy to use</td>
<td>Advanced features (RAM)</td>
</tr>
<tr>
<td>Typical Applications</td>
<td>Bus interfaces</td>
<td>Logic consolidation</td>
</tr>
<tr>
<td></td>
<td>Complex state machines</td>
<td>Board integration</td>
</tr>
<tr>
<td></td>
<td>Fast memory interfaces</td>
<td>Replace obsolete devices</td>
</tr>
<tr>
<td></td>
<td>Wide decoders</td>
<td>Simple state machines</td>
</tr>
<tr>
<td></td>
<td>PAL-device integration</td>
<td>Complex controllers</td>
</tr>
<tr>
<td>Design Timing</td>
<td>Usually fixed, PAL-like</td>
<td>Application dependent</td>
</tr>
<tr>
<td></td>
<td>Fast pin-to-pin delays</td>
<td>High internal performance</td>
</tr>
<tr>
<td>Process Technology</td>
<td>EPROM (OTP)</td>
<td>SRAM (ISP)</td>
</tr>
<tr>
<td></td>
<td>EEPROM (some ISP)</td>
<td>Anti-fuse (OTP)</td>
</tr>
<tr>
<td></td>
<td>FLASH (some ISP)</td>
<td>EEPROM (ISP)</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>0.5-2.0W static (some &quot;zero power&quot;)</td>
<td>Very low static</td>
</tr>
<tr>
<td></td>
<td>0.5-4.0W dynamic</td>
<td>Dynamic consumption is application dependent, 0.1-2W typical</td>
</tr>
</tbody>
</table>

See also: [www.optimagic.com/faq.html](http://www.optimagic.com/faq.html)
### Programmable Logic Market Data

#### (Reference)

<table>
<thead>
<tr>
<th>Ranking</th>
<th>Vendor</th>
<th>Revenues (millions)</th>
<th>'96-'97 Change</th>
<th>Market Share</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Altera</td>
<td>$631</td>
<td>$497</td>
<td>27%</td>
</tr>
<tr>
<td>2</td>
<td>Xilinx</td>
<td>$574</td>
<td>$509</td>
<td>13%</td>
</tr>
<tr>
<td>3</td>
<td>Vantis</td>
<td>$243</td>
<td>$248</td>
<td>-2%</td>
</tr>
<tr>
<td>4</td>
<td>Lattice</td>
<td>$237</td>
<td>$220</td>
<td>8%</td>
</tr>
<tr>
<td>5</td>
<td>Actel</td>
<td>$156</td>
<td>$150</td>
<td>4%</td>
</tr>
<tr>
<td>6</td>
<td>Lucent</td>
<td>$97</td>
<td>$91</td>
<td>7%</td>
</tr>
<tr>
<td>7</td>
<td>Cypress</td>
<td>$52</td>
<td>$68</td>
<td>-24%</td>
</tr>
<tr>
<td>8</td>
<td>Atmel</td>
<td>$31</td>
<td>$27</td>
<td>15%</td>
</tr>
<tr>
<td>9</td>
<td>QuickLogic</td>
<td>$29</td>
<td>$25</td>
<td>16%</td>
</tr>
<tr>
<td>10</td>
<td>TI</td>
<td>$18</td>
<td>$23</td>
<td>-22%</td>
</tr>
<tr>
<td>TOTAL</td>
<td></td>
<td>$2,068</td>
<td>$1,858</td>
<td>11%</td>
</tr>
</tbody>
</table>

**Source:**
Electronic Buyer’s News, 30-MAR-98
The Programmable Logic Jump Station

See also: www.optimagic.com/market.html
Hybrid Devices

- **WSI Programmable System Device (PSD)**
  - 8- or 16-bit MCU interface
  - CPLD-style macrocells
  - on-chip memory

- **Lucent ORCA 3 and 3+ FPGAs**
  - Motorola/IBM PowerPC interface
  - Limited Intel 960 interface
  - Limited connectivity to FPGA array
What Is a Configurable Processor?

- **Industry-standard processor**
- **Dedicated bus**
- **Programmable Logic**
  - Soft peripherals
  - User-defined functions
  - Hardware acceleration
- **On-Chip Memory**
Triscend E5 Configurable Processor

- Power Control
- Clock and Crystal Oscillator Control
- Power-On Reset
- Bus Arbiter
- Memory Interface Unit
- 8032 "Turbo" Microcontroller
- Address Mappers
- Two-channel DMA Controller
- JTAG Interface
- Configurable System Logic (CSL) Matrix
- Configurable System Interconnect (CSI) bus
- Byte-wide System RAM
- Hardware Breakpoint Unit
- Initialization Boot ROM
- Initialization
- Boot ROM
Case Study: Our Own Derivative
Case Study: Technical Challenges

- Communication between the processor and programmable logic functions
- Maintaining a standard development flow
- Debugging a system with both processor and programmable logic
Communication between the Processor and Programmable Logic

- Routing data and address bus
- Decoding/controlling bus transactions
- Register intimacy
- Debugging
Routing Bus Signals: FPGA Example

• I/Os between devices
  - Many required, even for basic 8-bit interface
  - Adds delay to critical path
  - Extra power consumption and EMI in two-chip solution

• Distributing address/data on-chip
  - Uses programmable interconnect
  - Adds delay to critical path
  - Variable delays in some architectures
  - Some devices provide bidirectional bussing
Another Approach: CSI Bus Socket
(Configurable System Interconnect)

- Distributes address and data to CSL matrix
  - No additional I/O required
  - Dedicated address decoding
  - Predictable, synchronous timing
  - Forward compatible with future configurable processors
  - Wait-state control
  - Contention-free bussing
Decoding Bus Transactions

FPGA Style

- Decode delay is fan-out and routing dependent
Decoding Bus Transactions

CPLD/PSD Style

- Decode delay is constant
Decoding Bus Transactions
CSI Selector Style

- Fast address decoding
  - Any address range
  - Access type
    - Code
    - Data
    - Special Function Register (SFR)
  - Three modes
    - Selector
    - Chip Select
    - DMA Control Register
  - Up to 200 selectors in a single device

- Decode delay is constant (less than 5 ns after clock)
Connecting the Two Development Worlds

Hardware Development
- Design and "soft" module libraries
- Passing register addresses to compiler/assembler
- Vendor place and route software
- Device programming support
- System-wide in-system debugging support

Software Development
- Compiler/assembler support
- Function libraries
- Instruction-set simulator
- System-wide in-system debugging support
Preserving Existing Tool Flow

1. System Configuration
2. Program Development
3. Program Debug
4. System Test and Debug
5. Device Programming

Configurable Processor Tools

MCU Development Tools

Soft Module Library

Source Code Library

Designer’s standard tool flow
Case Study Design: FastChip Software

“Soft” Module Library

Dedicated Resources

“Soft” peripherals dragged into CSL matrix

Resources Used Indicators

Dedicated Resources

“Soft” Module

Library

Resources Used

Indicators
Real-Time, In-System Debugging

- Difficult in most ASIC or system-on-a-chip designs
  - Must rely on simulation before completing design
- Most debuggers only support the processor
  - Monitor bus activity
  - Monitor processor registers
  - Break on event and single-step
- Additional debugging desired for programmable logic functions
  - Monitor the state of logic and flip-flops in “soft” peripherals
  - Monitor or force a breakpoint from programmable logic
Summary

• **Configurable embedded systems** offer potential benefits:
  – Faster time to market
  – Higher performance compared to discrete solutions
  – Higher product differentiation

• **Configurable processors** are a new class of single-chip programmable devices designed for embedded systems applications
  – Industry-standard processor
  – Dedicated, high-performance internal bus
  – Programmable logic, connected to internal bus
  – On-chip, high-density memory
Looking for More?

• **Triscend** (Booth 5010)
  - Applications engineers available for questions
  - Software demonstrations throughout the day
  - CD-ROM with on-line tutorial and FastChip preview release
  - Visit www.triscend.com

• **Roll Your Own RISC**
  (Wednesday, 8:30, Class 402)

• **Prototyping Embedded Microcontrollers in FPGAs**
  (Wednesday, 4:00, Class 470)

• **An Introduction to FPGA Design**
  (Thursday, 8:30 and 10:30, Classes 509 and 529)
Questions?