iCE65™ FPGA Low Power Design Guidelines

SiliconBlue®

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Introduction

To minimize static power consumption, all input connections must be in a defined state. In many applications, I/O voltage levels are guaranteed using pull-up or pull-down resistors. To minimize power consumption, PIO pins connected to pull-up or pull-down resistors must either be three-stated (Hi-Z or high-impedance) or driven to the same voltage as the pull-up or pull-down resistor voltage.

The most common reason for excessive state power consumption is that PIO pins or system I/O signals are driving against pull-up or pull-down resistors.

Voltage across a Resistor Causes Current Flow and Burns Power

Table 1 lists the various possible PIO pin configurations and how they interact with pull-up or pull-down resistors. For lowest possible power consumption, the FPGA PIO pins must be connected as shown in the table. Avoid the high power consumption condition.

Table 1: **PIO Pin Configurations and Possible Power Scenarios**

Pin Type	PIO Configuration	Is a Pull-up or Pull-down Resistor Connected?	Condition for Lowest Power Consumption	Condition to Avoid (Causes Maximum Power)
Used PIO Pins	Driving output (output, bidirectional I/O, or enabled output)	None	Output driving High or Low	Floating output (Hi-Z) or bus contention (one driver High, the other Low)
		Internal or external pull-up	Hi-Z or High input value	Drive Low
		External pull-down	Hi-Z or Low input value	Drive High
	Input-only	None	A stable High or Low input value	Floating or undefined input; slowly-changing input
		Internal or external pull-up	Hi-Z or High input value	Low input value
		External pull-down	Hi-Z or Low input value	High input value
Unused PIO Pins (Table 5)	Unused PIO pin (except in I/O Bank 3 on iCE65L04/L08 or iCE65P04)	Internal pull-up (default)	Hi-Z or High input value	Low input value
		None (non-default)	A stable High or Low input value. Tie external or actively drive internally.	Floating or undefined input
	Unused PIO pin in I/O Bank 3 (except iCE65L01)	None (default). Input disabled.	Hi-Z or undefined input. Input disabled.	None
JTAG	JTAG Inputs (TRST_B, TDI, TMS, TCK)	None	See Table 4	Floating or undefined input
Differ-ential Pair	Differential Channel	Compensation or termination resistors	Both differential outputs at same voltage or one output Hi-Z	Differential outputs driven to opposite logic value

The logic level at an un-driven FPGA pin may be maintained using a pull-up or pull-down resistor. However, take care to avoid excessive power consumption. Unused PIO pins represent a special case, as described later, on page 5 .

Common Accidental Power Wasters

The following list represents the most common power wasters found in iCE65 FPGA applications. Correct these conditions to reduce device power consumption.

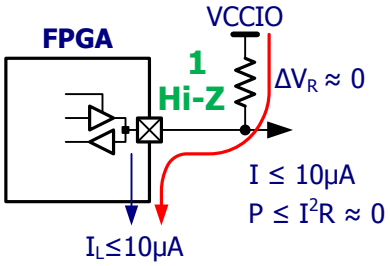
1. External Pull-up and Pull-down Resistors Driven to Wrong Logic Level, Drawing Current

The most likely cause of excess power consumption is I/O pins with an associated pull-up or pull-down resistor that are driven to the opposite logic value, creating the maximum voltage across the resistor.

Minimal Power State = No or Little Voltage across Resistor

Figure 1 shows the desired, minimal power state where there is little or no voltage differential across the pull-up or pull-down resistor. This example shows a pull-up resistor but the concept is similar for a pull-down resistor. If the FPGA drives its output High, or if the output is three-stated or placed in the high-impedance state (Hi-Z), then the voltage at the FPGA pin approaches the VCCIO supply voltage. There is a possible current flow path due to pin leakage, but worst-case, this amounts to 10 µA per pin. Consequently, there is little voltage drop across the pull-up resistor and little power consumed.

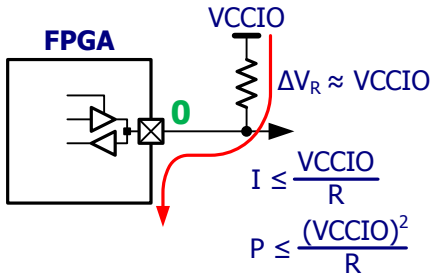
Figure 1: **Minimal Power State, No Voltage across Resistor (pull-up resistor example)**



Maximum Power State = Voltage across Resistor

Compare the minimal power state from Figure 1 to the maximum power state, shown in Figure 2, where the output drives to the opposite voltage of the pull-up or pull-down resistor, generating the maximum voltage difference across the resistor.

Figure 2: **Maximum Power State, Maximum Voltage across Resistor (pull-up resistor example)**

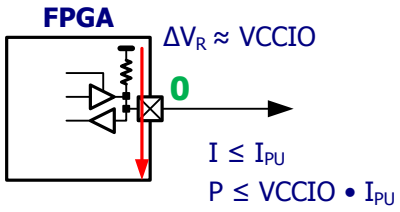


For example, in a 3.3 V interface with a 10 kΩ pull-up resistor, the state power consumption per pin will exceed 1 mW if the output driver fights against the pull-up or pull-down resistor! Drive the output to the same voltage level as the pull-up or pull-down voltage and the static power drops to almost nothing.

Optional Internal Pull-up Resistors

The situation is similar when driving against the FPGA's internal, optional pull-up resistor, as shown in Figure 3. As shown in Table 2, the optional pull-up is available on all iCE65 FPGAs in I/O Bank 0, 1, 2, and the SPI Bank. The optional pull-up resistor is also available in I/O Bank 3 on the iCE65L01 FPGA. There is no pull-up resistor present on the JTAG port input pins.

Figure 3: **Maximum Power State, Maximum Voltage across Optional Internal Pull-Up Resistor**

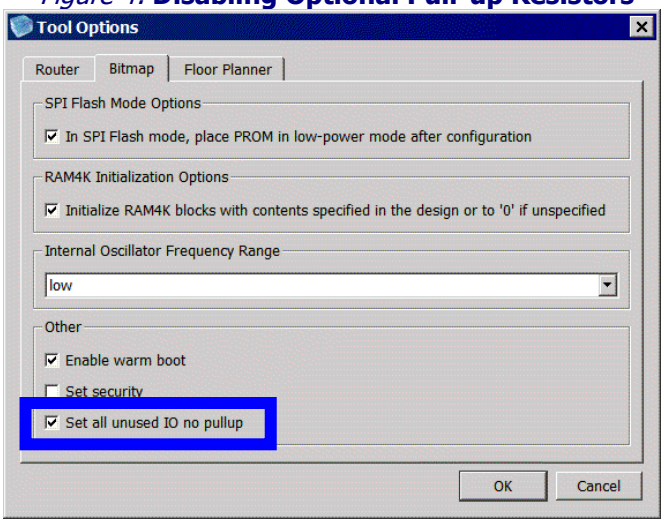


By default, unused PIO pins, except in I/O Bank 3 on FPGA larger than the iCE65L01, are defined as an input with the pull-up resistor enabled, as described in Table 5. This default can be disabled for a specific design from the iCEcube **Tool Options** settings by checking **`Set all unused IO no pullup`**, as show in Figure 4.

Table 2: **Optional Internal Pull-Up Resistor within I/O Banks, by Part Type**

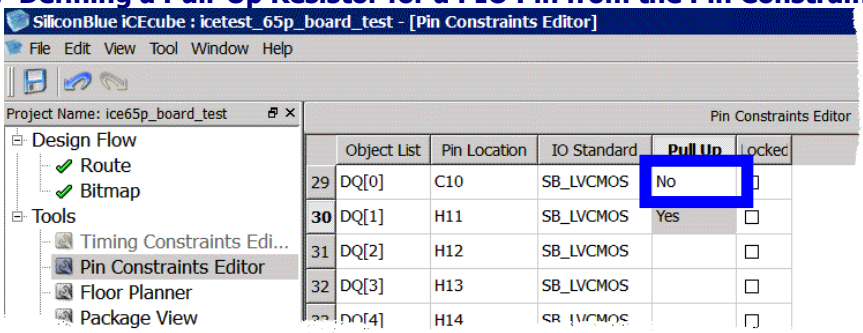
Part Type	I/O Bank 0	I/O Bank 1	I/O Bank 2	I/O Bank 3	SPI Bank	JTAG Port
iCE65L01	Optional pull-up	Optional pull-up	Optional pull-up	Optional pull-up	Optional pull-up	No pull-up
iCE65L04 iCE65P04	Optional pull-up	Optional pull-up	Optional pull-up	No pull-up	Optional pull-up	No pull-up
iCE65L08	Optional pull-up	Optional pull-up	Optional pull-up	No pull-up	Optional pull-up	No pull-up
iCE65P04	Optional pull-up	Optional pull-up	Optional pull-up	No pull-up	Optional pull-up	No pull-up

Figure 4: **Disabling Optional Pull-up Resistors**



The internal pull-up resistor is disabled by default for any PIO pin actually used in the application. To optionally assign a pull-up resistor for a specific PIO pin, use the iCEcube Pin Constraints Editor and select **`Yes`** from the **`Pull Up`** drop-down menu, as shown in Figure 5.

Figure 5: **Defining a Pull-Up Resistor for a PIO Pin from the Pin Constraints Editor**



Selecting a Pull-up/Pull-down Resistor Value

Select the proper resistor value for lowest power consumption and acceptable switching performance based on capacitive loading. A larger resistor value uses less power if the output driver ever drives against a pull-up or pull-down resistor. A large resistor value produces a smaller voltage drop, thereby consuming less power. However, a large resistor value also affects the transition time from the active driving state to the high-impedance (Hi-Z) state. Ideally, keep the transition time to 250 ns or less. One RC time constant is approximately the same time required to reach the switching threshold, as shown in Equation 1.

$$\tau = RC \approx 63\% \text{ final voltage} \leq 250 \text{ ns} \qquad \text{[Equation 1]}$$

Solve for R (in kΩ) using Equation 2, and where C is the total capacitance (in pF), including the capacitance of the PCB trace and all pins on the trace. Table 3 lists the maximum recommended pull-up or pull-down resistor values based on total capacitive loading. The resistor value must never larger than 45 kΩ, which is required to overcome pin leakage, I_L.

$$R\ (k\Omega) \leq \frac{250 \text{ ns}}{C\ (pF)} \qquad \text{[Equation 2]}$$

Table 3: **Largest Recommended Pull-up/Pull-down Resistor Values**

Capacitive Loading	Minimum Pull-up/ Pull-Down Resistor Allowed	Maximum Recommended Pull-up/ Pull-Down Resistor Value	Maximum Pull-up/Pull-Down Resistor Allowed
6 pF (unloaded pin)	≥ 390 Ω	≤ 41 kΩ	≤ 45 kΩ
10 pF		≤ 25 kΩ	
15 pF		≤ 16 kΩ	
20 pF		≤ 12.5 kΩ	
25 pF		≤ 10 kΩ	
30 pF		≤ 8.3 kΩ	
40 pF		≤ 6.25 kΩ	
50 pF		≤ 5 kΩ	

If the resistor is just to guarantee a voltage level, use the largest resistor value possible, according to Table 3. For some applications however, such as open-drain or open-source circuits, the pull-up or pull-down resistor value is ideally small to provide sufficient performance for the active-to-Hi-Z condition. However, the resistor value must be large enough so that the output driver can source or sink enough DC current to overcome the resistor, generally 390 Ω or larger.

2. Floating Used Input Pins Consume Power, Including JTAG Inputs

Floating or Hi-Z levels on used input pins also increases power consumption. To reduce power consumption, keep all used inputs at defined logic High or Low levels. Ununsed PIO pins are handled differently as outlined in Table 5.

Define All Input Values, Avoid Floating Inputs

All used input pins must be at a High or Low logic level, including the JTAG input pins. A floating input increases static current consumption. Similarly, once a floating input reaches its switching threshold, it can oscillate, causing spurious transitions that consume power.

The logic level on unused PIOs pins can be defined in a variety of different manners.

1. Driven High or Low by external device. Be careful that the output level does not conflict with any internal or external pull-up or pull-down resistors.
2. Pulled High or Low using an external resistor or pulled High using the optional pull-up resistor in PIO pins within I/O Bank 0, 1, 2 or the SPI Bank, or I/O Bank 3 on the iCE65L01 FPGA.

Tie JTAG Inputs for Lowest Power Consumption

During normal logic operation, the JTAG TRST_B pin must be Low. In most applications, the JTAG interface – only available on selected packages – is used in one of the three following ways.

- CASE 1: The JTAG inputs are constantly driven by some external device. If the input pins are constantly driven, then no additional pull-up or pull-down resistors are required.
- CASE 2: The JTAG port connects to a header, which is not always connected or driven by an external JTAG controller. In this case, the JTAG inputs must be connected to individual pull-up or pull-down resistors as shown in Table 4. The resistor holds the JTAG interface in the benign state and an external controller, when connected, can easily overdrive the resistors.
- CASE 3: Some applications may not ever use the JTAG interface. In this case, connect the inputs directly to ground, as shown in Table 4.

Table 4: **Defining the JTAG Input Pins**

JTAG Input	CASE 1: Connected and Actively Driven	CASE 2: JTAG Interface Connector, Not Actively Driven	CASE 3: JTAG Interface Not Used
TRST_B	Actively driven by controller	Pull-down resistor to ground	Tie to ground
TDI	Actively driven by controller	Pull-up resistor to VCCIO_1 or a pull-down resistor to ground	Tie to ground
TMS	Actively driven by controller	Pull-up resistor to VCCIO_1	Tie to ground
TCK	Actively driven by controller	Pull-up resistor to VCCIO_1	Tie to ground

3. Unused PIOs (except in I/O Bank 3 of iCE65L04/L08 or iCE65P04) Tied to GND or Pulled-Down

Ununsed PIO pins must be at a defined logic level. As shown in Table 5, iCE65 FPGAs have built-in features to maintain a static logic level for unused pins.

By default, ununsed PIO pins in I/O Bank 0, 1, 2 and the SPI bank and I/O Bank 3 on the iCE65L01 FPGA, are defined as inputs with an internal pull-up resistor to the PIO pin's associated voltage input (VCCIO_# or SPI_VCC). The electrical characteristics for the pull-up resistor is described in the iCE65 and iCE65P data sheets, duplicated here in Table 6 and Figure 6.

For minimum power, ideally leave unused PIO pins disconnected (floating), but never the JTAG inputs. Do not drive unused PIO pins that have a pull-up resistor, shown in Table 5, Low and do not connect them to a pull-down resistor as this unnecessarily consumes power, as shown in Figure 3. Optionally, drive these pins with a logic High.

Table 5: **Unused PIO Pins and Default Configuration**

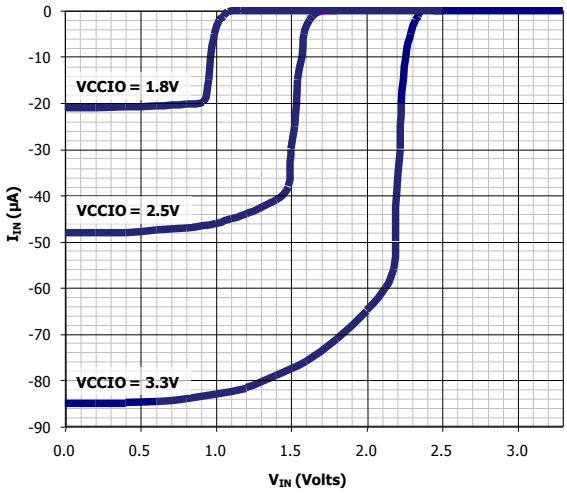
	I/O Bank 0 I/O Bank 1 I/O Bank 2 SPI Bank (I/O Bank3 on iCE65L01)	I/O Bank 3 (except on iCE65L01)	JTAG Inputs
I/O standards supported	Single-ended LVCMOS Differential outputs	Single-ended LVCMOS Single-ended specialty Differential inputs and outputs	Single-ended LVCMOS
Optional internal pull-up resistor available?	**Yes**	No	No
Input disable feature?	No	**Yes**	No
Default configuration for unused pins	Input with internal pull-up enabled	Input (input disabled, driving constant value)	Tie to ground
Low power state	Leave unconnected (floating, Hi-Z) or drive High	Leave unconnected (floating, Hi-Z)	See Table 4

I/O Bank 3 on the iCE65L04/P04 and the iCE65L08 is different than the other I/O banks. I/O Bank 3 on these FPGAs supports differential inputs and specialty I/O standards. Similarly, the PIO pins in I/O Bank 3 do not include a pull-up resistor. Instead, the input path has an input enable, which is disabled on unused PIO pins, forcing the pin to a known state. Leave unused PIO pins in I/O Bank 3 unconnected or floating.

Table 6: **Internal Pull-up Resistor in I/O Bank 0, 1, 2, and SPI Bank, and I/O Bank 3 on iCE65L01.**

VCCIO	Internal Pull-Up Current (V_{IN} = 0 V)	Effective Equivalent Resistor (V_{IN} = 0 V)
3.3V	85 µA	40 kΩ
2.5V	50 µA	50 kΩ
1.8V	20 µA	90 kΩ

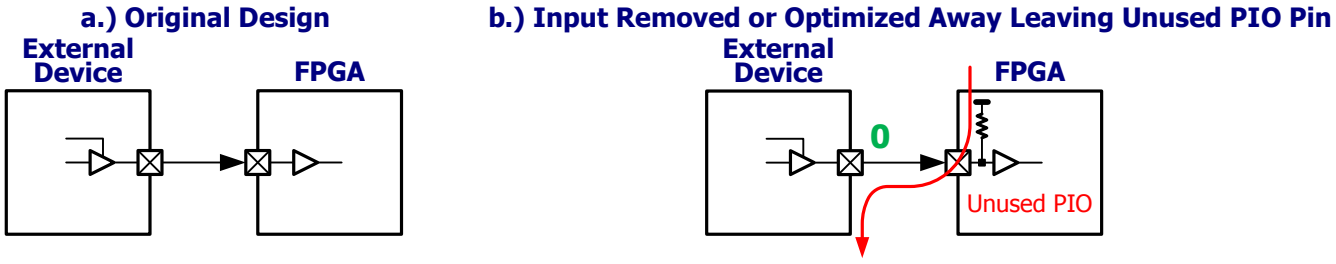
Figure 6: **Input with Internal Pull-Up Resistor Enabled (I/O Banks 0, 1, 2, and SPI Bank, and I/O Bank 3 on iCE65L01)**



4. FPGA Pin No Longer Used but Still Driven by External Device (I/O Banks 0, 1, 2, and SPI Bank, and I/O Bank 3 on iCE65L01)

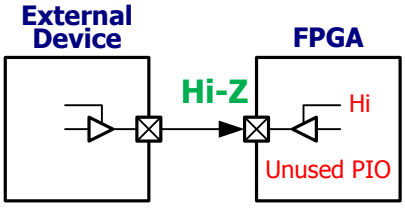
Hidden power wasters sometimes inadvertently sneak into designs. An FPGA input signal, shown in Figure 7a, may no longer be used in a later revision of the design, or the input signal may have been optimized away by the iCEcube software, both cases shown in Figure 7b. Being an unused PIO pin, the iCEcube development software automatically defines the FPGA pin as an input with an internal pull-up resistor, if the PIO pin is in I/O Bank 0, 1, 2 or the SPI Bank or I/O Bank 3 on the iCE65L01 FPGA.

Figure 7: Inputs That Are No Longer Used or Are Optimized Away



One possible solution is to define the unused FPGA PIO pin as a three-state output, as shown in Figure 8. The external device has full control over the logic level without causing additional FPGA power consumption.

Figure 8: **Possible Solution for Inputs That Are No Longer Used or Are Optimized Away**

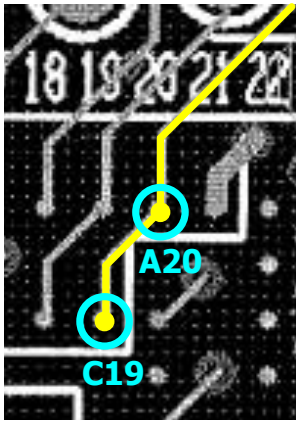


5. Internal Pull-up Resistor Not Disabled on Feed-Through Pad

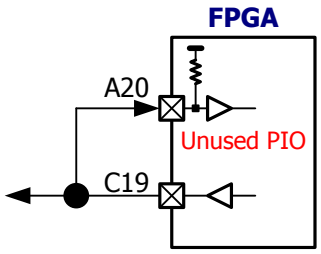
Printed circuit board (PCB) designers sometimes use unused PIO pin pads to route through to inner balls on a package, as shown in Figure 9a. This technique potentially reduces PCB layers and cost. In this example, package ball C19 is an output and the pad associated with ball A20 is a route-through connection. However, the unused PIO pad must be configured appropriately. By default, unused PIO pins in I/O Banks 0, 1, 2, or the SPI bank are inputs with the internal pull-up resistor enabled, as shown in Figure 9b. In this example, this configuration consumes power any time the output (ball C19) drives Low because of the internal pull-up resistor in the unused pad, used as a feed-through (ball A20).

Figure 9: **Feed-through Pads Affect Power Consumption**

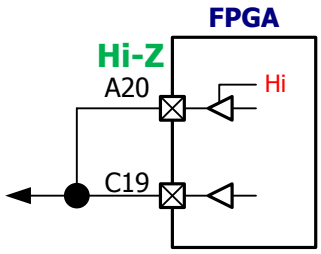
a.) Unused PIO Pad as a Feed-through



b.) Unused PIO Burns Power



c.) Three-State Saves Power

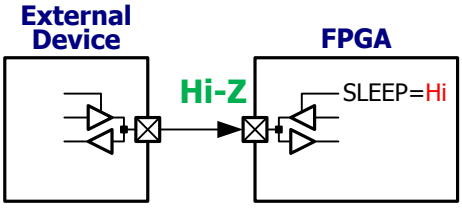


To reduce power consumption, define the unused pad as a three-state output, forced into the high-impedance (Hi-Z) state.

6. Bus Fight on Powered-down I/O Bank

To save power, individual FPGA I/O Banks can be turned off. To avoid potential power-consuming bus conflicts, three-state all the outputs within the bank before turning off the I/O bank, as shown in Figure 10. Unless placed in the high-impedance state (Hi-Z), a Low-driving output will continue to drive Low and potentially conflict with another driver, thereby consuming unnecessary power.

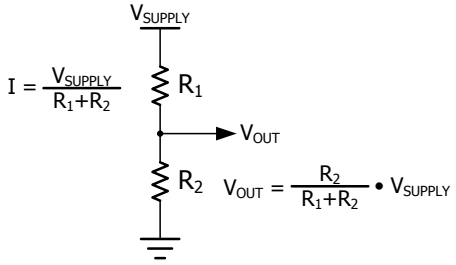
Figure 10: **Three-state FPGA Outputs Before Powering Down I/O Bank Power**



7. Resistor Dividers

Resistor voltage dividers, shown in Figure 11, often appear in digital designs, specifically to create reference voltages, for Thevenin termination, or to create special voltage levels. The primary drawback of resistor dividers is that they **constantly** consume power. Such circuits must be eliminated or optimized to reduce power consumption

Figure 11: **Resistor Voltage Divider**



The resistor-divider output voltage is the ratio of the series resistor values; the actual value of the resistors does not matter as long as the relationship of their values holds. Using larger resistor values results in lower power consumption.

8. Processor Download of Configuration Bitstream Not using Latest Code

Instead of configuring from internal Nonvolatile Configuration Memory (NVCM) or from an external SPI serial PROM, some applications download the FPGA configuration bitstream from an external processor. For lowest-power consumption for such applications, use the latest configuration 'C' code example from SiliconBlue. The latest revision properly turns off the Nonvolatile Configuration Memory (NVCM) to reduce power.

Other Power-Saving Techniques

The following are some additional techniques to reduce FPGA power consumption.

Select Low-Voltage Options; Use Lowest Possible VCCIO Voltage

As shown in Equation 3 and Equation 4, both static and dynamic power consumption increase with voltage, especially dynamic power, which grows exponentially with increased voltage. When possible, use lower-voltage versions of external components to save power. Similarly, use a lower VCCIO voltage for the attached FPGA I/O bank.

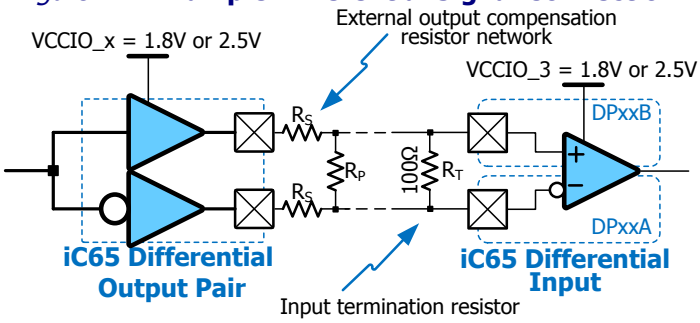
$$Static\ Power = Voltage \bullet Current \qquad \text{[Equation 3]}$$

$$Dynamic\ Power = Frequency \bullet Capacitance \bullet (Voltage)^2 \qquad \text{[Equation 4]}$$

Disable LVDS Output Drivers When Not in Use

Figure 12 shows an example LVDS, SubLVDS, or other differential signal connection. This specific example shows an iCE65 FPGA on both ends of the connection, but the iCE65 FPGA might be just one end.

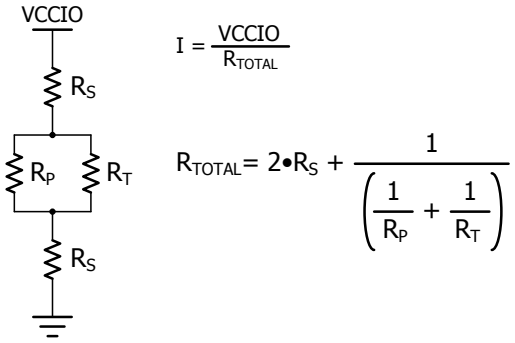
Figure 12: **Example Differential Signal Connection**



As a differential output driver, the iCE65 FPGA requires some external output compensation resistors. Similarly, there is typically an input termination resistor at the receiver input.

Figure 13 shows a static DC view of this connection. Being a differential output, one side of the driver is always High while the other is always Low. This approximates a constant voltage, VCCIO, across the resistor network. The DC current draw is the voltage divided by the effective total resistance of the network, as shown in Figure 13.

Figure 13: **Static Current of Differential Connection**



Using the recommended resistor values from the iCE65 data sheet for an LVDS connection (R_S = 150 Ω , R_P = 140 Ω , R_T = 100 Ω), the total effective resistance is about 358 Ω. Consequently, at VCCIO = 2.5 V, the DC current is about 7 mA per pin and the static power consumption is about 17.5 mW per pin.

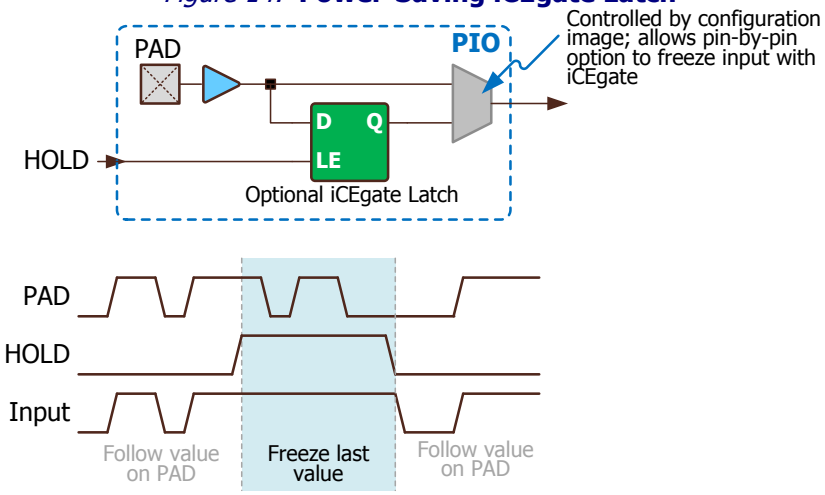
To reduce power consumption when not transmitting data, simply drive both differential output pins to the same logic level or force one output to the high-impedance state (Hi-Z). Either solution works as it eliminates the voltage differential across the resistor network.

Double-check that the differential receiver can tolerate this condition—both inputs at same voltage, either at VCCIO or at ground. The iCE65 differential receiver accommodates both these conditions.

Use iCEgate Feature to Block Input Transitions

CMOS logic consumes power any time that it switches. To reduce FPGA power consumption, block input transitions on any momentarily unused input pins by adding the iCEgate feature to the application, show in Figure 14. Each of the four I/O banks has its own iCEgate control input.

Figure 14: **Power-Saving iCEgate Latch**



For additional information on using the iCEgate feature, please refer to the following application note.

AN002: Using iCEgate Blocking for Ultra-Low Power
www.siliconbluetech.com/media/downloads/AN2iCEGATErev1.1.pdf

Revision History

Version	Date	Description
1.0	4-MAY-2010	Initial release.

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