iCEman65 P-Series Evaluation Kit User Guide

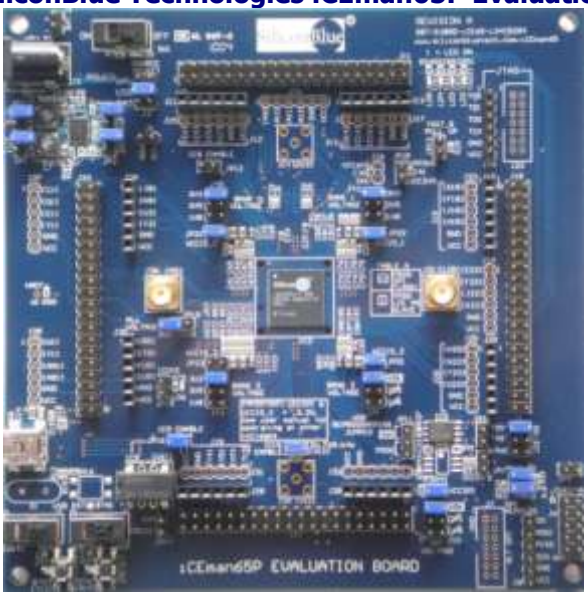
December 10, 2010 (1.1) **Preliminary**

- **Evaluation and development platform for SiliconBlue Technologies iCE65P ultra low-power programmable logic family**
  - iCE65P04
    - 3,520 logic cells
      - Approximately 200,000 system gates
      - Equivalent to about 2,700 macrocells
    - Phase-locked loop (PLL)
      - Clock frequency synthesis
      - Phase shifting; dynamic or static
    - 80Kbits of fast, on-chip RAM
  - 284-ball chip-scale BGA package
    - 172 programmable I/O pins
    - Four I/O banks, each with a selectable I/O voltage
- **8Mx16 CellularRAM (128Mbit)**
  - Asynchronous or synchronous operation
  - Burst data rates up to 160 Mbytes/second
- **Six-channel LVDS/SubLVDS input and output interface** *(some models)*
- **Extensive I/O expansion**
  - Four 40-pin ribbon cable connectors
  - Eight 6-pin peripheral module PMOD connectors
  - Available, affordable, off-the-shelf accessory boards
- **Selectable I/O bank voltages**
  - Choose 3.3V, 2.5V, or 1.8V
  - Isolation jumper for accurate power measurement
- **Multiple clock inputs**
  - 32.768 kHz oscillator on board
  - Socketed 27.0 MHz half-size oscillator
  - SMA-style clock input/output
  - Three additional unpopulated SMA clock inputs
- **SPI configuration interface**
  - 8Mbit SPI serial Flash PROM; store up to four independent configuration images
  - iCE65P slave SPI download interface
  - Requires a programming cable, sold separately
    - SiliconBlue iCEcable Interface, or
    - DediProg SF100 Flash Programmer

Overview

The iCEman65P evaluation board, pictured in Figure 1, is designed as an applications development and evaluation platform for the SiliconBlue Technologies ultra low-power iCE65P programmable logic family. The iCE65P evaluation board provides for extensive I/O expansion and voltage flexibility. Very few of the iCE65P programmable I/O pins are dedicated to specific functions.

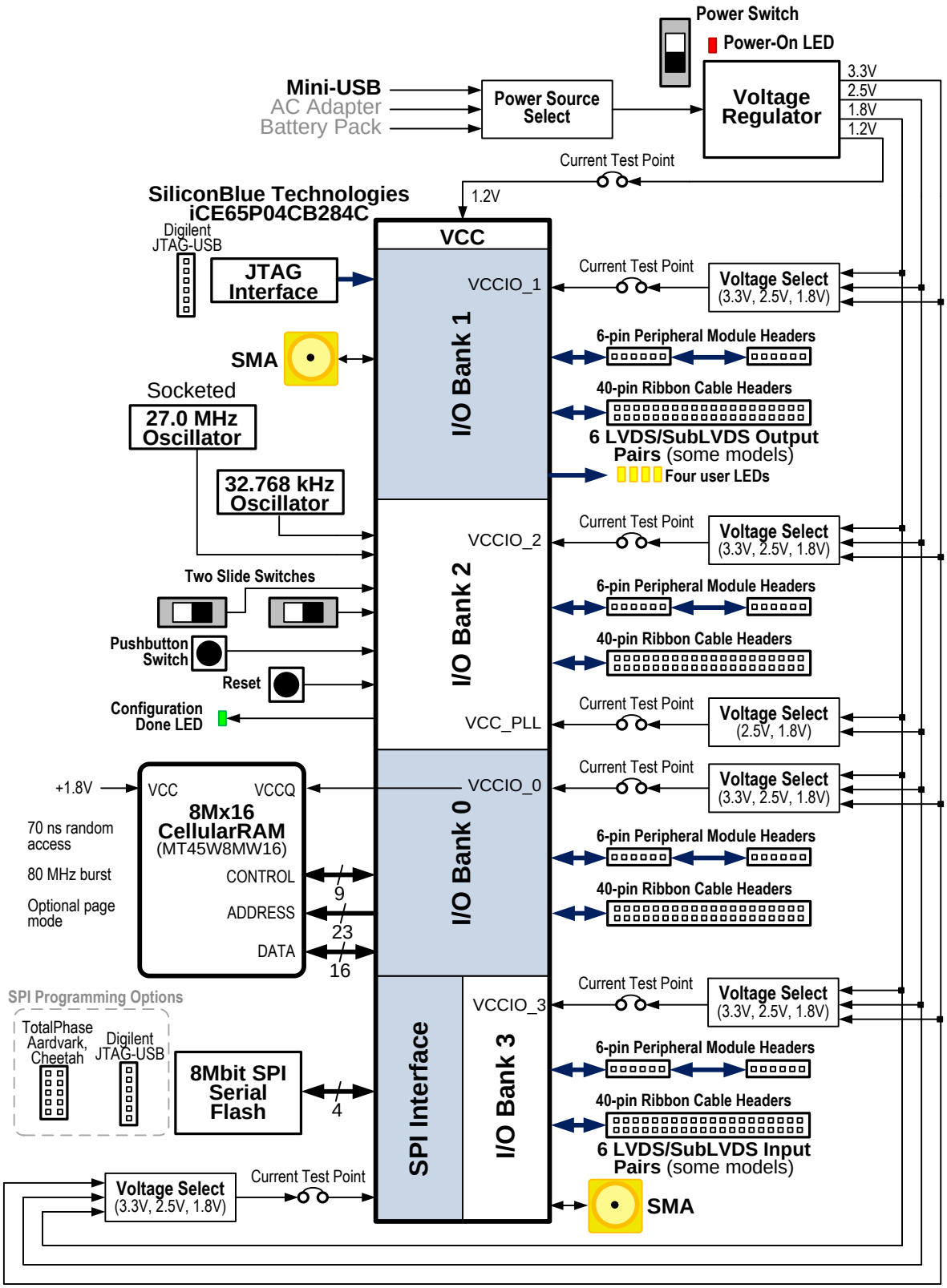
Figure 1: **SiliconBlue Technologies iCEman65P Evaluation Kit Board**



Block Diagram

Figure 2 provides a block diagram of the iCEman65P board, outlining major board components and interfaces. In the electronic version of this document, click on a feature to jump to the relevant section in the document.

Figure 2: **iCEman65P Board Block Diagram**



Switches and Buttons

By design, the iCEman65P board dedicates very few PIO pins to switches, pushbuttons, and LEDs. However, there are a few available on the board. Add other I/O functions with Compatible, Third-Party Peripheral Module (PMOD) Boards or other expansion boards.

Switches

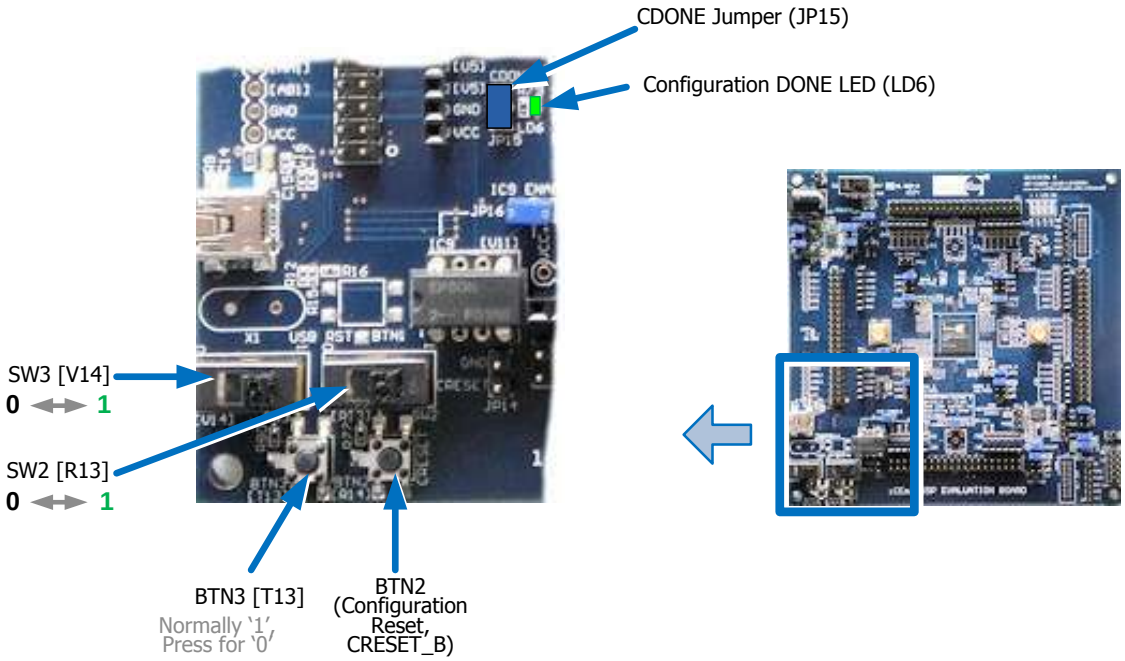
Power Supply Switch (SW1)

Slide switch SW1, shown in Figure 17 located in the upper left corner, enables the LP3906 regulator on the board. When power is applied, the red LED (LD1) next to the switch lights up.

User Switches (SW2, SW3)

Slide switches SW2 and SW3 are located in the lower left corner of the board, as shown in Figure 3. These switches are typically input signals for an iCE65P application. However, if the ColdBoot feature is enabled in the iCE65P configuration image, then these switches select which of the four possible configuration images is loaded during power on or after pressing and releasing the configuration reset, CRESET_B, pushbutton (BTN2).

Figure 3: **Switches, Pushbuttons, and LEDs**



After configuration, regardless if the ColdBoot feature is enabled or not, these switches are available as general-purpose control inputs to the iCE65P application. Optionally use these pins select one of four possible WarmBoot configuration images. See the iCE65P data sheet for additional information using ColdBoot and WarmBoot.

Table 1: **Slide Switches SW2 and SW3**

Switch	CB284 Ball	ColdBoot Function	WarmBoot Function	General-Purpose Function
SW2	R13	CBSEL0	Connect to port S0 on the SB_WARMBOOT primitive. Can also connect to other logic.	Connect to any logic function.
SW3	V14	CBSEL1	Connect to port S1 on the SB_WARMBOOT primitive. Can also connect to other logic.	Connect to any logic function.

Pushbuttons

Configuration Reset, CRESET_B (BTN2)

The BTN2 pushbutton is located in the lower left corner of the board, below the slide switches, adjacent to the Hirose FX2 connector, as pictured in Figure 3. The BTN2 pushbutton connects directly to the iCE65's active-Low configuration reset input, CRESET_B. Press this pushbutton switch at any time to reset the iCE65P device and force it to restart its configuration process. When jumper JP13 is installed (see Figure 20), then the CRESET_B pin is held in reset (Low) until the jumper is removed.

User Pushbutton (BTN3)

The BTN3 pushbutton is located in the lower left corner of the board, below the slide switches, closest to the corner, as pictured in Figure 3. Pushbutton BTN3 is primarily a general-purpose user input to the iCE65P device as shown in Table 2. However, BTN3 is also useful to demonstrate or evaluate the WarmBoot configuration operation.

BTN3 is normally High, or logic '1.' Press BTN3 to force the associated input Low, or to logic '0.'

Table 2: **Pushbutton Switch BTN3**

Switch	CB284 Ball	WarmBoot Function	General-Purpose Function
BTN3	T13	Connect to the BOOT port on the SB_WARMBOOT primitive. Press and release to cause a WarmBoot configuration operation.	Normally High. Press to force ball T13 Low.

LEDs

Power-On LED (LD1)

When power is applied to the board, LED LD1 lights up, indicating that the board is powered. This LED is located immediately adjacent to the power switch, as shown in Figure 17.

Configuration DONE LED (LD6)

When the iCE65P device is properly configured, the LD6 LED lights, although jumper JP15 must also be installed. See Figure 3.

Four User LEDs (LD5, LD4, LD3, LD2)

The iCEman65P includes four user LEDs, located in the upper right corner of the board as shown in Figure 4. These LEDs light only when the associated PIO pin drives High. There is no additional I/O current when these pins are unused or when the pins drive Low.

Figure 4: **Four User LEDs on Revision D Board or Later**

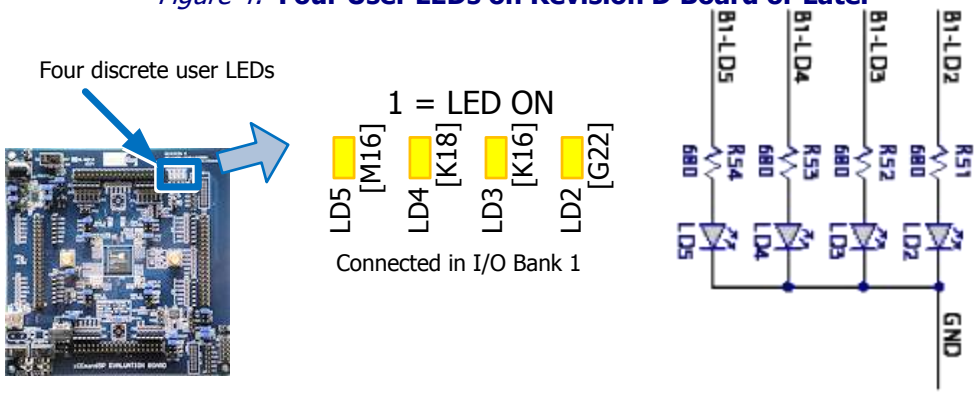


Table 3 lists the iCE65P ball numbers associated with each LED. All these PIO pins are in I/O Bank 1.

Table 3: **Four User LEDs**

LED	Schematic Name	Shared Connection	CB284 Ball
LD5 *(left-most)*	B1-LD5	N/A	[M16]
LD4	B1-LD4	N/A	[K18]
LD3	B1-LD3	N/A	[K16]
LD2 *(right-most)*	B1-LD2	N/A	[G22]

Clock Sources

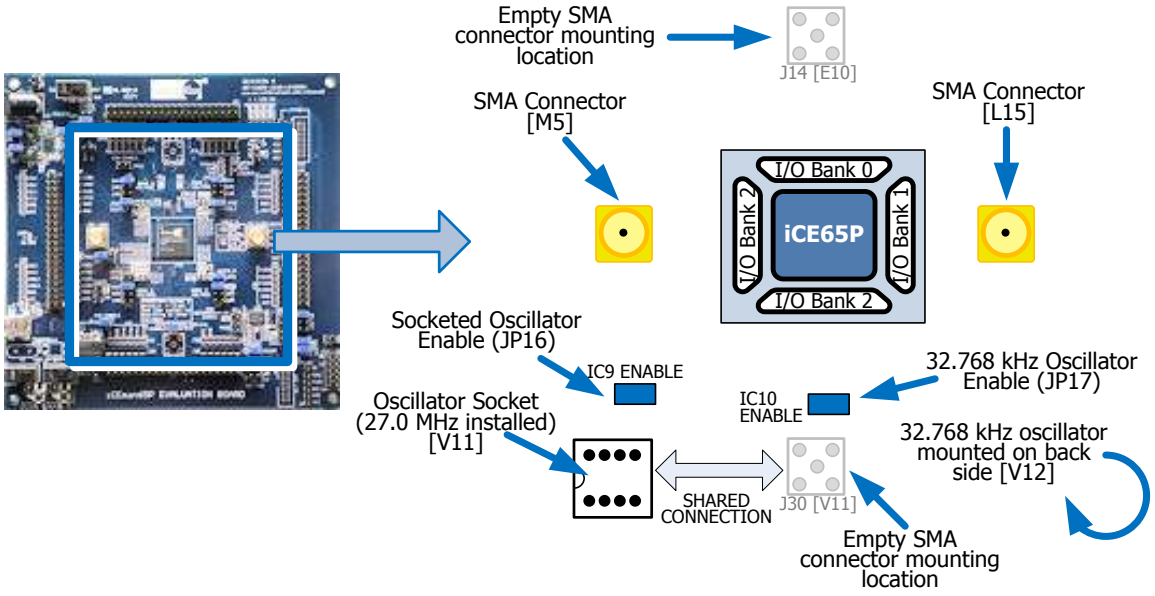
The iCE65P board has four default clock sources, as listed in Table 4 and depicted in Figure 5.

- 32.768 kHz Oscillator
- Socket Oscillator (IC9)
- SMA Clock Input/Output I/O Bank 1
- SMA Clock Input/Output I/O Bank 3

Table 4: **Default Clock Sources and Pin Connections**

Clock Source	iCE65P Ball	Clock Source Supply	Enable Control	Comment
32.768 kHz Oscillator	V12	VCCIO_2	JP17	Connects to global buffer input GBIN5
27.0 MHz Oscillator (socketed)	V11	VCCIO_2	JP16	Connects to global buffer input GBIN4
SMA connector (I/O Bank 1)	L18	VCCIO_1	None	Connects to global buffer input GBIN2
SMA connector (I/O Bank 3)	M5	VCCIO_3	None	Connects to global buffer input GBIN6

Figure 5: **Clock Sources**



32.768 kHz Oscillator

To demonstrate low-frequency operation, the iCEman65P evaluation board includes a 32.768 kHz oscillator, sometimes also called a 32K oscillator. This oscillator is enabled when jumper JP17 is installed, as shown in Figure 5.

The oscillator is physically mounted on the back side of the board. The oscillator is designed for 3.3V operation, so be sure that I/O Bank 2 is configured for 3.3V operation using jumper J41, shown in Figure 18.

To generate a 1 second period, divide the 32.768 kHz oscillator output using a 15-bit binary counter. The output from bit Q15 generates a one second clock period with a 50% duty cycle.

Socket Oscillator (IC9)

By default, the iCEman65P board includes a 27.0 MHz oscillator, which is installed in socket IC9 as shown in Figure 6. When installed, the oscillator is enabled when jumper JP16 is installed. When jumper JP16 is removed, then the oscillator is disabled.

The oscillator is designed for 3.3V operation, so be sure that I/O Bank 2 is configured for 3.3V operation using jumper J41, shown in Figure 18.

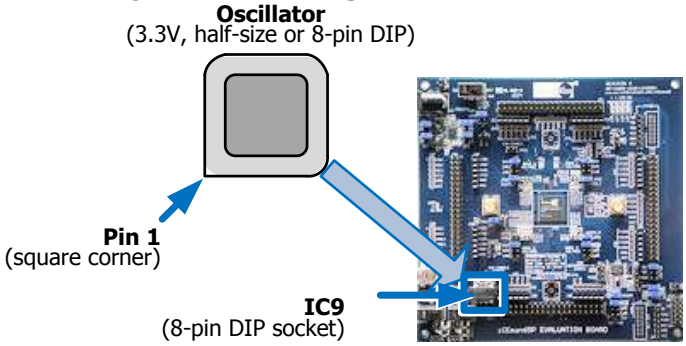
Using a Different Oscillator

To change to another frequency, simply remove the 32.0 MHz oscillator from the IC8 socket and replace it with a different, 3.3V oscillator packaged in either a half-size oscillator can or an 8-pin DIP package.

Installing an Oscillator

Insert the half-size oscillator into the 8-pin DIP socket labeled IC9. Be sure to align pin 1, the square corner of the oscillator, as shown in Figure 6. All other corners are rounded.

Figure 6: **Installing an Oscillator**



SMA Clock Input/Output

When shipped, the iCEman65P board has two SMA connectors, as shown in Figure 5. Use these connectors to supply a clock frequency from an external frequency generator. Optionally, supply an internally generated signal to the connector for easy external measurement with an oscilloscope or logic analyzer.

The SMA connectors attach to I/O Bank 1 and I/O Bank 3, so be sure that the I/O Bank voltage is compatible with the external clock source using jumper J42 (I/O Bank 1) and J43 (I/O Bank 3), shown in Figure 18.

Optional SMA Clock Inputs

As shown in Figure 5, the iCEman65P board has empty mounting locations for up to three additional SMA connectors. Each is associated with a specific I/O bank and global buffer. If using these SMA connectors, be sure that the I/O Bank voltage is compatible with the external clock source by adjusting the appropriate jumper shown in Figure 18.

Table 5: **Unpopulated SMA Connectors**

Unpopulated SMA Connections	I/O Bank	iCE65P Ball	Bank Power Supply	Comment
J14	0	E10	VCCIO_0	Shared connection with the CE# input on the CellularRAM. To use this SMA location, remove jumper JP12, which also disables the CellularRAM. Connects to global buffer input GBIN0.
J30	2	V11	VCCIO_2	Must remove or disable the clock oscillator in socket IC9 before using J30; as they share the same iCE65P package ball. Remove jumper JP16 to disable the oscillator. Connects to global buffer input GBIN4

To populate these locations, solder in a vertical, PCB mount, 50-ohm SMA RF/coaxial connector such as Molex part number 73391-0070 or a substitute.

40-pin Ribbon Cable Headers

The iCEman65P board has four 40-pin ribbon cable headers, located on the top, right, bottom and left edges of the board. As shown in Table 6, each header has an independent voltage supply, controlled by a jumper selection.

Table 6: **40-pin Ribbon Cable Headers**

Header Location	Header Designator	I/O Bank/ Voltage Source	Voltage Control	Pinout References
Top Edge	J11	I/O Bank 0 (VCCIO_0)	Jumper J40	Figure 7 Table 7
Right Edge	J18	I/O Bank 1 (VCCIO_1)	Jumper J42	Figure 8 Table 8
Bottom Edge	J27	I/O Bank 2 (VCCIO_2)	Jumper J41	Figure 10 Table 10
Right Edge	J33	I/O Bank 3 (VCCIO_3)	Jumper J43	Figure 11 Table 11

I/O Bank 0 (Top)

Figure 7 shows the ball connections for the iCE65P PIO pins that connect to the top-edge 40-pin header, J11. There are 36 PIO pins from I/O Bank 0 connected to the J11 header.

The header carries both +5V supply voltages and the VCCIO_0 supply, controlled by jumper header J40.

Figure 7: **Top 40-pin Header (J11) and BG284 Ball Connections**

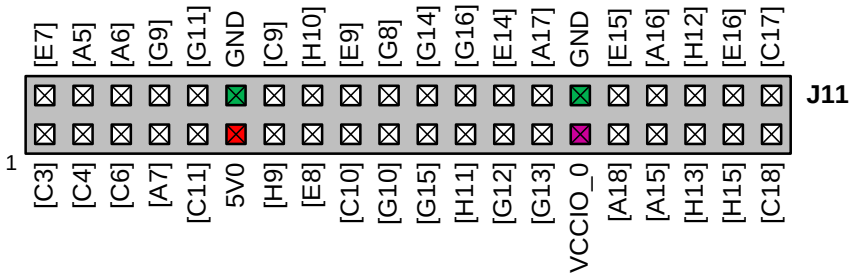


Table 7 provides a listing of the header connections.

Table 7: **Header J11 Pinout**

Shared	Schematic Name	CB284 Ball	Header J11		CB284 Ball	Schematic Name	Shared
RAM.A22	B0-IO00	[C3]	1	2	[E7]	B0-IO01	RAM.A19
RAM.D11	B0-IO02	[C4]	3	4	[A5]	B0-IO03	RAM.DQ15
RAM.A17	B0-IO04	[C6]	5	6	[A6]	B0-IO05	RAM.DQ13
RAM.DQ14	B0-IO06	[A7]	7	8	[G9]	B0-IO07	RAM.A0
RAM.DQ8	B0-IO08	[C11]	9	10	[G11]	B0-IO09	RAM.A5
	VCC5V0	**+5V DC**	**11**	**12**	**GND**	GND	
RAM.DQ12	B0-IO10	[H9]	13	14	[C9]	B0-IO11	RAM.DQ9
RAM.WAIT	B0-IO12	[E8]	15	16	[H10]	B0-IO13	RAM.DQ10
RAM.DQ0	B0-IO14	[C10]	17	18	[E9]	B0-IO15	RAM.A8
RAM.A1	B0-IO16	[G10]	19	20	[G8]	B0-IO17	RAM.A3
RAM.A4	B0-IO18	[G15]	21	22	[G14]	B0-IO19	RAM.A2
RAM.DQ1	B0-IO20	[H11]	23	24	[G16]	B0-IO21	RAM.CRE
RAM.ADV#	B0-IO22	[G12]	25	26	[E14]	B0-IO23	RAM.A12
RAM.A9	B0-IO24	[G13]	27	28	[A17]	B0-IO25	RAM.DQ7
	VCCIO_0	**VCCIO_0**	**29**	**30**	**GND**	GND	
RAM.A20	B0-IO26	[A18]	31	32	[E15]	B0-IO27	RAM.A22
RAM.DQ6	B0-IO28	[A15]	33	34	[A16]	B0-IO29	RAM.DQ5
RAM.DQ3	B0-IO30	[H13]	35	36	[H12]	B0-IO31	RAM.DQ2
RAM.A16	B0-IO32	[H15]	37	38	[E16]	B0-IO33	RAM.A11
RAM.A10	B0-IO34	[C18]	39	40	[C17]	B0-IO35	RAM.A13

I/O Bank 1 (Right)

Figure 8 shows the ball connections for the iCE65P PIO pins that connect to the right-edge 40-pin header, J18. There are 36 PIO pins from I/O Bank 1 connected to the J18 header.

The header carries both +5V supply voltages and the VCCIO_1 supply, controlled by jumper header J42.

Figure 8: **Right 40-pin Header (J18) and BG284 Ball Connections**

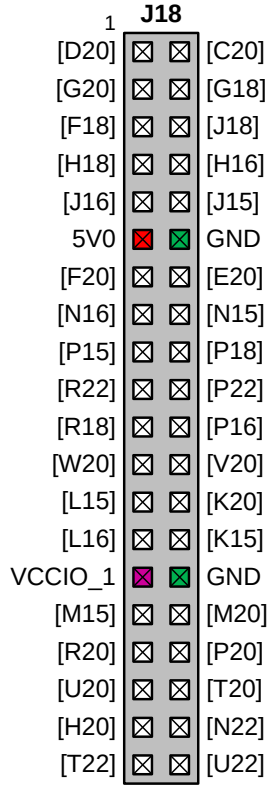


Table 8 provides a listing of the header connections.

Table 8: **Header J18 Pinout**

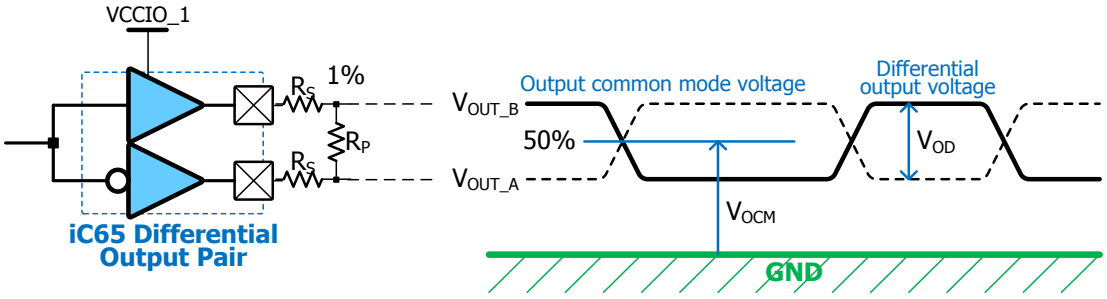
Shared	Schematic Name	CB284 Ball	Header J18		CB284 Ball	Schematic Name	Shared
	B1-IO00	[D20]	1	2	[C20]	B1-IO01	
	B1-IO02	[G20]	3	4	[G18]	B1-IO03	J19.1
J19.2	B1-IO04	[F18]	5	6	[J18]	B1-IO05	J19.3
J19.4	B1-IO06	[H18]	7	8	[H16]	B1-IO07	
	B1-IO08	[J16]	9	10	[J15]	B1-IO09	
	VCC5V0	**+5V DC**	**11**	**12**	**GND**	GND	
LVDS	B1-DP00_P	[F20]	13	14	[E20]	B1-DP00_N	LVDS
LVDS	B1-DP01_P	[N16]	15	16	[N15]	B1-DP01_N	LVDS
LVDS	B1-DP02_P	[P15]	17	18	[P18]	B1-DP02_N	LVDS
LVDS	B1-DP03_P	[R22]	19	20	[P22]	B1-DP03_N	LVDS
LVDS	B1-DP04_P	[R18]	21	22	[P16]	B1-DP04_N	LVDS
LVDS	B1-DP05_P	[W20]	23	24	[V20]	B1-DP05_N	LVDS
	B1-IO10	[L15]	25	26	[K20]	B1-IO11	
	B1-IO12	[L16]	27	28	[K15]	B1-IO13	
	VCCIO_1	**VCCIO_1**	**29**	**30**	**GND**	GND	
	B1-IO14	[M15]	31	32	[M20]	B1-IO15	
	B1-IO16	[R20]	33	34	[P20]	B1-IO17	
	B1-IO18	[U20]	35	36	[T20]	B1-IO19	
J20.1	B1-IO20	[H20]	37	38	[N22]	B1-IO21	
J20.3	B1-IO22	[T22]	39	40	[U22]	B1-IO23	

Differential Output Build Options

The iCEman65P board has three different build options.

- In the Standard version, all 36 I/O pins are single-ended LVCMOS I/Os. The VCCIO_1 voltage can be set to 1.8V, 2.5V, or 3.3V as required for the application.
- In the LVDS version, the output termination resistors are installed, creating six LVDS-compatible output channels. When used as LVDS-compatible differential outputs, set VCCIO_1 to 2.5V.
- In the SubLVDS version, the output termination resistors are installed, creating six SubLVDS-compatible output channels. When used as SubLVDS-compatible differential outputs, set VCCIO_1 to 1.8V.

Figure 9: **Differential Output Specifications**



Output common mode voltage: $V_{OCM} = \frac{VCCIO\_1}{2} \pm \Delta V_{OCM}$

Differential output voltage: $V_{OD} = |V_{OUT\_B} - V_{OUT\_A}|$

Table 9: **Recommended Operating Conditions for Differential Outputs**

Build Option	VCCIO_1 (V)			Ω		V_{OD} (mV)			V_{OCM} (V)		
	Min	Nom	Max	R_S	R_P	Min	Nom	Max	Min	Nom	Max
Standard	1.71	—	3.47	0	—	N/A	N/A	N/A	N/A	N/A	N/A
LVDS	2.38	2.50	2.63	150	140	300	350	400	$\frac{VCCIO}{2} - 0.15$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.15$
SubLVDS	1.71	1.80	1.89	270	120	100	150	200	$\frac{VCCIO}{2} - 0.10$	$\frac{VCCIO}{2}$	$\frac{VCCIO}{2} + 0.10$

I/O Bank 2 (Bottom)

Figure 10 shows the ball connections for the iCE65P PIO pins that connect to the bottom-edge 40-pin header, J27. There are 36 PIO pins from I/O Bank 2 connected to the J27 header.

The header carries both +5V supply voltages and the VCCIO_2 supply, controlled by jumper header J41.

Figure 10: **Bottom 40-pin Header (J27) and BG284 Ball Connections**

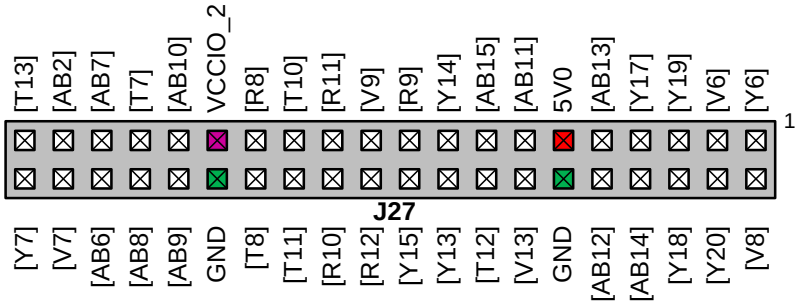


Table 10 provides a listing of the header connections.

Table 10: **Header J27 Pinout**

Shared	Schematic Name	CB284 Ball	Header J27		CB284 Ball	Schematic Name	Shared
	B2-IO00	[Y6]	1	2	[V8]	B2-IO01	
	B2-IO02	[V6]	3	4	[Y20]	B2-IO03	J28.1
J28.2	B2-IO04	[Y19]	5	6	[Y18]	B2-IO05	J28.3
J28.4	B2-IO06	[Y17]	7	8	[AB14]	B2-IO07	
	B2-IO08	[AB13]	9	10	[AB12]	B2-IO09	
	VCC5V0	**+5V DC**	**11**	**12**	**GND**	GND	
	B2-IO10	[AB11]	13	14	[V13]	B2-IO11	
	B2-IO12	[AB15]	15	16	[T12]	B2-IO13	
	B2-IO14	[Y14]	17	18	[Y13]	B2-IO15	
	B2-IO16	[R9]	19	20	[Y15]	B2-IO17	
	B2-IO18	[V9]	21	22	[R12]	B2-IO19	
	B2-IO20	[R11]	23	24	[R10]	B2-IO21	
	B2-IO22	[T10]	25	26	[T11]	B2-IO23	
	B2-IO24	[R8]	27	28	[T8]	B2-IO25	
	VCCIO_2	**VCCIO_2**	**29**	**30**	**GND**	GND	
	B2-IO26	[AB10]	31	32	[AB9]	B2-IO27	
	B2-IO28	[T7]	33	34	[AB8]	B2-IO29	
	B2-IO30	[AB7]	35	36	[AB6]	B2-IO31	
	B2-IO32	[AB2]	37	38	[V7]	B2-IO33	
BTN3, J9.1, pull-up	B2-IO34	[T13]	39	40	[Y7]	B2-IO35	J29.2

I/O Bank 3 (Left)

Figure 11 shows the ball connections for the iCE65P PIO pins that connect to the right-edge 40-pin header, J33. There are 36 PIO pins from I/O Bank 1 connected to the J33 header.

The header carries both +5V supply voltages and the VCCIO_3 supply, controlled by jumper header J43.

Figure 11: **Left 40-pin Header (J33) and BG284 Ball Connections**

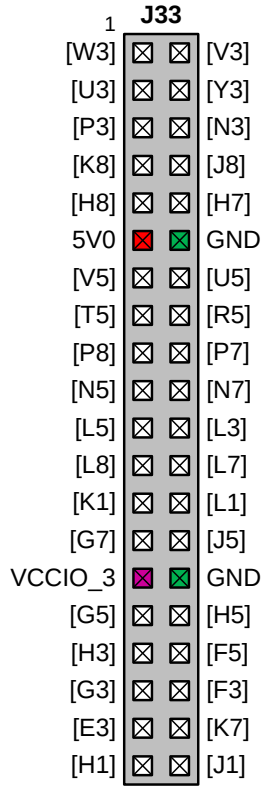


Table 11 provides a listing of the header connections.

Table 11: **Header J33 Pinout**

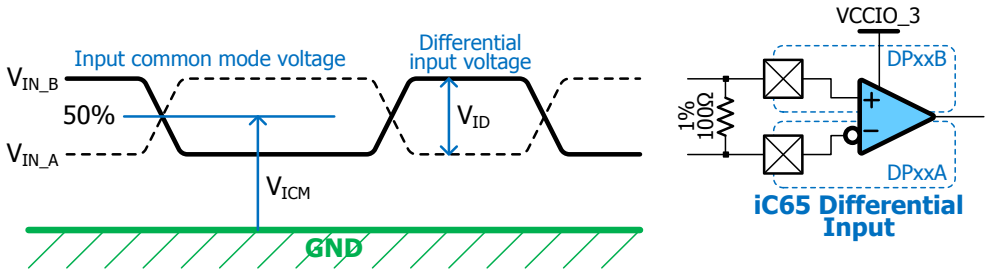
Shared	Schematic Name	CB284 Ball	Header J33		CB284 Ball	Schematic Name	Shared
	B3-IO00	[W3]	1	2	[V3]	B3-IO01	
J34.3	B3-IO02	[U3]	3	4	[Y3]	B3-IO03	J34.4
	B3-IO04	[P3]	5	6	[N3]	B3-IO05	
J34.2	B3-IO06	[K8]	7	8	[J8]	B3-IO07	J34.1
	B3-IO08	[H8]	9	10	[H7]	B3-IO09	
	VCC5V0	**+5V DC**	**11**	**12**	**GND**	GND	
J35.4	B3-DP19_P	[V5]	13	14	[U5]	B3-DP19_N	J35.3
J35.2	B3-DP20_P	[T5]	15	16	[R5]	B3-DP20_N	J35.1
	B3-DP21_P	[P8]	17	18	[P7]	B3-DP21_N	
	B3-DP22_P	[N5]	19	20	[N7]	B3-DP22_N	
GBIN7	B3-DP23_P	[L5]	21	22	[L3]	B3-DP23_N	
	B3-DP24_P	[L8]	23	24	[L7]	B3-DP24_N	
	B3-IO10	[K1]	25	26	[L1]	B3-IO11	
	B3-IO12	[G7]	27	28	[J5]	B3-IO13	
	VCCIO_1	**VCCIO_3**	**29**	**30**	**GND**	GND	
	B3-IO14	[G5]	31	32	[H5]	B3-IO15	
	B3-IO16	[H3]	33	34	[F5]	B3-IO17	
	B3-IO18	[G3]	35	36	[F3]	B3-IO19	
	B3-IO20	[E3]	37	38	[K7]	B3-IO21	
	B3-IO22	[H1]	39	40	[J1]	B3-IO23	

Differential Input Build Options

The iCEman65P board has three different build options.

- In the Standard version, all 36 I/O pins are single-ended LVCMOS I/Os. The VCCIO_3 voltage can be set to 1.8V, 2.5V, or 3.3V as required for the application.
- In the LVDS version, the input termination resistors are installed, creating six LVDS-compatible input channels. When used as LVDS-compatible differential inputs, set VCCIO_3 to 2.5V.
- In the SubLVDS version, the input termination resistors are installed, creating six SubLVDS-compatible input channels. When used as SubLVDS-compatible differential inputs, set VCCIO_3 to 1.8V.

Figure 12: **Differential Input Specifications**



Input common mode voltage:

$$V_{ICM} = \frac{VCCIO\_3}{2} \pm \Delta V_{ICM}$$

Differential input voltage:

$$V_{ID} = |V_{IN\_B} - V_{IN\_A}|$$

Table 12: **Recommended Operating Conditions for Differential Inputs**

Build Option	VCCIO_3 (V)			R_T (Ω)	V_{ID} (mV)			V_{ICM} (V)		
	Min	Nom	Max		Min	Nom	Max	Min	Nom	Max
Standard	1.71	—	3.47	None	—	—	—	—	—	—
LVDS	2.38	2.50	2.63	100	250	350	450	$\frac{VCCIO\_3}{2} - 0.30$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.30$
SubLVDS	1.71	1.80	1.89	100	100	150	200	$\frac{VCCIO\_3}{2} - 0.25$	$\frac{VCCIO\_3}{2}$	$\frac{VCCIO\_3}{2} + 0.25$

Compatible Cabling

The 40-pin headers support IDC flat-ribbon assemblies with 0.1-inch pitch at least on socket connector types. The connectors are arranged as two rows of 20 connectors each (2x20). Both direct and twisted-pair versions of these cables are available from a variety of vendors.

- 2x20 Ribbon Cable, 0.1" Spacing
- IDE Hard Disk Drive (HDD) Cable

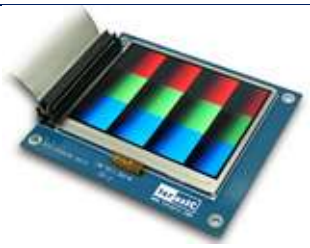
Compatible Third-Party Boards

The 40-pin header is designed to work with the following third-party products. These products require that the iCEman65P board be powered by an external AC adapter or from USB. The products listed in Table 13 connect to the iCEman65P board using a 40-wire ribbon cable included with the kits.

These products have not yet been verified to work with the iCEman65P board.

SiliconBlue Technologies makes no warranty or guarantee of compatibility for these third-party products.

Table 13: **Available Expansion Boards for 40-Pin Header**

Board	Description, Link to More Information
	**1.3 Megapixel Digital Camera Module** www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=39&No=50
	**5 Mega Pixel Digital Camera Package** www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=68&No=281
	**3.6-inch Digital Panel Kit** www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=39&No=78
	**4.3-inch Ultra-High Resolution LCD Touch Panel Kit** www.terasic.com.tw/cgi-bin/page/archive.pl?Language=English&CategoryNo=39&No=213

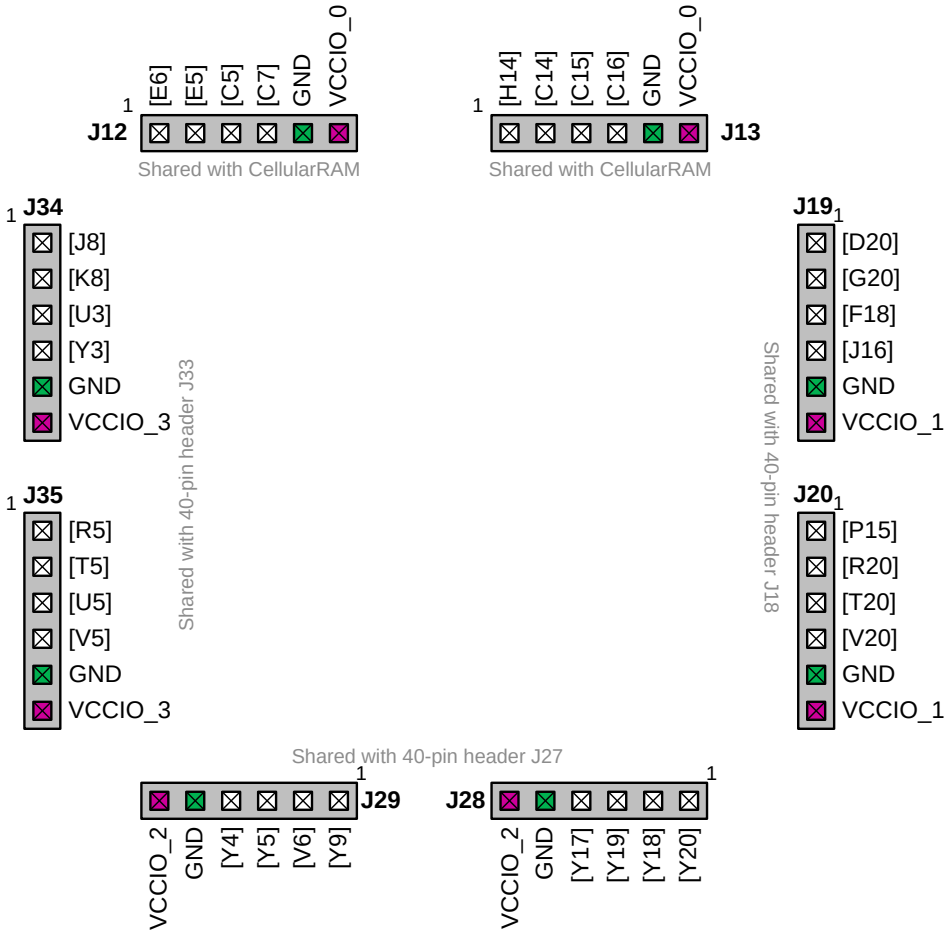
Peripheral Module (PMOD) Connectors

The iCE65P evaluation board includes eight 6-pin Peripheral Module (PMOD) connectors, as shown in Figure 13 and listed in Table 14. By default, each of the four I/O banks has two PMOD connectors. Both PMOD connectors within a bank are controlled by a common voltage selection jumper. Many of the PMOD connectors share signals with the other expansion connectors in the same I/O bank.

Table 14: **6-pin Peripheral Module Headers**

Header Location	Header Designator	I/O Bank/ Voltage Source	Voltage Selection	Pinout References	
Top Edge	J12 (left)	I/O Bank 0 (VCCIO_0)	Jumper J40	Figure 13	Table 15
	J13 (right)				Table 16
Right Edge	J19 (top)	I/O Bank 1 (VCCIO_1)	Jumper J42	Figure 13	Table 17
	J20 (bottom)				Table 18
Bottom Edge	J29 (left)	I/O Bank 2 (VCCIO_2)	Jumper J41	Figure 13	Table 19
	J28 (right)				Table 20
Left Edge	J34 (top)	I/O Bank 3 (VCCIO_3)	Jumper J43	Figure 13	Table 22
	J35 (bottom)				Table 21

Figure 13: **Digilent Peripheral Module (PMOD) Location and BG284 Ball Connections**



I/O Bank 0 (Top)

The top PMOD headers share connection with the CellularRAM.

Top Left (J12)

Table 15: **Top-Left PMOD Header (J12)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[E6]	B0-PM-A1	CellularRAM UB#
2	[E5]	B0-PM-A2	CellularRAM LB#
3	[C5]	B0-PM-A3	CellularRAM OE#
4	[C7]	B0-PM-A4	CellularRAM WE#
GND	GND	GND	—
VCC	VCCIO_0	VCCIO_0	Voltage selected using jumper J40

Top Right (J13)

Table 16: **Top-Right PMOD Header (J13)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[H14]	B0-IO36	CellularRAM DQ4
2	[C14]	B0-IO37	CellularRAM A6
3	[C15]	B0-IO38	CellularRAM A7
4	[C16]	B0-IO39	CellularRAM A15
GND	GND	GND	—
VCC	VCCIO_0	VCCIO_0	Voltage selected using jumper J40

I/O Bank 1 (Right)

Right Top (J19)

Table 17: **Right-Top PMOD Header (J19)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[G18]	B1-IO03	J18.4
2	[F18]	B1-IO04	J18.5
3	[J18]	B1-IO05	J18.6
4	[H18]	B1-IO06	J18.7
GND	GND	GND	—
VCC	VCCIO_1	VCCIO_1	Voltage selected using jumper J42

Right Bottom (J20)

Table 18: **Right-Bottom PMOD Header (J20)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[H20]	B1-IO20	J18.37
2	[N22]	B1-IO21	J18.36
3	[T22]	B1-IO22	J18.39
4	**N.C.**	B1-IO23	J18.40 **(*** NOT CONNECTED TO iCE65P04 ***)**
GND	GND	GND	—
VCC	VCCIO_1	VCCIO_1	Voltage selected using jumper J42

I/O Bank 2 (Bottom)

Bottom Left (J29)

Table 19: **Bottom-Left PMOD Header (J29)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[T13]	B2-IO34	J27.39, BTN3 **(*** USE AS INPUT ONLY ***)**
2	[Y7]	B2-IO35	J27.40
3	[Y5]	B2-IO36	
4	[Y4]	B2-IO38	J32.A44
GND	GND	GND	—
VCC	VCCIO_1	VCCIO_2	Voltage selected using jumper J41

Bottom Right (J28)

Table 20: **Bottom-Right PMOD Header (J28)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[Y20]	B2-IO03	J27.4
2	[Y19]	B2-IO04	J27.5
3	[Y18]	B2-IO05	J27.6
4	[Y17]	B2-IO06	J27.7
GND	GND	GND	—
VCC	VCCIO_1	VCCIO_2	Voltage selected using jumper J41

I/O Bank 3 (Left)

Right Top (J34)

Table 21: **Right-Top PMOD Header (J34)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[J8]	B3-IO07	J33.8
2	[K8]	B3-IO06	J33.7
3	[U3]	B3-IO02	J33.2
4	[Y3]	B3-IO03	J33.5
GND	GND	GND	—
VCC	VCCIO_3	VCCIO_3	Voltage selected using jumper JP43

Right Bottom (J35)

Table 22: **Right-Bottom PMOD Header (J35)**

Pin	CB284 Ball	Schematic Name	Shared Connections/Notes
1	[R5]	B3-DP20_N	J33.16
2	[T5]	B3-DP20_P	J33.15
3	[U5]	B3-DP19_N	J33.14
4	[V5]	B3-DP19_P	J33.13
GND	GND	GND	—
VCC	VCCIO_3	VCCIO_3	Voltage selected using jumper J423

Compatible, Third-Party Peripheral Module (PMOD) Boards

Table 23 lists the available third-party expansion boards that plug into one of the Peripheral Module (PMOD) connectors on the iCEman65P board. PMOD modules are available for a variety of functions. Also see the list of Other Useful Peripheral Module Accessories.

- **Prototyping/Breadboarding**
- **Displays**
- **Inputs, Switches, Pushbuttons**
- **Serial Interfaces**
- **Analog/Digital, Digital/Analog Conversion**
- **Memory**
- **Sensors**
- **Audio**
- **Connectors**
- **Motor Control/High-Drive Outputs**

These products have not yet been verified to work with the iCEman65P board.

SiliconBlue Technologies makes no warranty or guarantee of compatibility for these third-party products.

Table 23: **Available Third-Party Peripheral Module (PMOD) Boards**

Board	Description, Link to More Information
Prototyping/Breadboarding	
	**PMOD Breadboard Prototyping Board** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-BB&Nav1=Products&Nav2=Peripheral Uses a 2x6-pin header. Recommend 6-pin headers and a 2x6-pin splitter cable.
Displays	
	**Four Discrete LEDs** www.digilentinc.com/Data/Products/PMOD-LED/pmod-led-rm.pdf Verified for compatibility.
	**Dual Seven-Segment LED Module** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-SSD&Nav1=Products&Nav2=Peripheral NOTE: Requires two PMOD connections on the iCEman65P board Verified for compatibility. Recommend 6-pin headers and two 6-pin extension cables.
	**16x2 Character LCD Display** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-CLS&Nav1=Products&Nav2=Peripheral NOTE: Requires two PMOD connections on the iCEman65P board Recommend 6-pin headers and two 6-pin extension cables.
Inputs, Switches, Pushbuttons	
	**Four Debounced Pushbutton Switches** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-BTN&Nav1=Products&Nav2=Peripheral
	**Four Slide Switches** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-SWITCH&Nav1=Products&Nav2=Peripheral

Board	Description, Link to More Information
	**Rotary Shaft Encoder and Pushbutton Module** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-ENC&Nav1=Products&Nav2=Peripheral
	**Debounced Digital Inputs with Input Protection** www.digilentinc.com/Data/Products/PMOD-DIN1/pmod-din1-rm.pdf
Serial Interfaces	
	**PS/2-Style Mouse/Keyboard Interface** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-PS2&Nav1=Products&Nav2=Peripheral
	**RS-232 Serial Port Interface** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-RS232&Nav1=Products&Nav2=Peripheral
Analog/Digital, Digital/Analog Conversion	
	**Two-Channel, 12-bit Analog-to-Digital Converter (ADC)** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-AD1&Nav1=Products&Nav2=Peripheral
	**Four-Channel, Digital-to-Analog Converter (DAC)** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-DA1&Nav1=Products&Nav2=Peripheral
	**Four-Channel, 12-bit Digital-to-Analog Converter (DAC)** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-DA2&Nav1=Products&Nav2=Peripheral
Memory	
	**PMOD Secure Digital (SD) Media Card Interface** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-SD&Nav1=Products&Nav2=Peripheral Uses a 2x6-pin header. Recommend 6-pin headers and a 2x6-pin splitter cable.
	**16 Mbit SPI Serial Flash PROM (M25P16)** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-SF&Nav1=Products&Nav2=Peripheral NOTE: This PROM is compatible with the 8 Mbit SPI Serial Flash PROM already on the iCEman 65 board.

Sensors	
	**Infrared Light Detector Module** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-LS1&Nav1=Products&Nav2=Peripheral
	**Temperature/Thermostat Module** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-TMP&Nav1=Products&Nav2=Peripheral
Audio	
	**Microphone Module** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-MIC&Nav1=Products&Nav2=Peripheral
	**Speaker/Headphone Amplifier Module** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-AMP1&Nav1=Products&Nav2=Peripheral
Connectors	
	**Screw Terminal Connectors** www.digilentinc.com/Data/Products/PMOD-CON1/pmod-con1-rm.pdf
	**BNC Connectors** www.digilentinc.com/Data/Products/PMOD-CON2/pmod-con2-rm.pdf
	**RCA Audio Jack Connectors** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-CON4&Nav1=Products&Nav2=Peripheral
Motor Control/High-Drive Outputs	
	**Servo Motor Connectors** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-CON3&Nav1=Products&Nav2=Peripheral
	**H-Bridge Module for Small/Medium-Size DC Motors** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-HB3&Nav1=Products&Nav2=Peripheral
	**Open-Collector Output Module (Transistor Drivers)** www.digilentinc.com/Data/Products/PMOD-OC1/pmod-oc1-rm.pdf
	**Open-Drain Output Module (Power FETs)** www.digilentinc.com/Products/Detail.cfm?Prod=PMOD-OD1&Nav1=Products&Nav2=Peripheral

Other Useful Peripheral Module Accessories

Table 24 lists some other useful accessories when developing applications with Peripheral Modules. Some of the Peripheral Modules described in Table 23 require these additional accessories to connect to the iCEman65P board.

Table 24: **Other Useful Peripheral Module Accessories**

Picture	Description, Link to More Information
	**6Pin-Header: Six Pin Header and Gender Changer** www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Cables&Cat=Cable Useful to connect to a Peripheral Module via a 6-pin or 2x6-pin splitter cable.
	**6pinCable: Six Pin Extension Cable** www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Cables&Cat=Cable
	**2X6SPLIT: 2x6 Header to Two 1x6 Header Splitter Cable** www.digilentinc.com/Products/Catalog.cfm?Nav1=Products&Nav2=Cables&Cat=Cable

CellularRAM

The iCEman65P board includes a 128Mbit Micron MT45W8MW16 CellularRAM, connected to I/O Bank 0. The memory is organized as 8M words, each 16 bits wide. The CellularRAM interface appears in Figure 15. When used in an application, the CellularRAM uses ALL the I/O pins in I/O Bank 0. The CellularRAM is physically mounted on the back side of the board.

- **Micron MT45W8MW16BGX-708 CellularRAM**
  www.micron.com/products/ProductDetails.html?product=products/dram/psram-cellularram/MT45W8MW16BGX-701+IT
  - 8Mx16 data organization
  - 70 ns random access time
  - Burst READ and WRITE modes
    - 4, 8, 16, 32, or continuous burst
    - 80 MHz maximum clock rate
  - Page mode READ access
  - Low power consumption

Power Supplies

The CellularRAM core logic is always supplied by the 1.8V supply on the board.

The CellularRAM's I/O logic is supplied by the VCCIO_0 voltage-select block, J40.

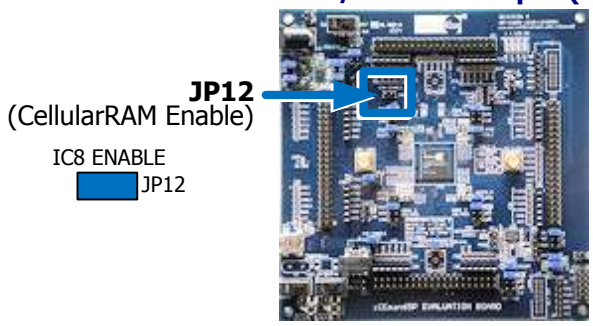
Enable/Disable Jumper (JP12)

The CellularRAM consumes all the programmable I/O (PIO) pins in I/O Bank 0. By default, the CellularRAM is enabled. To disable the CellularRAM and reclaim all the PIO pins in I/O Bank 0, simply remove jumper JP12, shown in Figure 14. When JP12 is removed, the CellularRAM's CE# chip-select pin is pulled High, disabling the memory.

Table 25: **Jumper JP12: CellularRAM Enable/Disable**

Jumper JP12	Function
Installed (DEFAULT)	When inserted, the JP12 jumper connects FPGA I/O [E10] to the CellularRAM's CE# chip-select input. The FPGA application actively drives CE# to enable the CellularRAM.
Removed	When the JP12 jumper is removed, the CellularRAM's CE# input is pulled High via a 10 kΩ resistor to VCCIO_0. This disables the CellularRAM and allows the FPGA application to use all the PIO pins in I/O Bank 0 for other purposes.

Figure 14: **CellularRAM Enable/Disable Jumper (JP12)**



Interface

Figure 15 presents the interface from the FPGA to the CellularRAM. Table 26 provides the detailed FPGA ball assignments and their shared connections to other headers on the board. Jumper JP12 must be inserted to use the CellularRAM

Figure 15: **CellularRAM Interface**

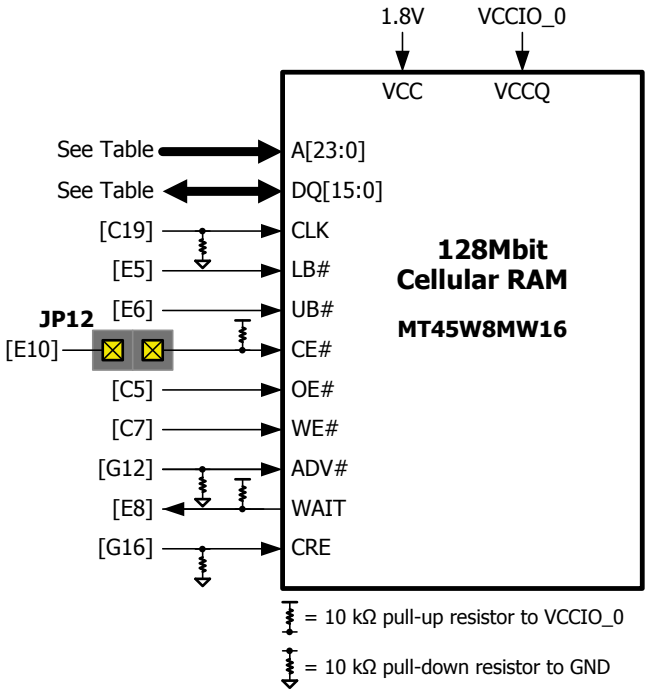


Table 26 lists the CellularRAM signals on the iCEman65P board.

Table 26: **Interface Signals to Consumer Memory Board**

Signal	FPGA Ball	Shared Header Connection	Schematic Signal	Description
A22	[E15]	J11.32	B0-IO27	Address inputs
A21	[C3]	J11.1	B0-IO00	
A20	[A18]	J11.31	B0-IO26	
A19	[E7]	J11.2	B0-IO01	
A18	[C13]	—	B0-IO40	
A17	[C6]	J11.5	B0-IO04	
A16	[H15]	J11.37	B0-IO32	
A15	[C16]	J13.4	B0-IO39	
A14	[E11]	—	B0-IO42	
A13	[C17]	J11.40	B0-IO35	
A12	[E14]	J11.26	B0-IO23	
A11	[E16]	J11.38	B0-IO33	
A10	[C18]	J11.39	B0-IO34	
A9	[G13]	J11.27	B0-IO24	
A8	[E9]	J11.18	B0-IO15	
A7	[C15]	J13.3	B0-IO38	
A6	[C14]	J13.2	B0-IO37	
A5	[G11]	J11.10	B0-IO09	
A4	[G15]	J11.21	B0-IO18	
A3	[G8]	J11.20	B0-IO17	
A2	[G14]	J11.22	B0-IO19	
A1	[G10]	J11.19	B0-IO16	
A0	[G9]	J11.8	B0-IO07	
DQ15	[A5]	J11.4	B0-IO03	Data lines, bidirectional
DQ14	[A7]	J11.7	B0-IO06	
DQ13	[A6]	J11.6	B0-IO05	
DQ12	[H9]	J11.13	B0-IO10	
DQ11	[C4]	J11.3	B0-IO02	
DQ10	[H10]	J11.16	B0-IO13	
DQ9	[C9]	J11.14	B0-IO11	
DQ8	[C11]	J11.9	B0-IO08	
DQ7	[A17]	J11.28	B0-IO25	
DQ6	[A15]	J11.33	B0-IO28	
DQ5	[A16]	J11.34	B0-IO29	
DQ4	[H14]	J13.1	B0-IO36	
DQ3	[H13]	J11.35	B0-IO30	
DQ2	[H12]	J11.36	B0-IO31	
DQ1	[H11]	J11.23	B0-IO20	
DQ0	[C10]	J11.17	B0-IO14	
CLK	[C19]	—	B0-IO41	Clock, pull-down
LB#	[E5]	J12.2	B0-PM-A2	DQ[7:0] byte enable
UB#	[E6]	J12.1	B0-PM-A1	DQ[15:8] byte enable
CE#	[E10]	J14	B0-CLKSMA/CE	Chip-enable, controlled by JP12, pull-up
OE#	[C5]	J12.3	B0-PM-A3	Active-Low output enable
WE#	[C7]	J12.4	B0-PM-A4	Active-Low write enable
ADV#	[G12]	J11.25	B0-IO22	Address Valid, pull-down
WAIT	[E8]	J11.15	B0-IO12	Wait, pull-up
CRE	[G16]	J11.24	B0-IO21	Control Register Enable, pull-down

Pull-up = 10 kΩ pull-up resistor to VCCIO_0 supply. **Pull-down** = 10 kΩ pull-down resistor to ground

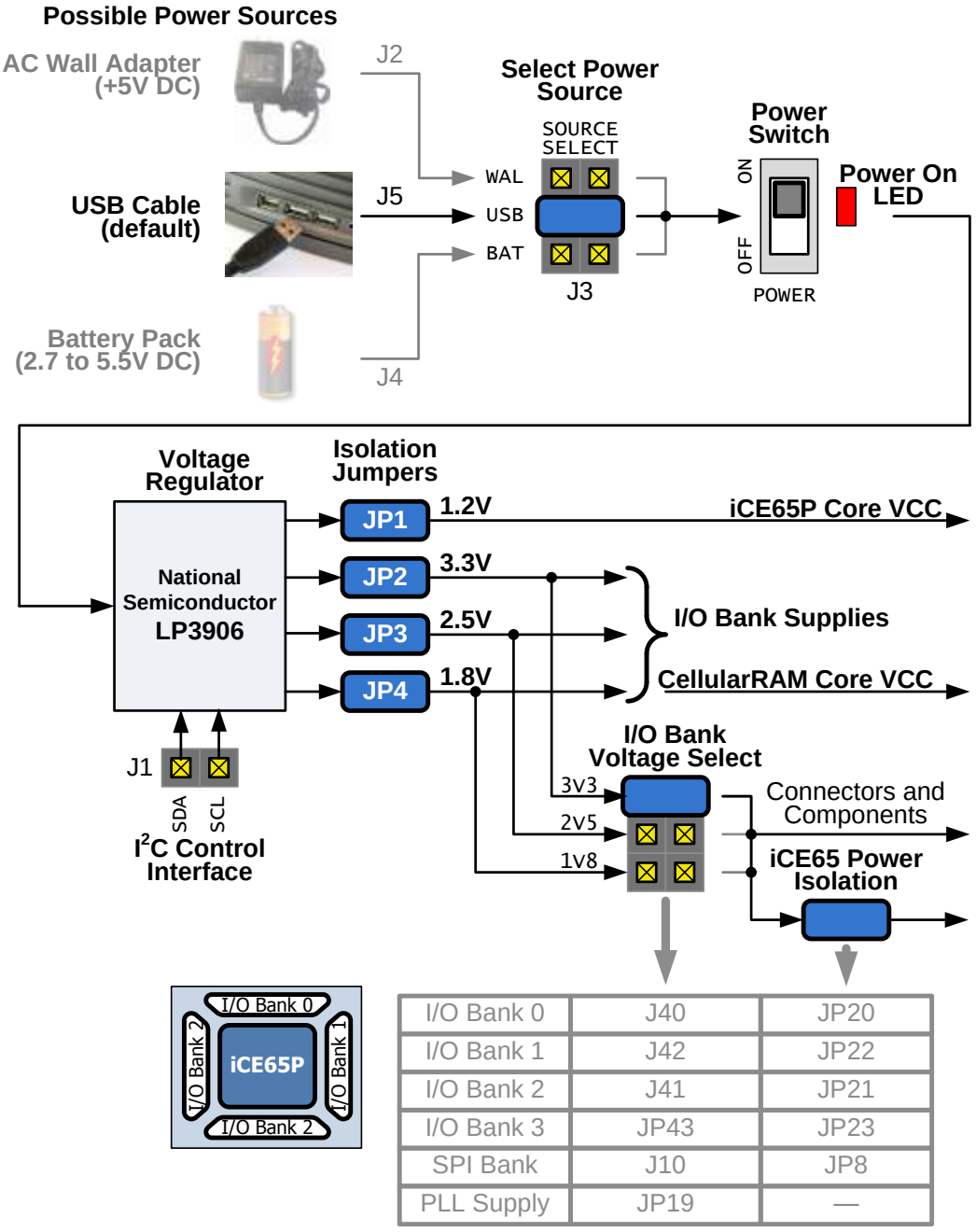
Power Supply Design Overview

Figure 16 depicts the power supply design for the iCEman65P board. There are three possible Board Power Sources, although generally the board is powered from the USB cable connected to a USB port on a PC or powered USB hub.

The J3 jumper selects between the three possible power sources, as described in Table 27. The select power source is then controlled by the power switch, SW1. If the board is connected to a power supply, then the red LED next to the switch lights up when the switch is turned ON.

When the power switch is ON, the selected power source then drives a National Semiconductor LP3906 four-output regulator. The regulator provides 1.2V for the iCE65P's core voltage and 3.3V, 2.5V, and 1.8V to the I/O Bank Supply and Phase-Locked Loop (PLL) Supply Voltage Controls.

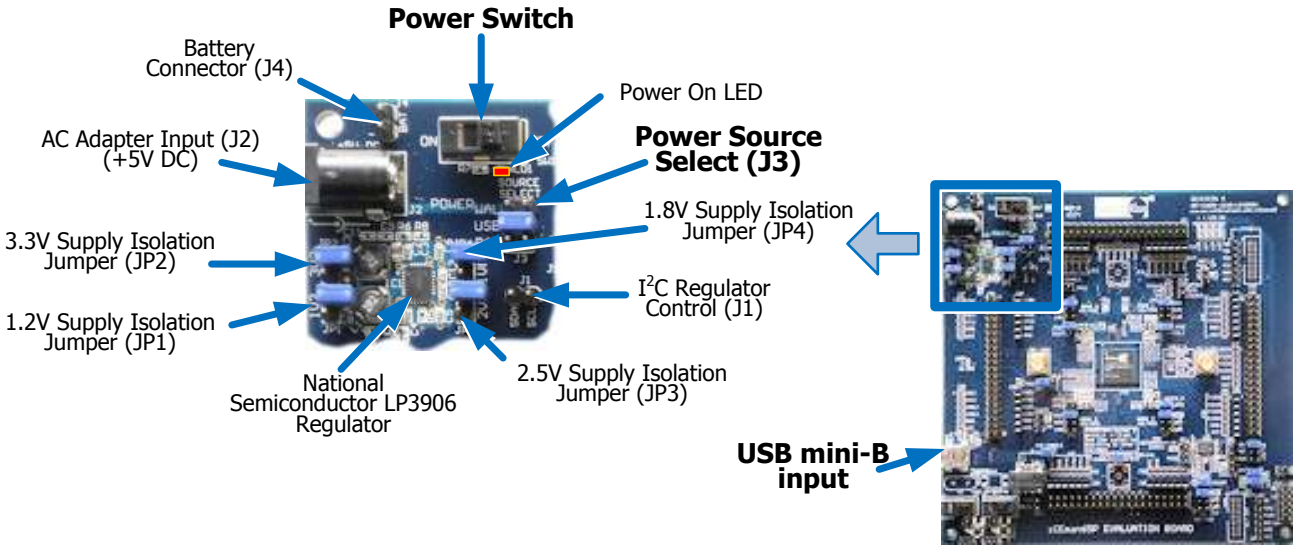
Figure 16: **iCEman65P Board Power Supply Overview**



I/O Bank 0	J40	JP20
I/O Bank 1	J42	JP22
I/O Bank 2	J41	JP21
I/O Bank 3	JP43	JP23
SPI Bank	J10	JP8
PLL Supply	JP19	—

The LP3906 regulator also includes an I^2C control interface. Consequently, an external controller can adjust the regulator voltage outputs. Any adjustments are only active while power is supplied to the board. When the power supply is removed, the regulator returns to the default output voltage levels. Consult the LP3906 data sheet for additional information.

Figure 17: **iCEman65P Board Power Supply Jumpers**



Board Power Sources

By default, the iCE65P board operates directly from the power supplied from a USB port. Just connect the included USB cable between the mini-B connector on the board and a powered port on your computer or USB hub.

However, the board physically supports three possible power sources, offering additional flexibility.

1. USB 2.0 Connector
2. +5V DC Wall Power Adapter
3. External Battery Pack

Select the desired power source using jumper J3, located in the upper left corner of the board, near the power switch and LED.

The selected power source is controlled by the SW1 power switch. The LD1 LED lights when power is applied to the board.

Table 27: **Power Input Sources, Jumper J3 Settings**

Power Source	Jumper J3 Setting	Cabling Requirements
+5V DC from AC Wall Adapter	SOURCE SELECT WAL ■ USB ⊠ ⊠ BAT ⊠ ⊠ J3	Requires a +5V DC adapter (not included), connected to the barrel plug (J2).
USB Connector (DEFAULT)	SOURCE SELECT WAL ⊠ ⊠ USB ■ BAT ⊠ ⊠ J3	Connect the included mini-USB cable to a powered USB port on a computer or to a powered USB hub.
External Battery Pack	SOURCE SELECT WAL ⊠ ⊠ USB ⊠ ⊠ BAT ■ J3	Connect a battery pack (not included) to jumper header J4.

USB 2.0 Connector

The USB 2.0 cable supplied with the kit typically supplies power to the iCE65P board. The total power to the board may be limited by the USB host controller to approximately 2.5 W (5V @ 500 mA), which is more than sufficient for most stand-alone iCE65P applications. If you add you multiple add-on boards or modules, then the +5V DC Wall Power Adapter may prove a better power option.

To power the board from the USB connector, attach a cable between a host with a powered USB port and the board's mini-USB connector. Also, set jumper J3 to the "USB" setting, as shown in Table 27.

+5V DC Wall Power Adapter

For additional power capacity, connect the iCE65P board directly to AC wall power using a +5V DC wall adapter. Set jumper J3 to the "WAL" setting, as shown in Table 27.

The +5V DC input is the best choice for applications that use any of the Hirose FX2 connectors, the 40-pin ribbon cable connectors, or the Samtec connector because the attached peripheral boards may require additional power.

An AC adapter is not included with the iCEman65P kit. However, one is available for purchase as listed in Table 28. The switching power supply directly supports North American, Japanese, and Taiwanese AC outlets. The optional adapter kit is available for European countries and the United Kingdom.

Table 28: **AC Wall Power Adapters**

Picture	Description, Link to More Information
	**5VDC Switching Power Supply** www.digilentinc.com/Products/Catalog.cfm?NavPath=2,393&Cat=3
	**European/UK Wall Plug Adapter** www.digilentinc.com/Products/Catalog.cfm?NavPath=2,393&Cat=3

External Battery Pack

The iCE65P board is optionally powered by a battery pack. Connect the batter pack to the plated-through holes associated with the J4 connector, located in the upper left corner of the board.

A single Li-ion cell has a nominal voltage of 3.6V and can be connected directly to the J4 header. However, there is no recharging mechanism provided on the board.

If using NiCd, NiMH, or alkaline batteries, use a pack with three or four cells connected in series, which provides a nominal voltage of 3.6V or 4.8V.

If using a battery pack, set jumper J3 to the "BAT" setting, as shown in Table 27.

I/O Bank Supply and Phase-Locked Loop (PLL) Supply Voltage Controls

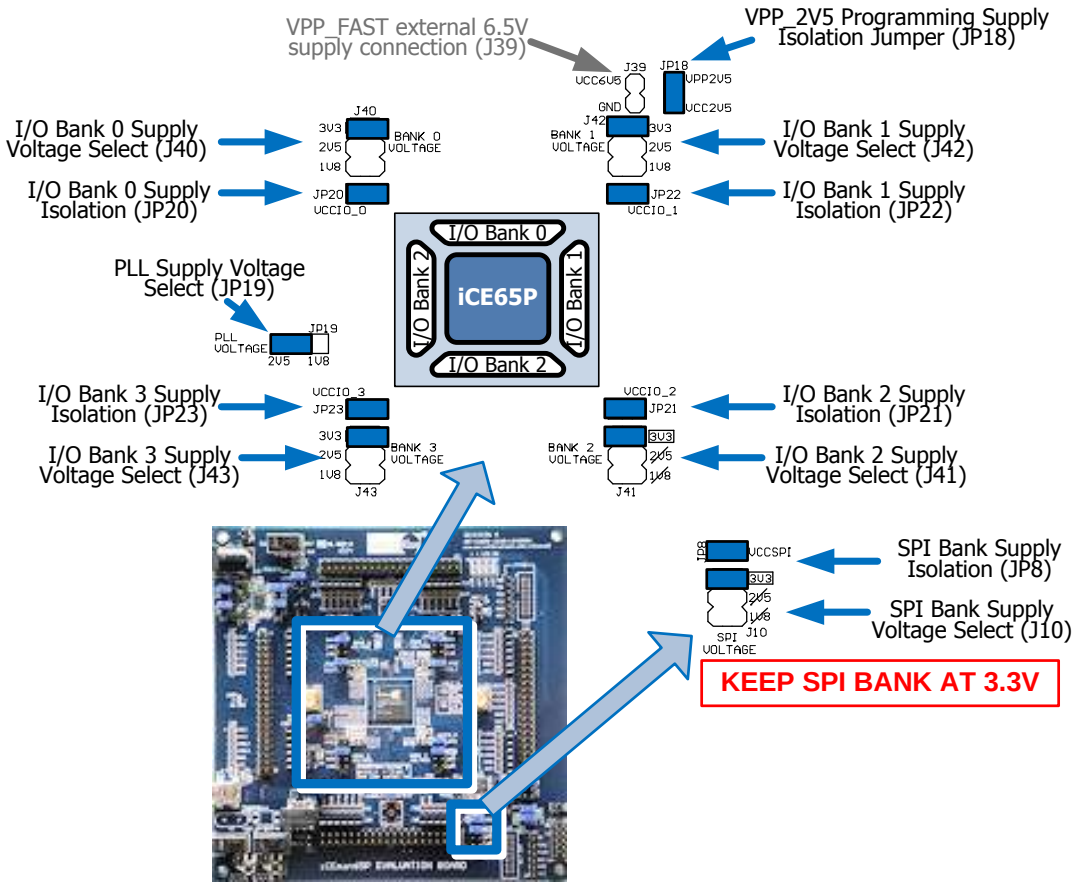
As shown in Table 29, each of the four iCE65P I/O banks, the SPI configuration interface bank, and the phase-locked loop (PLL) supports a range of I/O standards and voltages.

Table 29: **I/O Bank Voltage Settings**

I/O Bank/Feature	FPGA Supply	Controlling Jumper Header	Available Options
I/O Bank 0 (top)	VCCIO_0	J40	3.3V, 2.5V, 1.8V
I/O Bank 1 (right)	VCCIO_1	J42	3.3V, 2.5V, 1.8V
I/O Bank 2 (bottom)	VCCIO_2	J41	Normally set to 3.3V
I/O Bank 3 (left)	VCCIO_3	J43	3.3V, 2.5V, 1.8V
SPI	SPI_VCC	J10	Normally set to 3.3V
PLL	PLL_VCC	JP19	2.5V, 1.8V

Figure 18 indicates the location and default setting for each of the voltage select jumpers.

Figure 18: **I/O Bank and SPI Bank Voltage Jumpers**



Power Measurement/Voltage Isolation

Each voltage input to the iCE65P device has an isolation jumper. This jumper provides two possible functions.

1. Remove a specific jumper to isolate the supply rail and provide power from an external source.
2. Remove a specific jumper to measure the current flowing to the specific voltage rail.

Voltage Rail	Nominal Voltage	Upstream Voltage Source	Isolation Jumper	Reference Figure
Primary input supply	5.0V	Selectable, controlled by jumper J3	J3	Figure 17
VCC1V2: iCE65P core voltage	1.2V	LP3906 output SW1	JP1	Figure 17
VCC3V3: 3.3V supply	3.3V	LP3906 output SW2	JP2	Figure 17
VCC2V5: 2.5V supply	2.5V	LP3906 output LDO1	JP3	Figure 17
VCC1V8: 1.8V supply, CellularRAM core supply	1.8V	LP3906 output LDO2	JP3	Figure 17
VCCIO_0: FPGA I/O Bank 0 supply, CellularRAM I/O supply	Selectable	Controlled by jumper J40	JP20	Figure 18
VCCIO_1: FPGA I/O Bank 1 supply	Selectable	Controlled by jumper J42	JP22	Figure 18
VCCIO_2: FPGA I/O Bank 2 supply	3.3V (Selectable)	Controlled by jumper J41	JP21	Figure 18
VCCIO_3: FPGA I/O Bank 3 supply	Selectable	Controlled by jumper J43	JP23	Figure 18
VCC_PLL: FPGA Phase-Locked Loop (PLL) supply	2.5V (Selectable)	Controlled by jumper JP23	N/A	Figure 18
VCCSPI: SPI Bank supply	3.3V (Selectable)	Controlled by jumper J10	JP8	Figure 18
VPP2V5: NVCM programming voltage	2.5V	LP3906 output LDO1	JP19	Figure 18
VPP6V5: Fast NVCM programming voltage	6.5V	External voltage source	J39	Figure 18

SPI Configuration Interface

The iCEman65P board uses a 'V'-series part, meaning that the device does not physically have internal programmable Nonvolatile Configuration Memory (NVCM). The iCE65L04 device on the board optionally configures itself from an attached SPI Flash PROM or is downloaded like a processor peripheral using an SPI-like interface.

Figure 19 shows the various options available on the SPI interface.

SPI Serial Flash

All iCEman65P boards have a 25-series SPI serial Flash PROM to hold one or more iCE65P configuration images. Revision A and B boards also include a 45-series SPI serial Flash PROM for additional compatibility testing. By default, however, all instructions use the 25-series SPI Flash PROM.

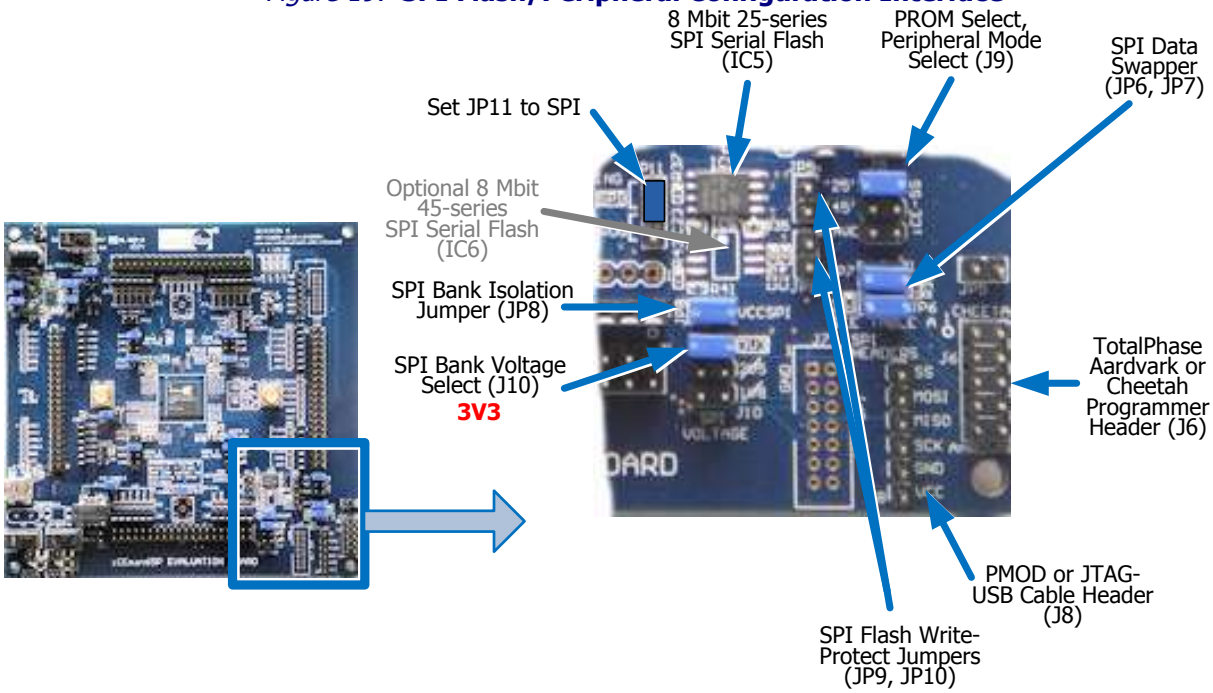
Default Options

As pictured in Figure 19, the following are the default jumper settings required to program and configure from the 25-series SPI serial Flash PROM.

- The USB programmer must target the SPI serial Flash. Set jumper JP11 to the "SPI" setting.
- The 25-series SPI serial Flash PROM is the default memory. Set jumper J9 to the "25" setting.
- The 25-series SPI serial Flash PROM operates from a 3.3V supply. Install the SPI bank isolation jumper (JP8) and set the SPI bank voltage to 3.3V by setting jumper J10 to "3V3."
- To program the 25-serial PROM, ensure that the associated write-protect jumper, JP9, is removed.
- Set the SPI data swapper jumpers, JP6 and JP7, to the settings shown in Figure 19.

Selecting a Configuration PROM

Figure 19: **SPI Flash/Peripheral Configuration Interface**



Supply Voltage

Although the SPI interface can operate at different voltages, set jumper J10 to 3.3V. The SPI serial PROM mounted on the board is a 3.3V device.

SPI Serial Flash

Each SPI serial PROM location has two associated jumpers, pictured in Figure 19.

Enable Jumpers

Header block J9 controls which SPI PROM, if any, is enabled, as described in Table 30. The selection controls the location of the iCE65P configuration image. Only one jumper is allowed.

Table 30: **Jumper J9 Settings: Configuration Source Select**

J9 Jumper Setting	Function
'25'	When inserted, the 8Mbit M25P80 25-series SPI serial PROM is the configuration source for the iCE65P component.
'45'	This setting is only useful if an AT45DB081D or similar PROM is mounted in location IC5. If mounted on the board, the 45-series SPI serial PROM is the configuration source for the iCE65P component.
SLAVE	If inserted, then the iCE65P component is configured by an external processor or controller using an SPI-like serial interface.

Write-Protect Jumpers

Both SPI PROMs have an associated write-project jumper, as described in Table 31. Installing the associated jumper prevents the PROM from being erased, programmed, or overwritten. The jumper must be removed to program the associated PROM.

Table 31: **SPI PROM Write-Protect Jumpers**

Jumper	Function
JP9	Normally empty. When inserted, protects the 8Mbit M25P80 25-series SPI serial PROM against any erase, programming, or write operations. This jumper must be removed in order to program the PROM.
JP10	Normally inserted. When inserted, protects the 45-series SPI serial PROM, if mounted in location IC5, against any erase, programming, or write operations. This jumper must be removed in order to program the PROM.

SPI Flash Programming

The iCEman65P board supports four different programming options, as listed in Table 32. The iCEman65P does not include an on-board programmer. Various solutions provide select or generic SPI Flash programming, the ability to configure the iCE65 mobileFPGA directly via SPI, or the ability to program the iCE65 mobileFPGA's internal Nonvolatile Configuration Memory (NVCM).

Table 32: **iCEman65P Programming/Cofiguration Solutions**

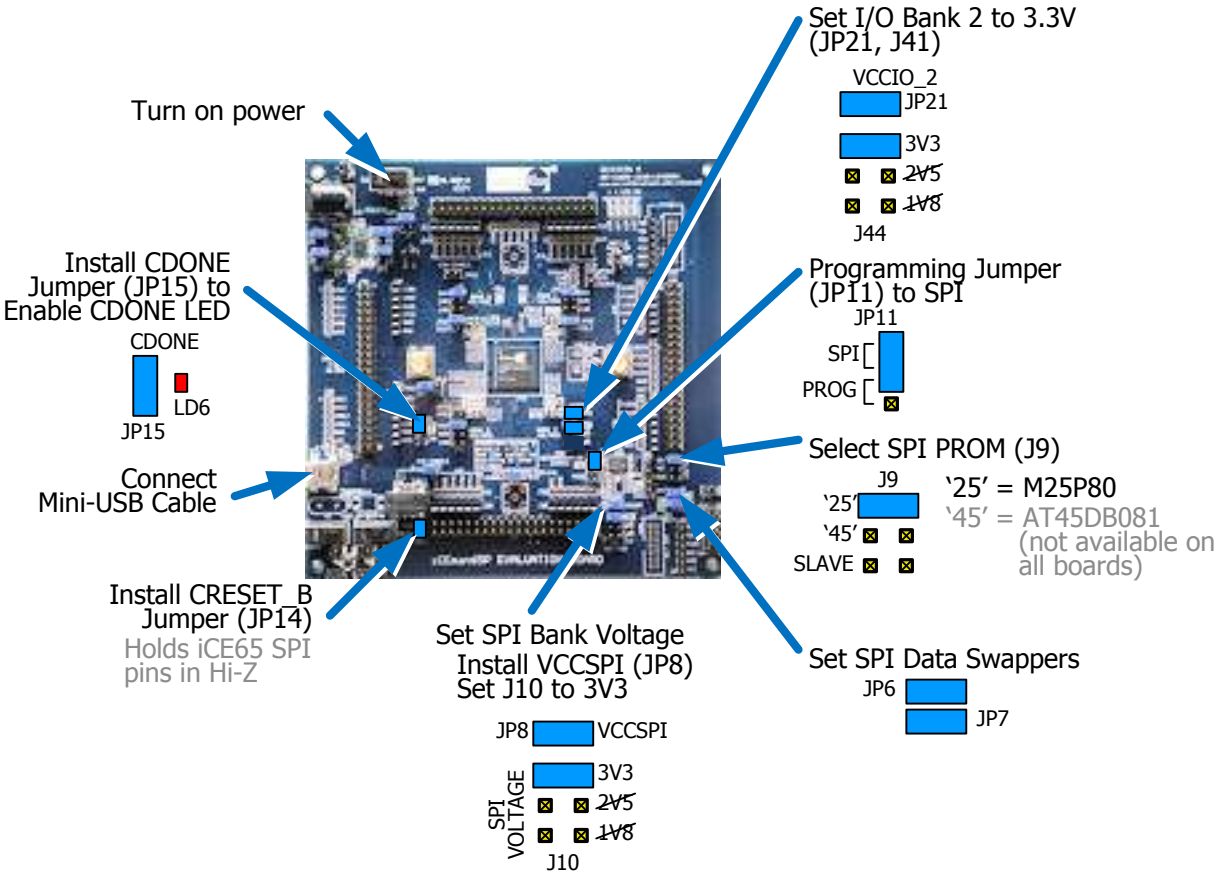
Programming Option	Programming Software	SPI Flash	iCE65 Direct via SPI	iCE65 NVCM
SiliconBlue iCEcable	iCEchip SiliconBlue Programmer	ST Micro/Numonyx M25P80 M25P16 M25P32 M25P20	Yes	Yes
DediProg SF100 Flash Programmer	Included	Generic, multiple SPI Flash vendors and densities	Yes	No
TotalPhase Cheetah/Aardvark Programmer	FLASH Center	Generic, multiple SPI Flash and I^2C vendors and densities	No	No
Digilent USB-JTAG Programmer	Adept/iCEutil	ST Micro/Numonyx M25P80 M25P16	No	No

Board Setup/Jumper Settings

To program the SPI Flash, configure the iCEman65P board as shown in Figure 20.

- Connect power to the to the board but leave the power switch turned off.
- Insert a jumper on JP14 to force the iCE65P CRESET_B pin Low. This holds the iCE65P SPI interface in high-impedance (Hi-Z), allowing the USB controller or external programmer full access to the SPI Flash PROM.
- Ensure that the SPI bank is set for 3.3V operation. Install jumper JP8 and set jumper J10 to 3V3.
- Set the SPI data swapper, JP6 and JP7, as shown in Figure 20 and also shown in Table A on the board. The jumpers must be in the horizontal setting.
- Ensure that I/O Bank 2 is set to 3.3V. Install jumper JP21 and set jumper J44 to 3V3.
- Ensure that the CDONE LED is enabled. Install jumper JP15.
- Ensure that the jumper JP11 is set to SPI.
- Turn on the board power switch.

Figure 20: **SPI Flash Programming Jumper Settings**



Post-Programming Operations

After successfully programming the SPI Flash PROM, simply remove the CRESET_B jumper (JP13). This releases the iCE65P device from reset. The iCE65P part will automatically load from the programmed SPI Flash PROM and the CDONE LED lights indicating successful configuration.

TotalPhase Cheetah/Aardvark Programmer

The iCEman65P board supports two different USB-based SPI memory programmers from TotalPhase, Inc (www.totalphase.com). Both programmers support a variety of industry-standard SPI serial PROMs. These programmers are NOT included with the iCEman65P evaluation kit. They are third-party products sold and supported by TotalPhase, Inc.

- **Cheetah SPI Host Adapter**
  www.totalphase.com/products/cheetah_spi/
- **Aardvark I2C/SPI Host Adapter**
  www.totalphase.com/products/aardvark_i2cspi/

Software Requirements

The TotalPhase SPI programmers come complete with an installation CD-ROM and provide drivers and software for both the Windows and Linux OS environments.

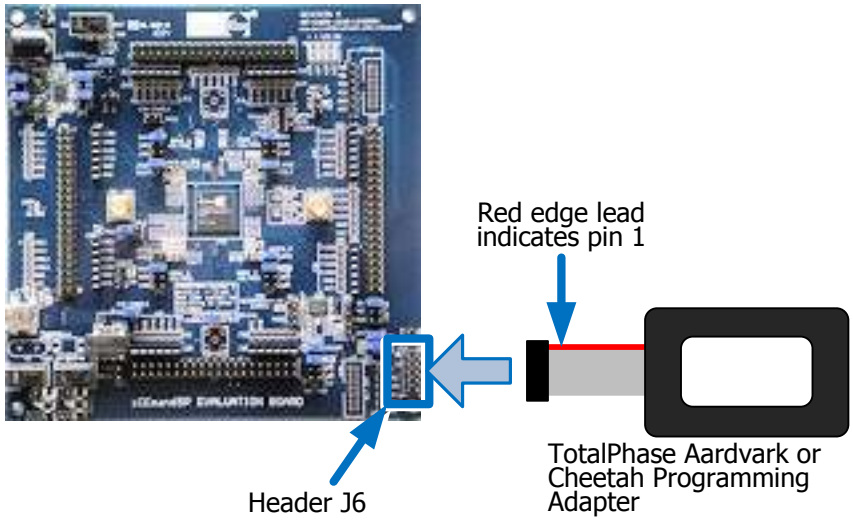
- **Aardvark Control Center**
  www.totalphase.com/products/control_center/
- **Cheetah GUI Software**
  www.totalphase.com/products/cheetah_gui/
- **TotalPhase Flash Center Software**
  www.totalphase.com/products/flash_center/

Board Setup/Jumper Settings

The board setup when using the TotalPhase programmers appears in Figure 20.

Plug the Aardvark or Cheetah programmer header onto the J6 header, located in the lower right corner of the board, as shown in Figure 21. The header on the iCEman65P board is not keyed. The red-colored line on the adapter cable is pin 1, and should be at the top, as shown in the figure. Plug the Aardvark or Cheetah adapter into the USB port on your computer.

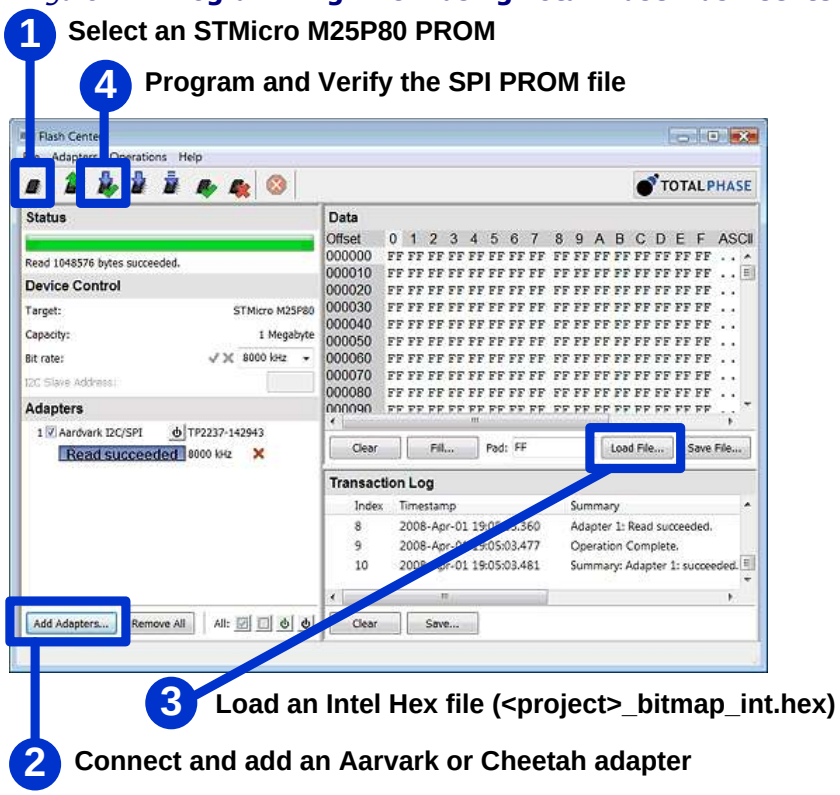
Figure 21: **TotalPhase Aardvark or Cheetah Adapter Plugs into Header J6**



Programming the PROM Using Flash Center

As shown in Figure 22, programming the STMicro SPI serial Flash PROM on the iCEman65P board is a relatively simple four-step process.

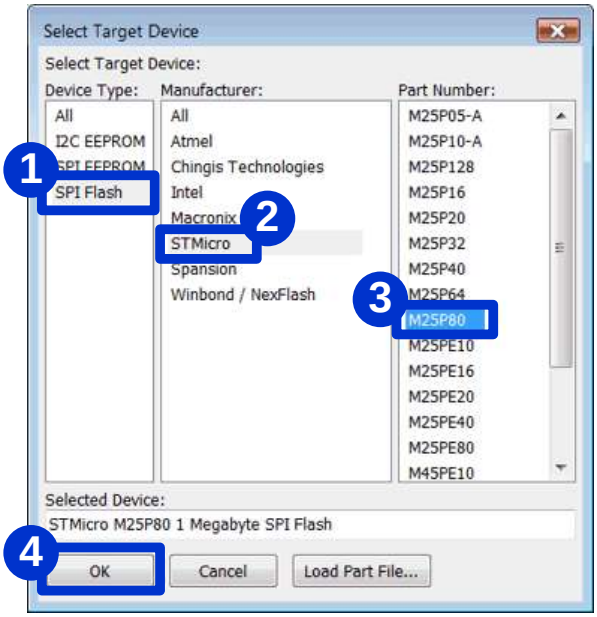
Figure 22: **Programming PROM using TotalPhase Flash Center**



After invoking the Flash Center software …

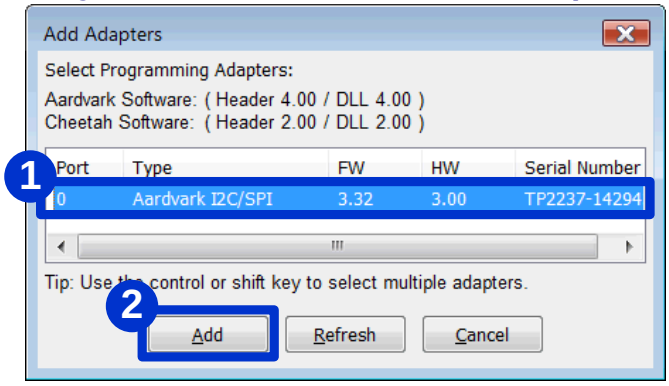
1. **Select the STMicro M25P80 SPI serial Flash PROM.** Click the Select Target icon in the toolbar. Then select the STMicro M25P80 SPI serial Flash PROM, as shown in Figure 23. Depending on your version of Flash Center, this device may be listed under the manufacturer name Numonyx, which is the joint venture between the Intel and STMicro Flash memory divisions.

Figure 23: **Select STMicro M25P80 SPI Serial Flash PROM**



2. **Add a TotalPhase Aardvark or Cheetah adapter.** Connect the USB-based TotalPhase Aardvark or Cheetah programmers to your computer. Click **Add Adapters**, as shown in Figure 22. Select and add the adapter, as shown in Figure 24.

Figure 24: **Add Aarvark or Cheetah Adapter**



3. **Load the Intel Hex version of the iCE65P configuration bitmap.** By default, the Intel Hex file will be named `<project>_int_bitmap.hex`. The SiliconBlue iCECUBE development system generates the bitmap files in the `../<project_name>_Impl/sbt/outputs/bitmap` sub-directory, where <project_name> is the iCEcube project name.

   Click **Load File** as shown in Figure 22. The contents of the selected file appear in the Data buffer display.

4. Program and Verify the SPI PROM file, as shown in Figure 22. The Flash Center software erases the PROM sectors as required, programs the contents loaded in the Data buffer, and then verifies the contents.

Remove CRESET_B Jumper (JP14)

After programming the SPI serial Flash PROM, remove jumper JP14 and store it on the board, typically on jumper JP10. Jumper JP10 is the write-project for the 45-series SPI PROM.

After jumper JP14 is removed, the iCE65P device loads the new configuration data from the SPI PROM. The CDONE LED, LD6 shown in Figure 3, lights up indicating that the iCE65P device is configured correctly.

Digilent USB-JTAG Programmer

The iCEman65P board also supports the Digilent JTAG-USB cable using the ICEUTIL programming utility. The JTAG-USB cable potentially provides a possible low-cost programming solution for stand-alone iCE65P applications.

- **Digilent JTAG-USB Cable**
  www.digilentinc.com/Products/Detail.cfm?Prod=JTAG-USB&Nav1=Products&Nav2=Cables

Software Requirements

The on-board USB programmer requires the following Windows/DOS-based programming software. Refer to the ***Adept Programming Software and ICEUTIL.EXE Installation Guide*** for installation instructions.

- **Adept USB Programming Software**
  www.siliconbluetech.com/iCEman65/downloads/Adept.msi
  This software installs the various device drivers required for the on-board USB programmer.
- **ICEUTIL.EXE Command-Line Utility**
  www.siliconbluetech.com/iCEman65/downloads/iceutil.exe
  After installing the Adept USB software, use this command-line utility to program the SPI Flash PROM on the iCEman65P board.
- **Adept Programming Software and ICEUTIL.EXE Installation Guide**
  www.siliconbluetech.com/iCEman65/AdeptICEUTILInstallation.pdf

Plug the cable directly into SPI header J8, located in the bottom-right corner of the board. Table 33 illustrates how the JTAG-USB cable connects to the J8 header.

Table 33: **SPI Header J8 Supports Digilent JTAG-USB Cable**

SPI Header J8	JTAG-USB Cable	Function
SS	TMS	SPI PROM slave select.
MOSI	TDI	SPI Master Output, Slave Input
MISO	TDO	SPI Master Input, Slave Output
SCK	TCK	SPI clock
GND	GND	Ground
VCC	VDD	Voltage controlled by jumpers JP8 and J10, shown in Figure 18.

The only difference when using the ICEUTIL programming utility is the target device name (`-d <device_name>`). The device name for the iCEman65P USB programmer is `iCEman65`. However, the JTAG-USB cable has a different device name. Use the Adept USB Administrator software to determine the name of the cable. For example, if USB Administrator reports the name as "DCabUSB", then use this value as the device name with the ICEUTIL utility as "`-d DCabUsb`".

The board setup and programming is similar to using the iCEman65P **Error! Reference source not found.**.

Measuring Power

The iCEman65P board is specifically designed to easily measure power on the iCE65P device.

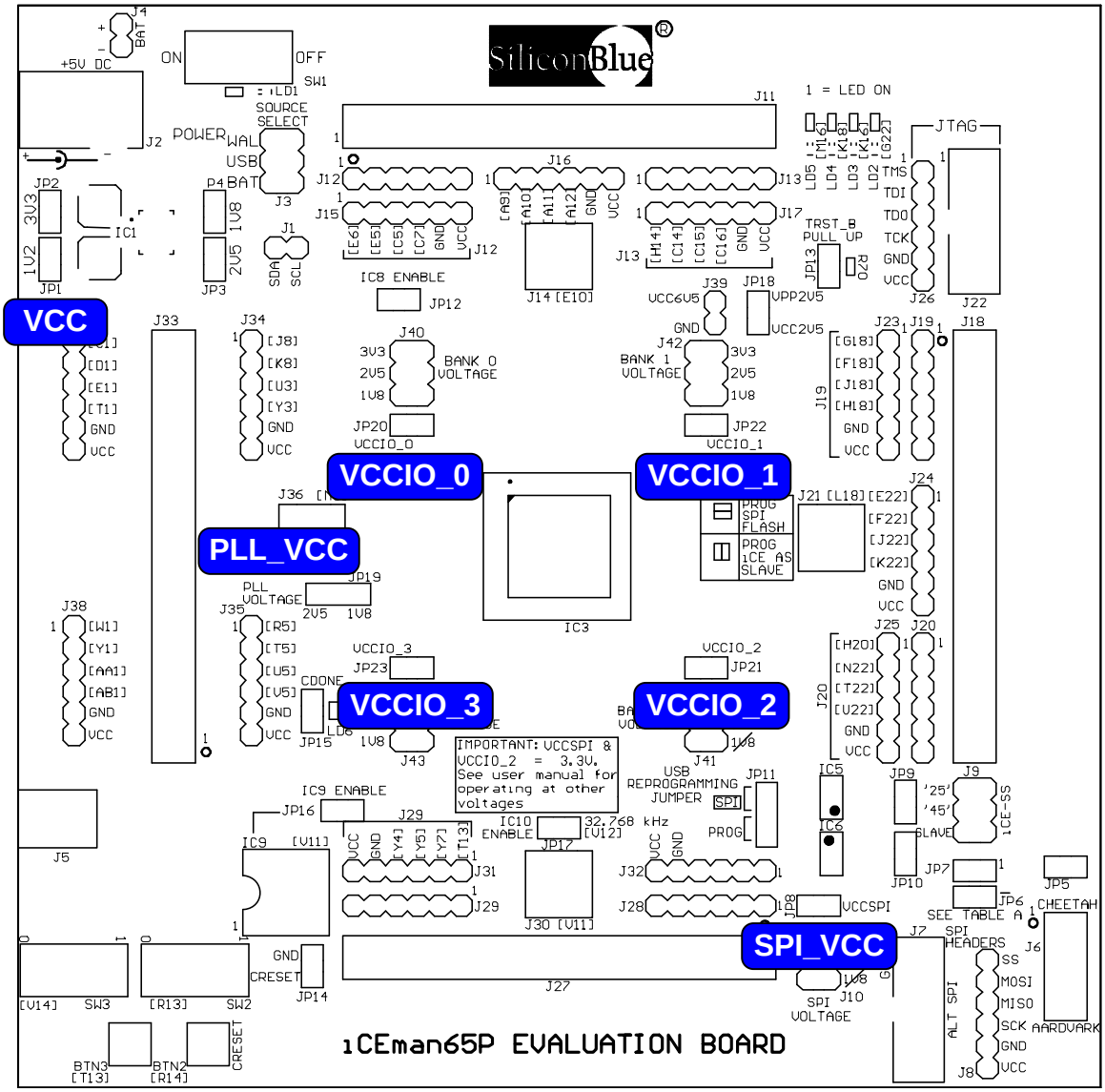
Test Access Points

Each iCE65P voltage rail has a two-pin header access point, as listed in Table 34 and indicated in Figure 25.

Table 34: **iCE65P Power Measurement Test Points**

Voltage Input	iCE65P Power Rail	Jumper Test Point
VCC	iCE65P Core Logic	JP1
VCCIO_0	I/O Bank 0 (Top)	JP20
VCCIO_1	I/O Bank 1 (Top)	JP22
VCCIO_2	I/O Bank 2 (Bottom)	JP21
VCCIO_3	I/O Bank 3 (Left)	JP23
SPI_VCC	SPI Bank	JP8
PLL_VCC	PLL	JP19

Figure 25: **iCE65P Power Measurement Jumper Access Points**



Power Testing Methods

There are a variety of methods to measure power on the iCEman65P board as described below.

Easy Method using a Multimeter

The iCEman65P evaluation kit includes a small, red and black, two-pin MTE connector, shown in Figure 26. The cable provides an easy connection between the iCEman65P board and your high-accuracy multimeter. Use a meter with a minimum of 10,000 counts; 50,000 counts or more is recommended for better accuracy.

Figure 26: **Included Power Test Cable**

To take a quick measurement, follow these steps.

1. Turn off power to the iCEman65P board.
2. Remove the jumper associated with the voltage rail to be measured. Refer to Table 34 and Figure 25 to locate the correct jumper.
3. Insert the power test cable shown in Figure 26 over the empty jumper location.

4. Connect the available power cable leads to your multimeter using the multimeter's alligator or test clips.
5. Configure the multimeter to measure current using its highest mA or Amp range. This setting typically has the lowest voltage drop internally within the meter.
6. Reapply power to the iCEman65P board and configure the iCE65P device if necessary.
7. Observe the power reading on the multimeter. At low clock rates, which result in lower iCE65P power, switch the meter to a lower amperage setting for better accuracy reading the low current levels. However, this also may increase the resistance across the meter leads. Using too low of a meter setting causes a large voltage drop within the meter, violating the minimum input voltage specification to the iCE65P device.
8. The value measured by the multimeter is a current. Convert the measurement to power using Equation 1. The voltage is the operating voltage, the voltage across the jumper. This value can be accurately measured with a second multimeter to show the voltage drop across the first. However, just measuring the initial voltage, before taking any current readings, usually provides acceptable accuracy and the voltage drop across the meter is generally small.

Equation 1

$$\text{Power} = \text{Current} \times \text{Voltage}$$

Although this method is easy, here are a few caveats and pointers.

- **Always start at the highest current setting for your meter. Using too small a setting may damage your meter!** After determining the maximum current range for your measurement, then you can safely use the appropriate lower current setting.
- The voltage drop across the meter leads may violate the minimum supply voltage specification for the iCE65P device. To determine the voltage drop, use a second multimeter to measure either the voltage across the first meter's leads during a test or the resistance between the first meter's leads.
- Using the highest current measurement setting typically results in the lowest voltage drop.

Using High-Precision, Small-Value Resistors

For more-accurate, time-sensitive measurements, place a low-value resistor across the jumper test point. According to Ohm's Law, the current passing through the resistor produces a voltage drop. Measure the voltage differential across the resistor during expected operation. Convert the measurement to power using Equation 2. The voltage is the measured voltage across the resistor; the resistance is the value of the resistor.

Equation 2

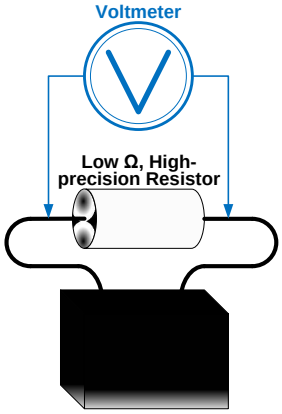
$$\text{Power} = \frac{(\text{Voltage})^2}{\text{Resistance}}$$

The following are a few guidelines on selecting a resistor.

- Use a high-precision resistor.
- The resistor must handle the power dissipated under the anticipated test conditions.
- Too small a resistor value may result in too small a voltage difference across the resistor to measure with your test equipment.
- Too large a resistor value may result in too large of a voltage difference across the resistor. Too large a voltage drop might violate the minimum voltage specifications for the iCE65P device.

Figure 27 shows an example header block designed to fit over one of the jump locations. Measure the voltage drop across the low-value resistor, either with a voltmeter or with data acquisition equipment.

Figure 27: **Resistor Header Block**



This method is recommended for taking power measurements over time.

Quick Board Test

The following procedure provides a quick and simple board test. This is the same design that is pre-programmed on the board when it is shipped from the factory and described in the ***Getting Started*** booklet included with the board.

Set Jumpers

Start by setting the jumpers to their default locations shown in Figure 29.

Install Oscillator

Install the 27.0 MHz oscillator in location IC8, as described in "Installing an Oscillator" on page 6. The precise oscillator frequency does not matter, although the oscillator should be in the 5 to 40 MHz range for this simple test.

Insert PMOD-LED Module

The board ships with a small, 6-pin LED peripheral module. Connect this module to the top-edge, left-most PMOD socket, J12 (see Figure 13 on page 15). Note the location of the power and ground connections. The LEDs on the module face toward the SiliconBlue logo. Even if the module is installed backwards, no damage occurs.

Program SPI Flash

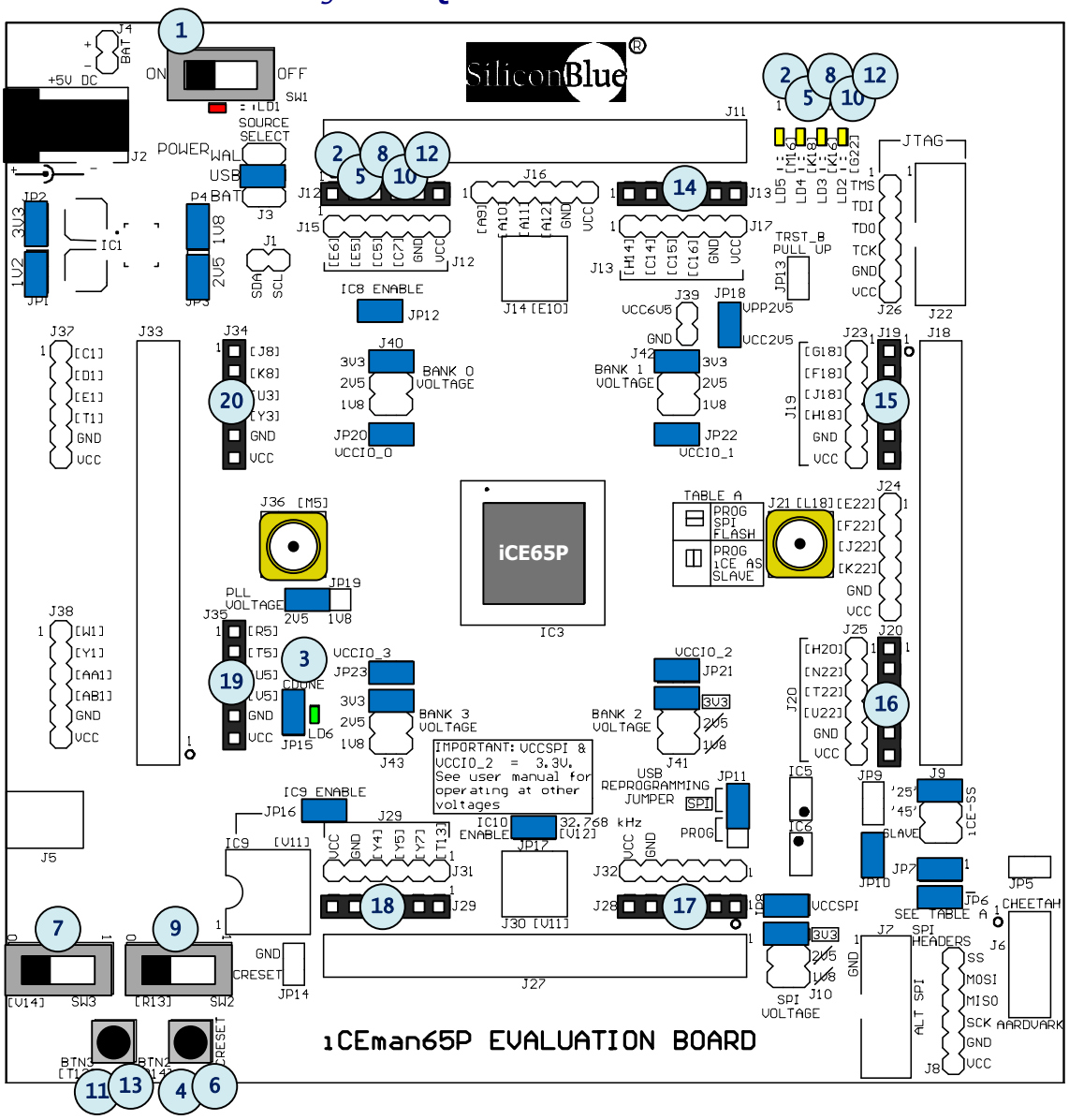
Program the SPI serial PROM with the following configuration image.

When programming is complete, remove the jumper on JP14, which holds the iCE65P CRESET_B pin Low during programming.

Test Procedure and Observations

To test the board, perform the following steps and observations. See Figure 28 for the associated test reference points.

Figure 28: **Quick Test Reference Points**



0. Start the test with no power applied to the board; power switch SW1 is turned off.
1. Apply power to the board by switching SW1 to the ON position. The adjacent LED, LD1, should light.
2. Observe that the LEDs on the board and on the LED peripheral module blink in a directional pattern.
3. Check that the CDONE LED, LD2, is lit.
4. Press and hold pushbutton BTN2, which asserts the iCE65P's CRESET_B signal.
5. Observe that the LEDs are static because the iCE65P is held in the reset state. The LEDs on the peripheral module are lit, pulled High by the iCE65P's internal pull-up resistors. The yellow LEDs on the board may be off or dimly lit.
6. Release BTN2. The LEDs again blink.
7. Change slide switch SW3. Left or right does not matter.
8. Observe that the LEDs change direction.
9. Change slide switch SW2. Left or right does not matter.
10. Observe that the LEDs change direction.
11. Press and hold BTN3.

12. Observe that the green LEDs are static and fully lit. The peripheral module LEDs are static and not lit.
13. Release BTN3 and the LEDs again blink.
14. Remove the LED peripheral module and connect it to the top-edge, right-most header, J13. The LEDs face toward the iCE65P component. The LEDs toggle as before. The top-edge and right-edge PMOD connectors in this test design are controlled by the 32.768 kHz oscillator on the back of the board.
15. Remove the LED peripheral module and connect it to the right-edge, top-most header, J19. The LEDs face toward the iCE65P component. The LEDs toggle as before.
16. Remove the LED peripheral module and connect it to the right-edge, bottom-most header, J20. The LEDs face toward the iCE65P component. The LEDs toggle as before, except that top-most LED remains lit. This is because there is no pin driving this LED and the LED is pulled High via a pull-up resistor on the module.
17. Remove the LED peripheral module and connect it to the bottom-edge, right-most header, J28. The LEDs face toward the iCE65P component. The LEDs toggle as before. The bottom-edge and left-edge PMOD connectors in this test design are controlled by the 32.0 MHz oscillator mounted in socket IC9.
18. Remove the LED peripheral module and connect it to the bottom-edge, left-most header, J29. The LEDs face toward the iCE65P component. The LEDs toggle as before.
19. Remove the LED peripheral module and connect it to the left-edge, bottom-most header, J35. The LEDs face ***away*** the iCE65P component. The LEDs toggle as before.
20. Remove the LED peripheral module and connect it to the left-edge, top-most header, J34. The LEDs face ***away*** the iCE65P component. The LEDs toggle as before.

Functions Tested

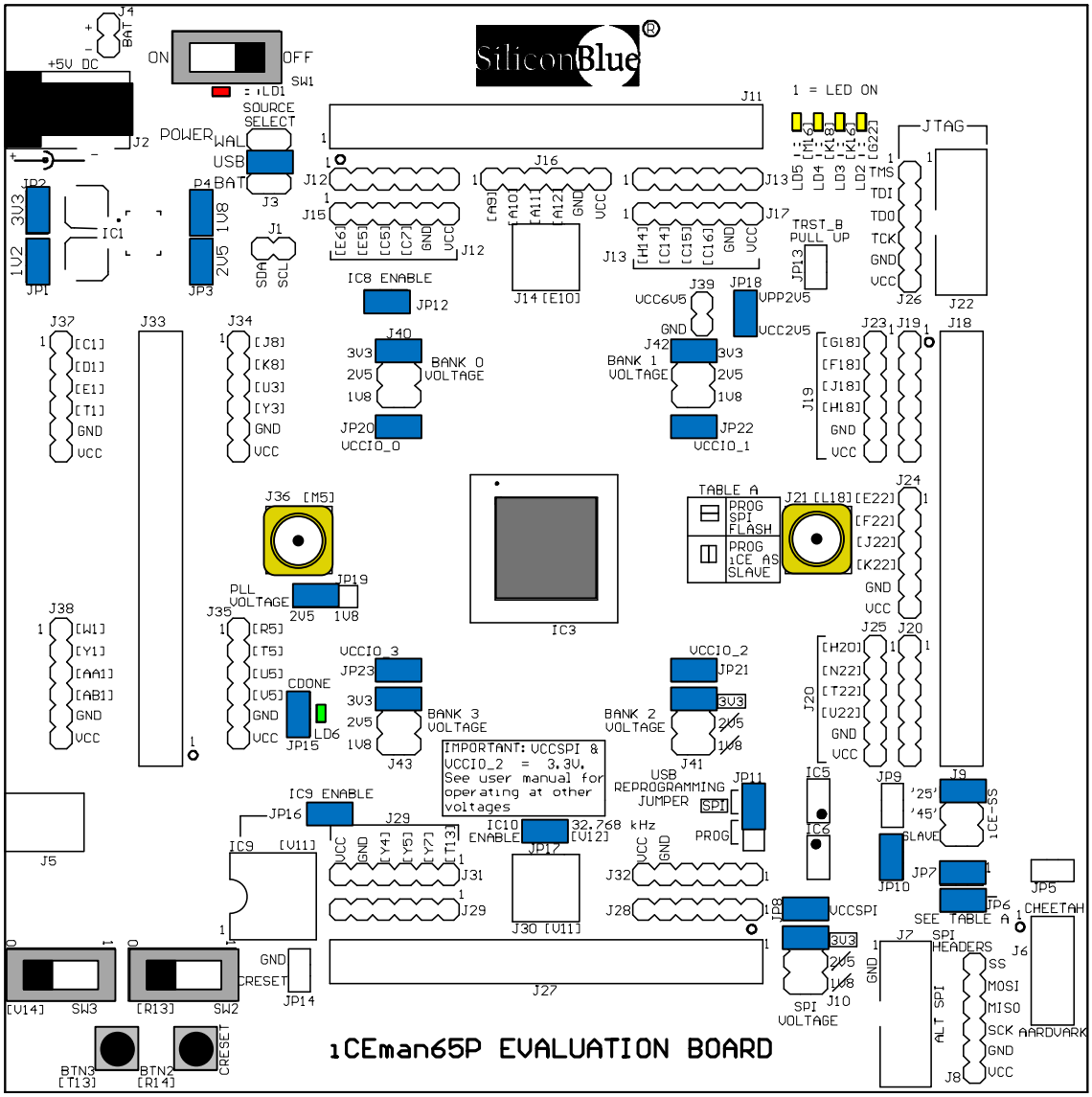
While this test does not comprehensively test the board, here is a list of items and functions exercised by this simple application.

- USB power connection
- iCE65P04 device for basic functionality
- M25P80 SPI configuration memory
- Power switch SW1 and LED, LD1
- LP3906 regulator
- The CDONE LED, LD2
- Four discrete LEDs (Rev. D boards and later), LD3 through LD6
- Slide switches SW2 and SW3
- Pushbutton switches BTN2 (CRESET_B) and BTN3
- 32.768 kHz oscillator
- IC8 oscillator socket and installed oscillator
- PMOD-LED module
- All eight PMOD sockets and connections

Factory Jumper Settings/Component Location, Top-Side

Figure 29 shows the default factory jumper settings and the location of major components on the board. All resistor and capacitor locations are removed for clarity. See Figure 30 for complete top-side silkscreen markings.

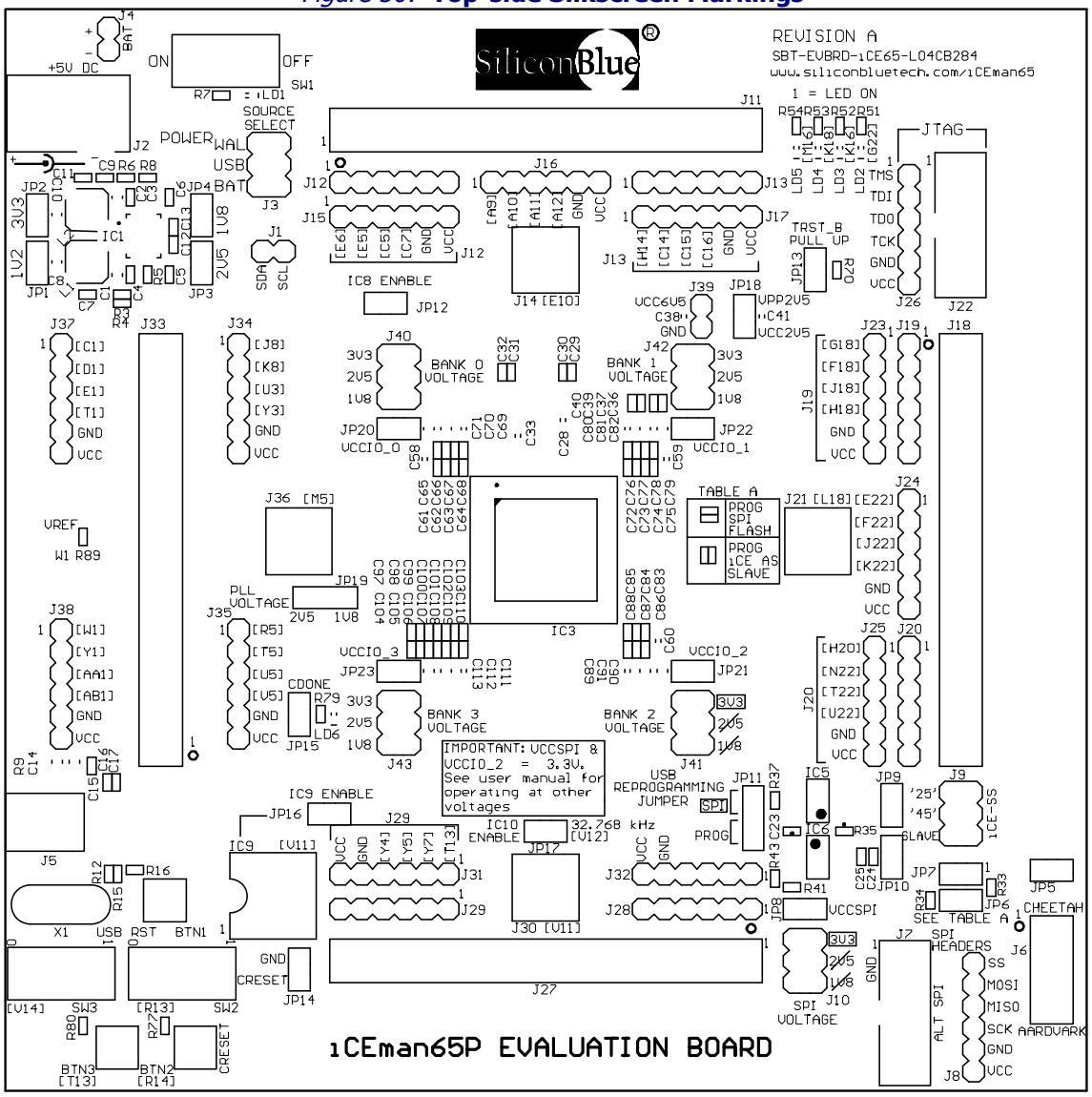
Figure 29: **Default Factory Jumper Settings**



Top-side Silkscreen Markings

Figure 30 shows the top-side silkscreen markings, including reference designators for all components mounted on the top side of the board.

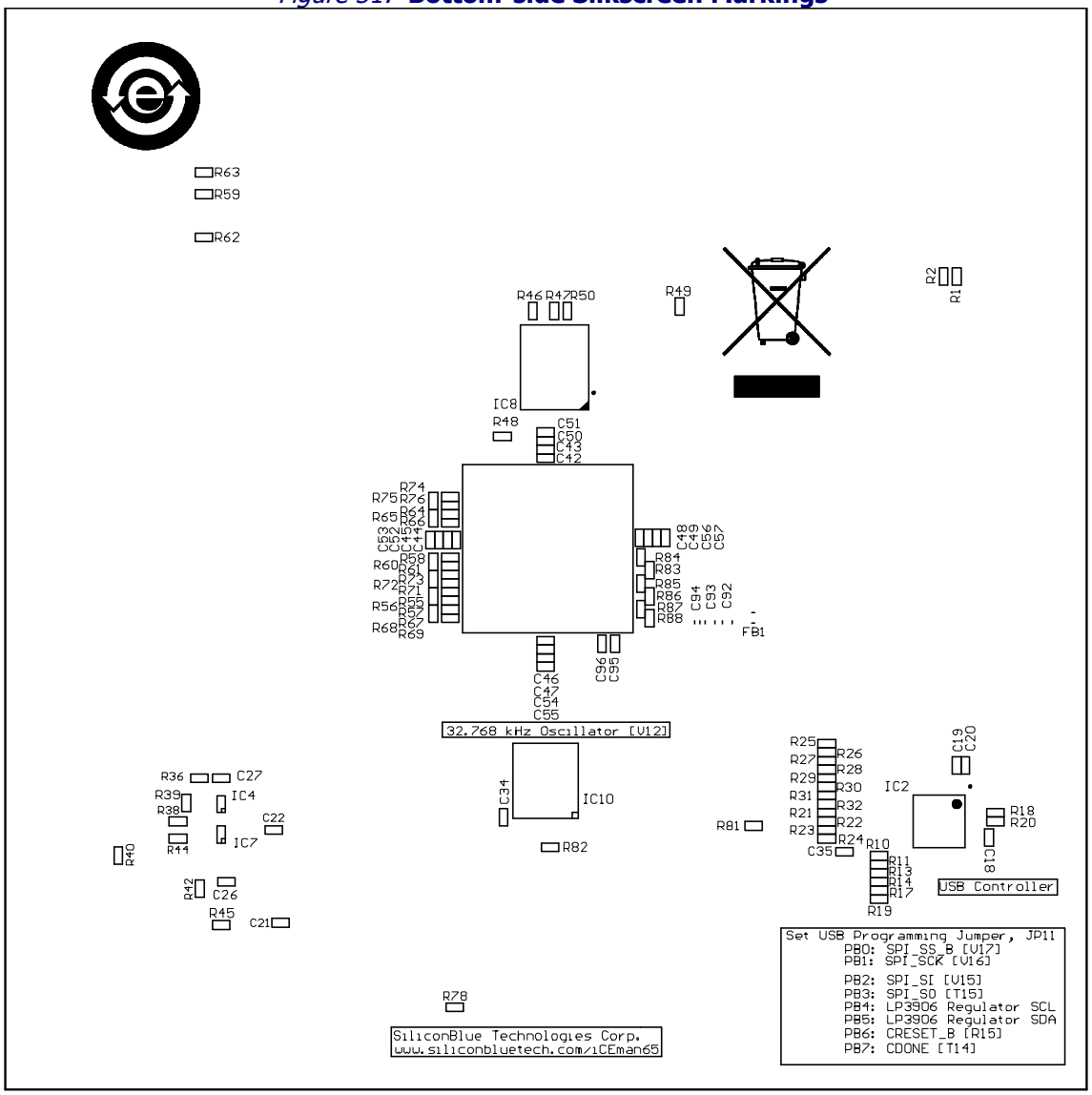
Figure 30: **Top-side Silkscreen Markings**



Bottom-side Silkscreen Markings

Figure 31 shows the top-side silkscreen markings, including reference designators for all components mounted on the bottom side of the board, including the CellularRAM, and the 32 KHz oscillator.

Figure 31: **Bottom-side Silkscreen Markings**



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Reduction of Hazardous Substances (RoHS)

The iCEman65P board is designed for RoHS compliance.

Revision History

Version	Date	Description
1.1	10-DEC-2010	Correct burst performance for CellularRAM mounted on the board. The -708 speed grade supports 80 MHz burst operations. Updated web addresses in Table 28. Added list of programmers required to support the board. Improved quality of graphics in the electronic version.
1.0	12-FEB-2010	Initial release.

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