HOT APPLICATIONS:

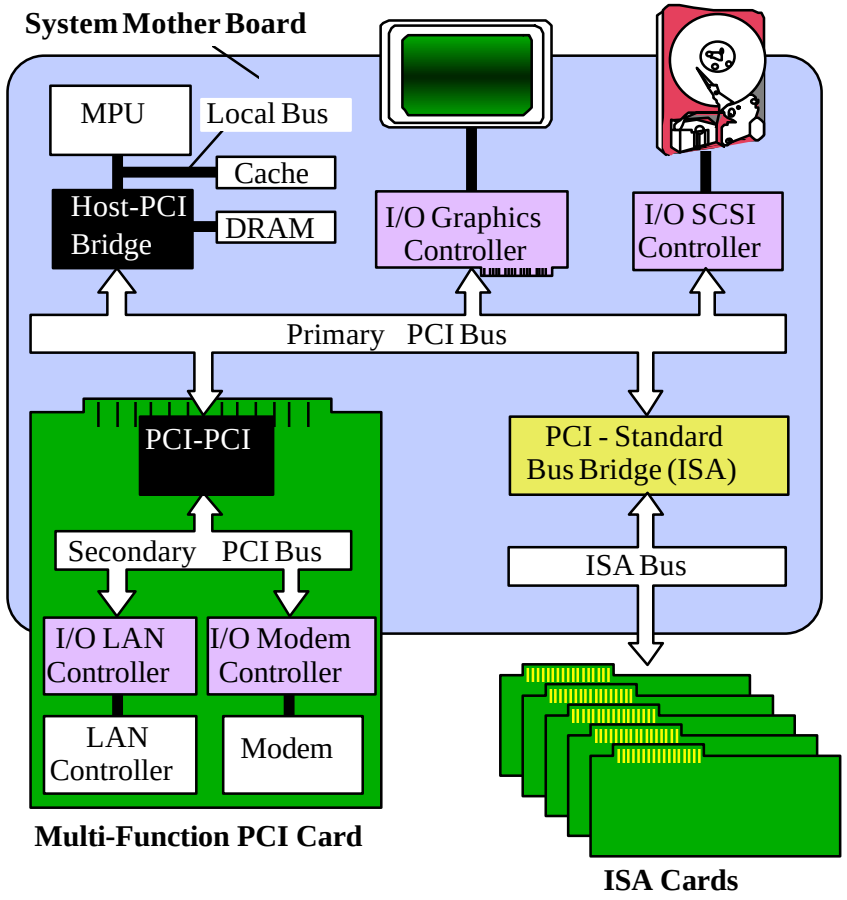
PCI, Plug and Play, PCMCIA

- PCI (Peripheral Component Interconnect)
- Plug and Play ISA
- PCMCIA
- Designing for High-Volume, Low-Cost

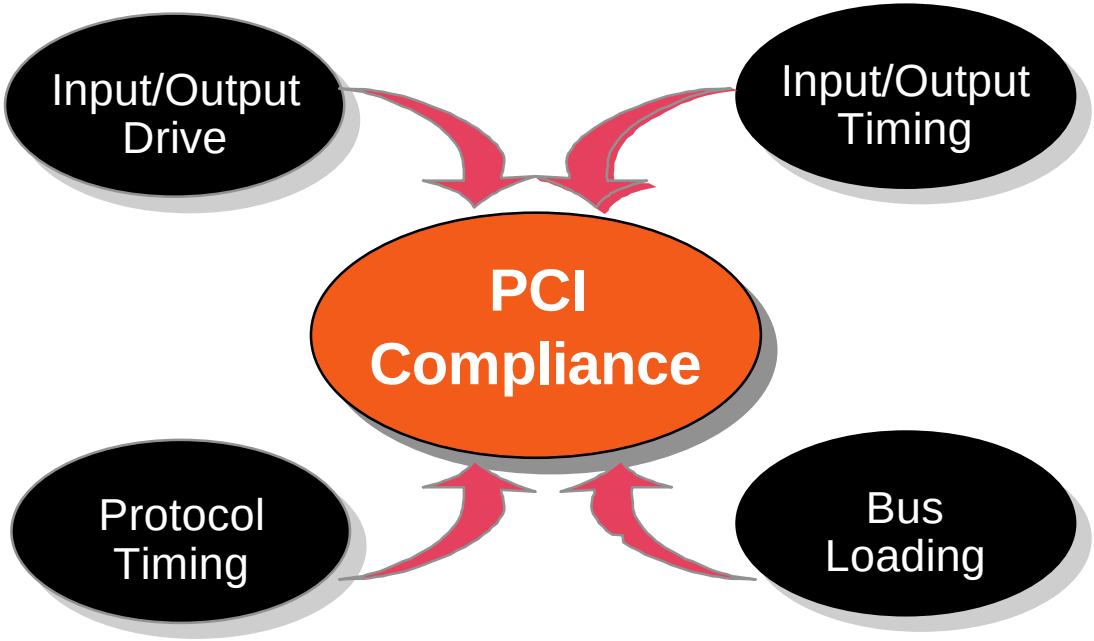
Peripheral Component Interconnect (PCI)

Why PCI?

- New applications—like video—demand higher bandwidth
- Existing ISA architecture too slow
  - Stuck with slow, 8-/16-bit performance
  - Bottleneck for I/O-intensive applications



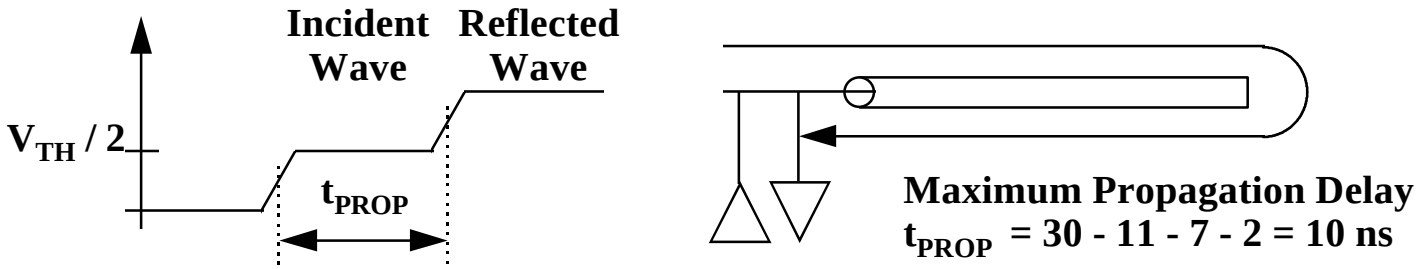
PCI Technical Challenges



- 100% Compliance **REQUIRED** for:
  - Add-in boards to be plugged into ANY PCI system
  - System to accept PCI add-in card from ANY manufacturer

“Reflective-Wave” Switching

- PCI BUS is unterminated, key parameter is Z_O
- Signals ***must*** switch on ***first*** reflected wave



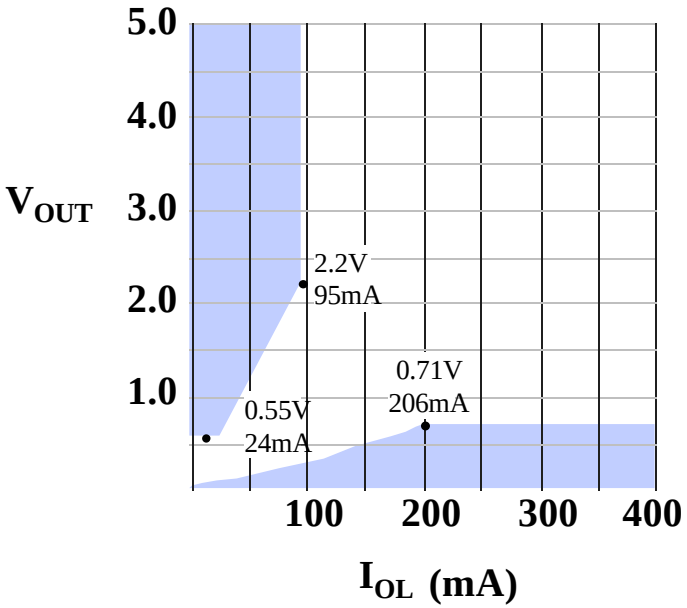
- Signal propagation delays availability of signals
- Signals are compliant when they follow a switching trajectory that defines both current and voltage (V/I Curves)

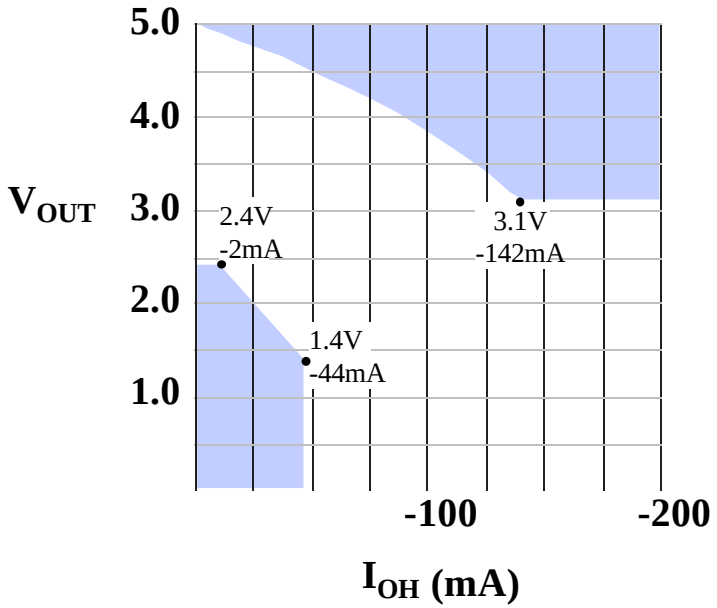
Bus Loading

- Loading
  - PCI BUS is unterminated, key parameter is capacitance
  - Maximum limit is 10 loads @ 10 pF each per bus pin
  - Add-on cards restricted to 2 loads max
  - Single device pin per board pin
  - Expansion board (bridge) is needed to exceed max limit
- Xilinx input capacitance is measured to be **less than 10 pF per device pin** for plastic packages
  - EPLDs: XC7300-10 and faster in PQFP
  - FPGAs: XC3100A-2, XC4000E-3 and faster in PQFP

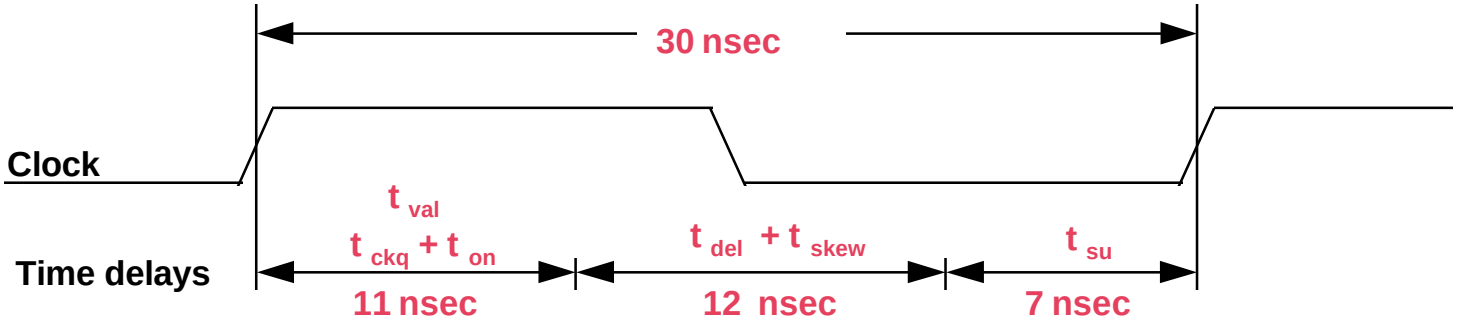
Input/Output Drive Specifications

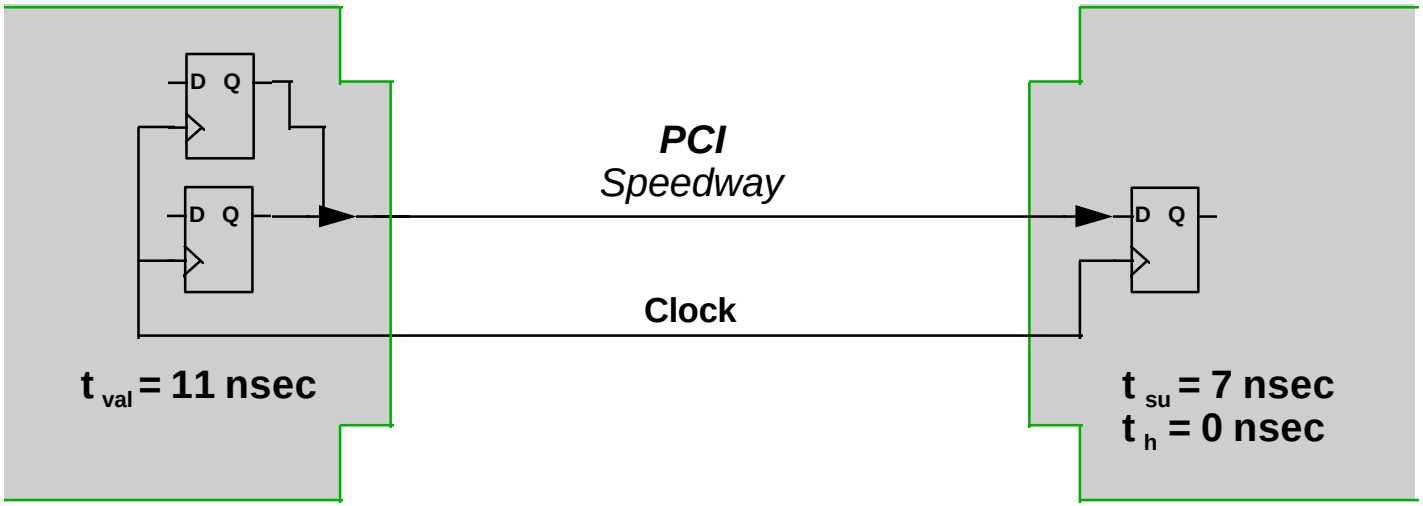
- PCI I/O drive is defined to correctly manage signal reflection within the impedance requirements of the PCI bus
- PCI defines a region on a V/I diagram with **specific measurement points**



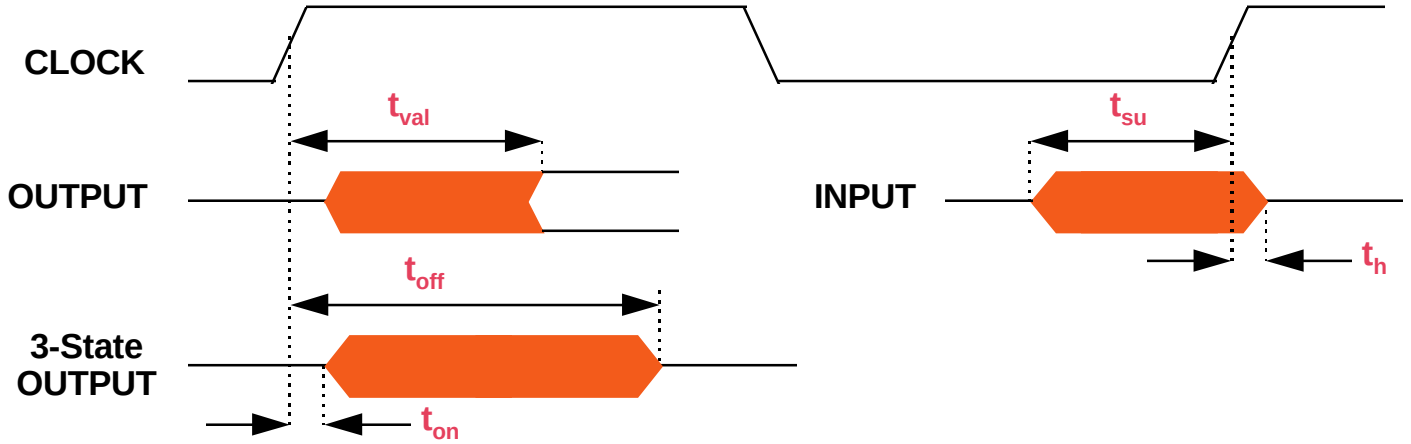


Composite Input / Output Timing





Detailed PCI Timing Specifications



Parameter	5 V Signaling min	5 V Signaling max	3.3 V Signaling min	3.3 V Signaling max	Units
t_h	0		0		nsec
t_{su} (bussed)	7		7		nsec
t_{su} (point-to-point)	10		12		nsec
t_{val} (bussed)	2	11	2	11	nsec
t_{val} (point-to-point)	2	12	2	11	nsec
t_{on}	2		2		nsec
t_{off}		28		28	nsec

REFERENCE

PCI Three-state Buffer Control:

The Often-Missed Critical Issue

- Turn-around cycles (high-impedance state) inserted at each point where signal drive is passed from one agent to another
- Agents require multiple, independent output enables for different signal classes
- Most programmable logic devices have enough output enables for basic PCI interface — but are there enough for the rest of*your* logic?

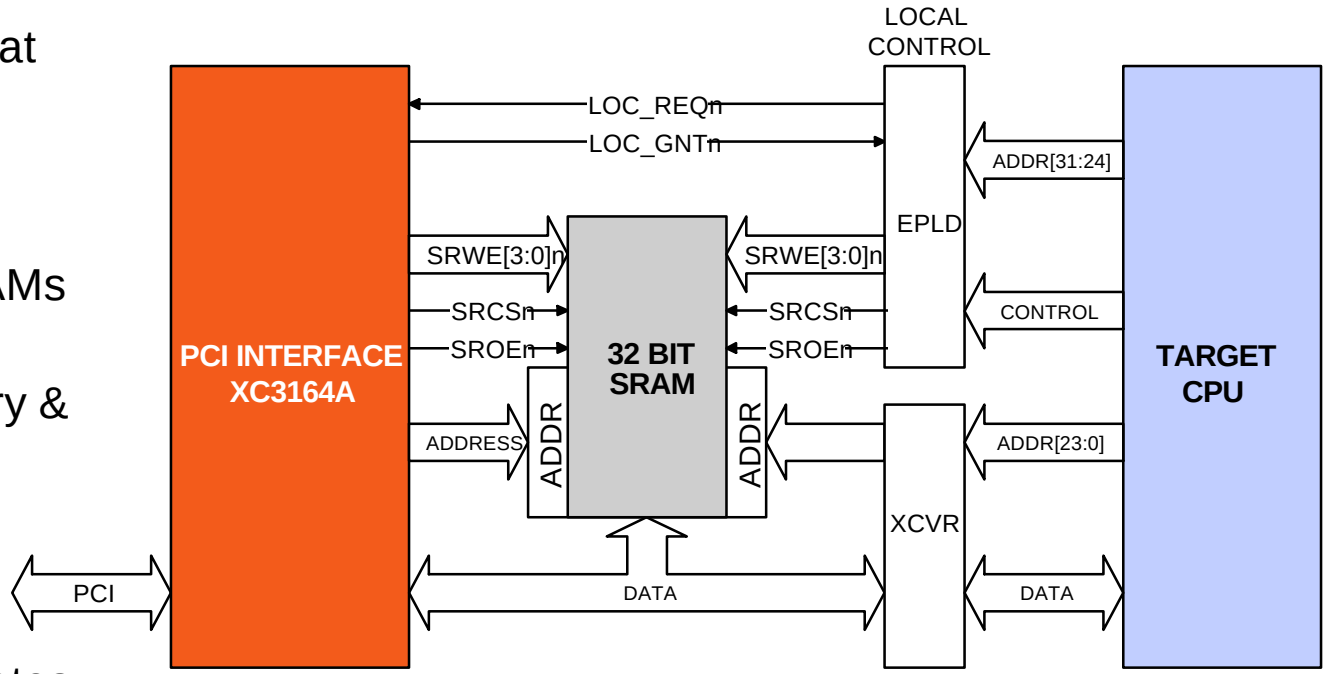
Class of Signals	Signal Name	Initiator/Target	Target
Address Data	AD[31:0]	√	√
Framing	FRAME#, CBE[3:0]#	√	
Parity	PAR	√	√
Parity Error	PERR#	√	√
Master Handshake	IRDY#	√	
Target Handshake	TRDY#,DEVSEL#,STOP#	√	√
Total		**6**	**4**

Xilinx PCI Compliant Solutions

Issue	XC7300 -10/7/5	XC3100A-2 XC3400	XC4000E-3 XC4400
Design Method	PAL/CPLD	FPGA/ASIC	
Process Technology	CMOS EPROM	CMOS SRAM	
PCI Compliance	**100%**	**100%**	**100%**
Gate Density	up to 5K	up to 7.5K	up to 25K
Target Interface	√	√	√
Initiator Interface	Simple	Simple	Full
Configuration Registers	Internal/ External	Internal/ External	Full Internal
Signaling	5/3.3V	5V	
Bus Width	32 bit	32 bit	32/64 bit

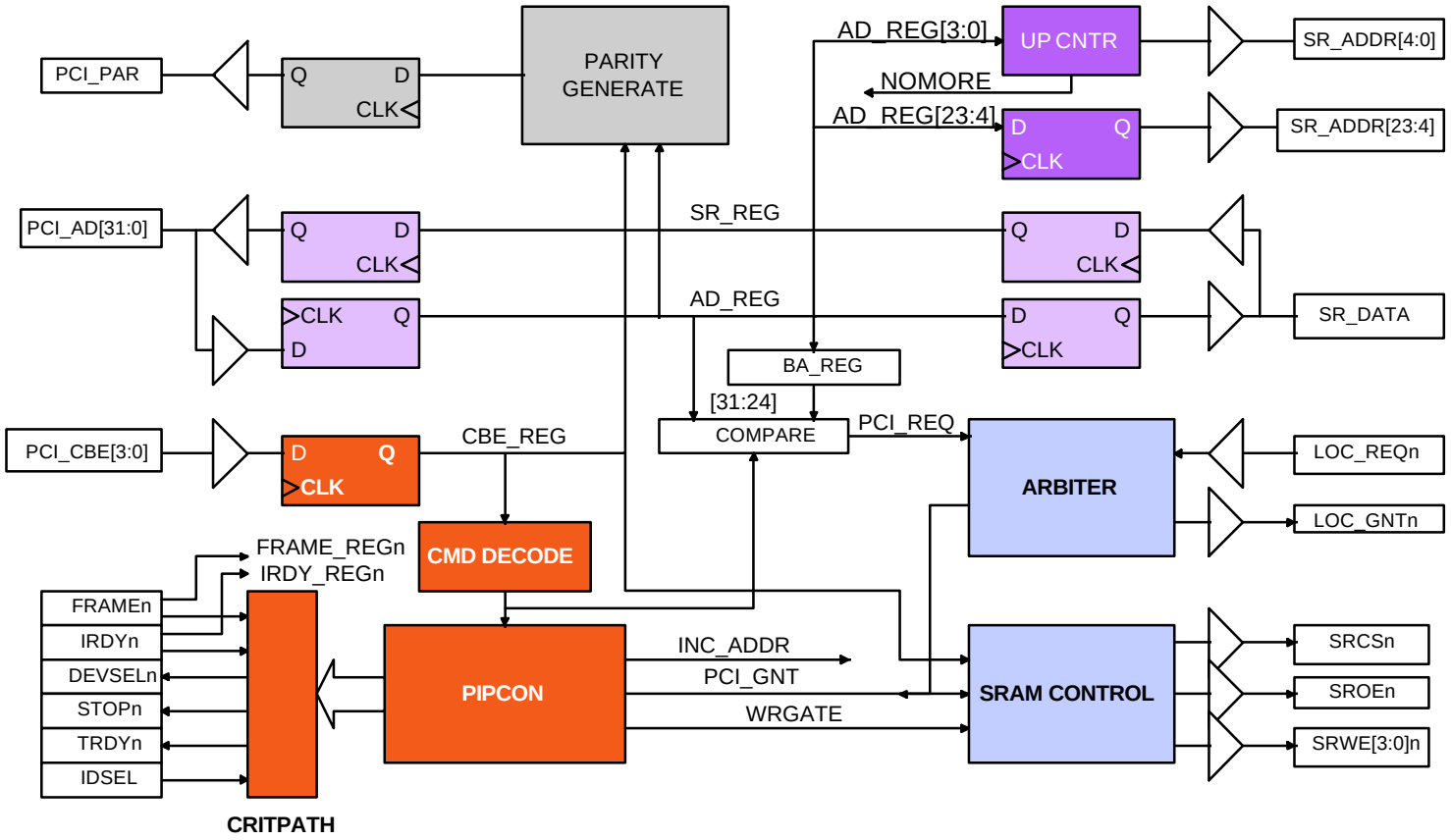
PCI Target in XC3164A-2 FPGA

- Worst Case Design at 33 MHz
- DEVSEL# asserted at clock 5
- TRDY# asserted at clock 6
- Requires 15 ns SRAMs for one clock burst
- Responds to memory & configuration CBE
- Asserts STOP# on address counter overflow and initiator read wait states



On the CD-ROM

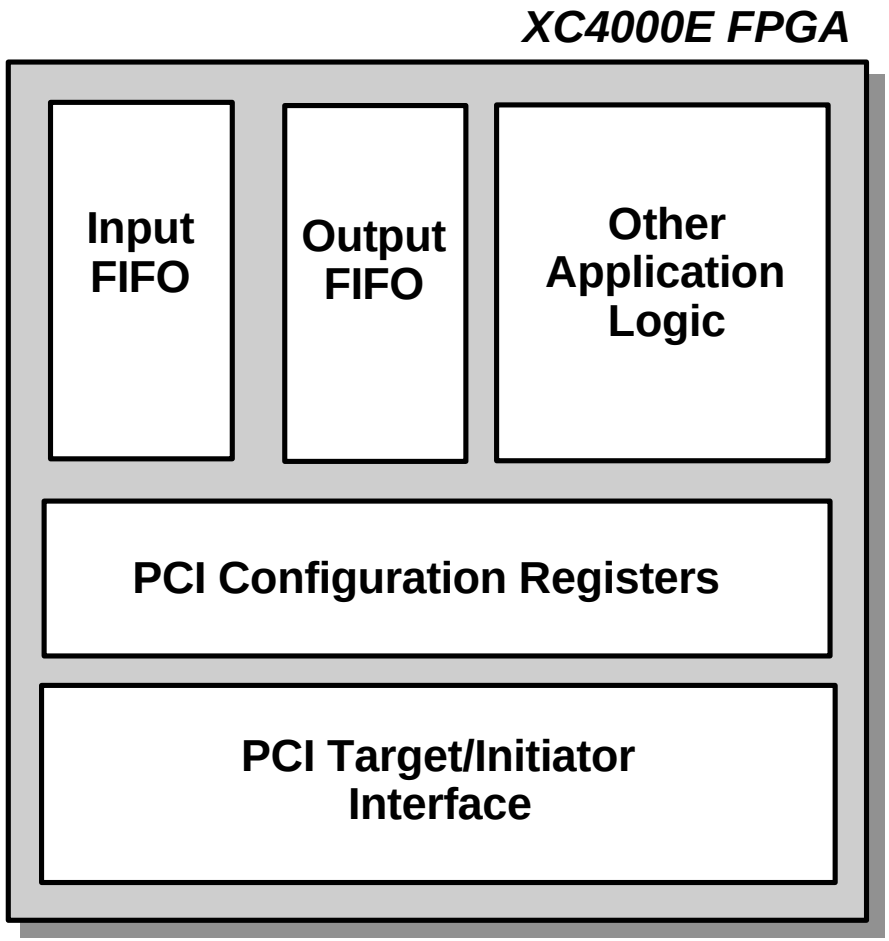
XC3164A PCI Interface Block Diagram



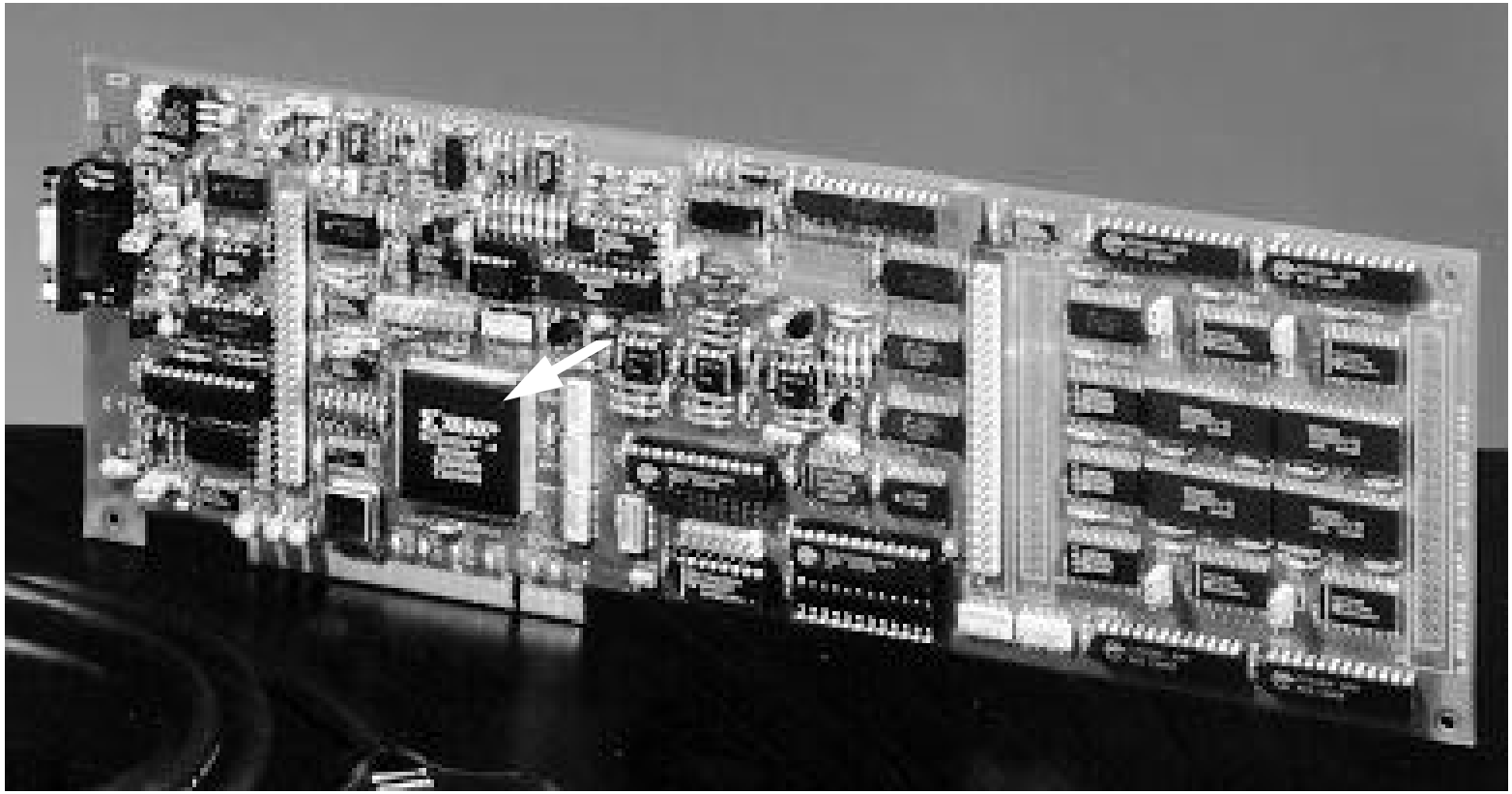
- Pipelined data path
- De-multiplexed address/data bus

XC4000E and PCI

- 100% PCI compliant
- On-chip RAM for
  - Configuration memory
  - FIFOs
- High-density designs
  - Target/Initiator in a single device
- Cost-reduction strategy
  - PCI compliant XC4400 HardWire gate arrays
  - 100% drop-in compatible with XC4000E

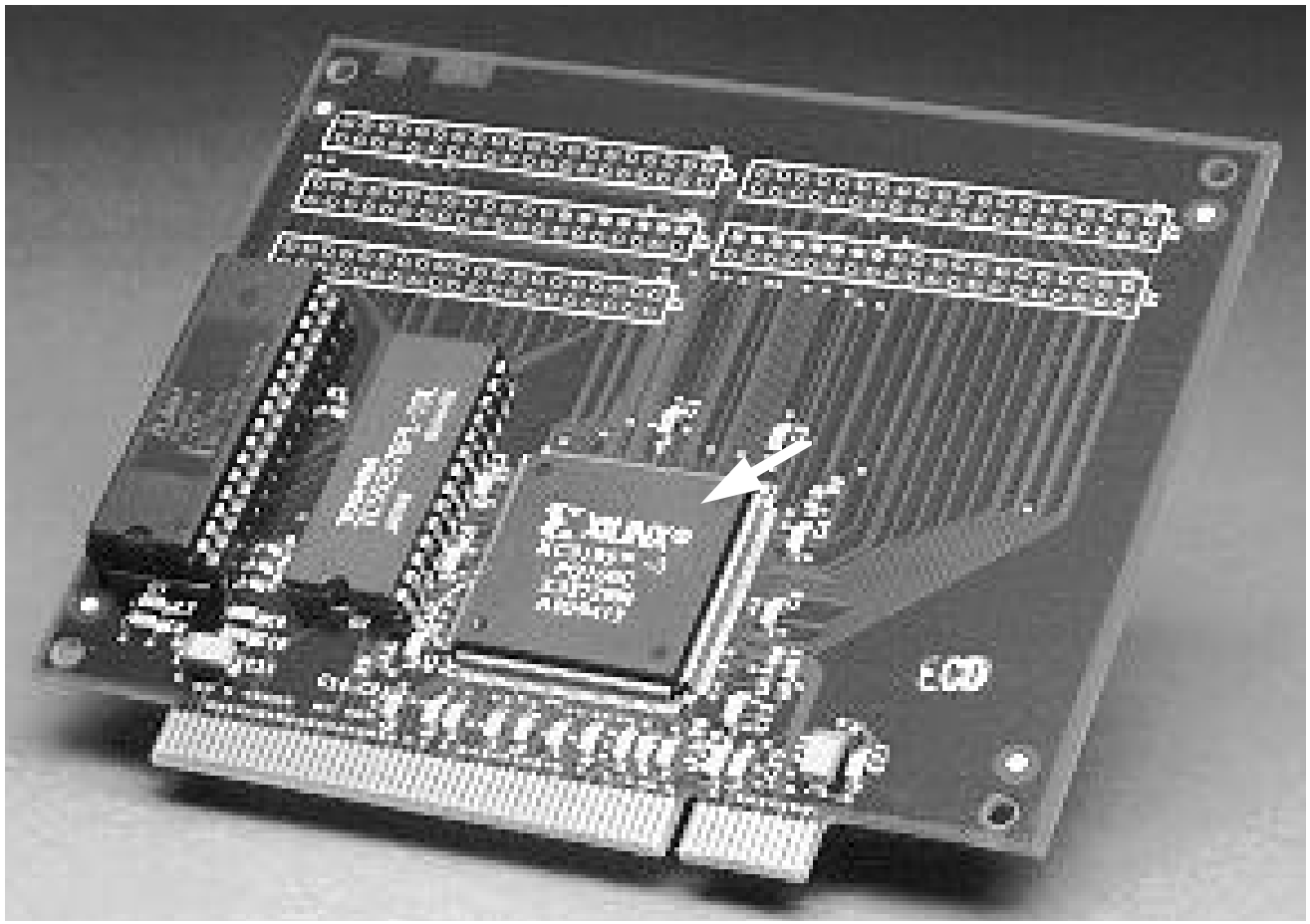


MuTech Video Digitizer PCI Card



- Required 100% PCI compliance using XC3195A
- Integrated specific features not found in PCI chipsets
- Contains PCI interface, capture control, memory control, etc.

PCI Special Interest Group PCI Test Board

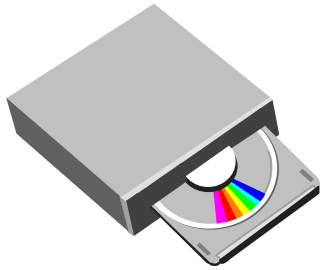


- Tests PCI system compliance

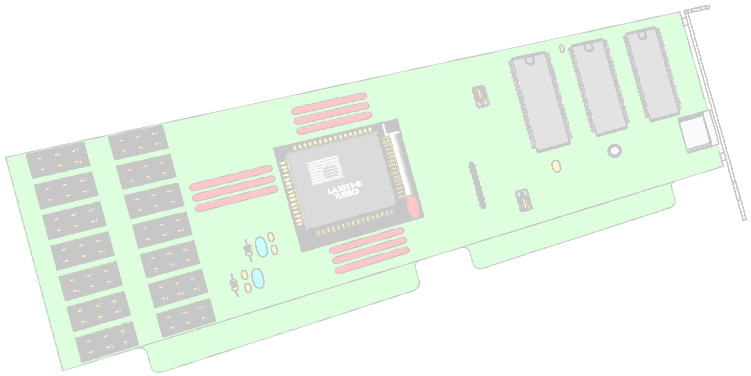
Xilinx PCI Support

- Xilinx is an active member of PCI Special Interest Group (PCI-SIG)
- PCI market backgrounder
- PCI compliance checklists
- XC7300 EPLD App. Note/Design
  - VHDL and ABEL
- XC3164A-2 FPGA App. Note/Design
  - Verilog source files for Exemplar Logic CORE, or
  - VIEWlogic schematics
- EMAIL: **pci@xilinx.com**
  - Literature requests
  - Technical questions

	XC7300	XC3100A	XC4000E
Compliance Checklist	√	√	3Q '95
Target App Note and Design Files	√	√	
Initiator/Target App Note		3Q '95	3Q '95



Plug and Play ISA Interface



Why Plug and Play ISA?

- No mechanism for allocating resources among ISA cards in a system
- Current ISA cards require “jumper” to control memory and I/O space, to steer DMA and interrupts
- Other bus standards are already “Plug and Play” (NuBus, Micro Channel, EISA, PCI)
- Plug and Play ISA retrofits same capabilities into the industry’s most popular bus standard
- Plug and Play ISA cards will co-exist with today’s ISA cards
- Windows ‘95 and Plug and Play BIOS coming soon

Plug and Play ISA Technical Challenges

- No significant technical challenges (except understanding the specification)
- Every ISA board has different interface requirements
- Need low-cost solution for high-volume ISA market

Plug and Play Configuration Sequence

- Cards power-on in quiescent state
- Plug and Play software sends initiation key telling all cards to begin configuration process
- Plug and Play software isolates one card at a time
- Assigns a “handle” to the isolated card and reads its resource requirements
- After reading all cards’ requests, assigns conflict-free resources to each card
- Activates all Plug and Play ISA cards and removes them from configuration mode

Isolation Protocol

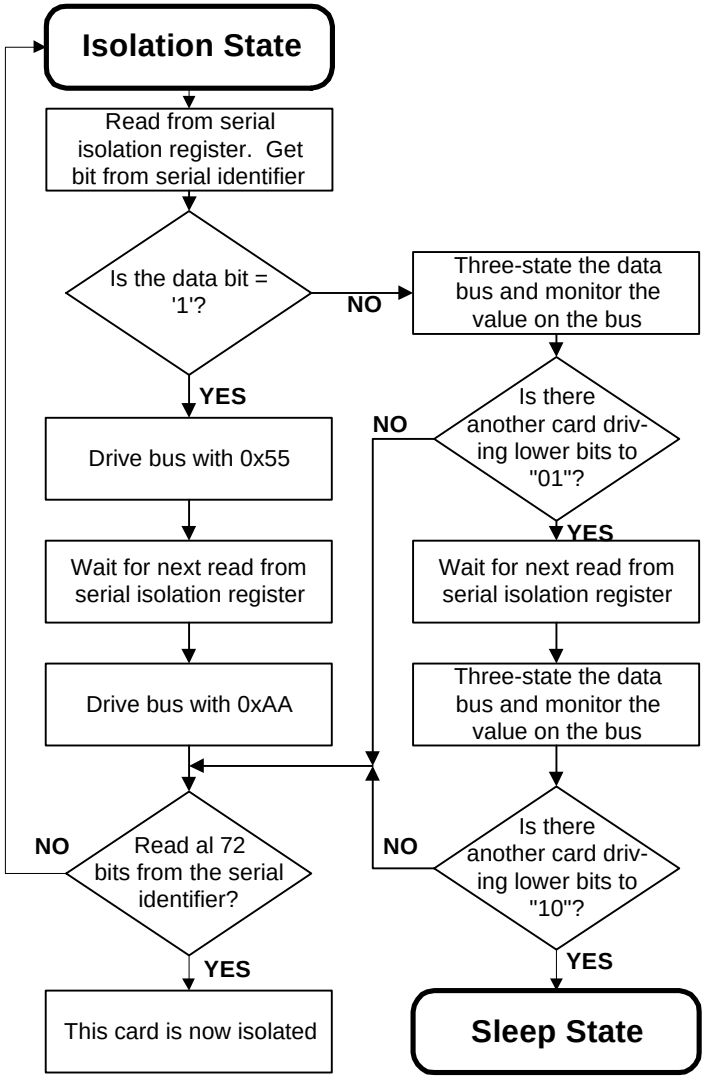
- 72-bit Serial Identifier

Check-sum	Serial Number				Vendor ID			
Byte 0	**Byte 3**	**Byte 2**	**Byte 1**	**Byte 0**	**Byte 3**	**Byte 2**	**Byte 1**	**Byte 0**
7:0	7:0	7:0	7:0	7:0	7:0	7:0	7:0	7:0

Shift Direction

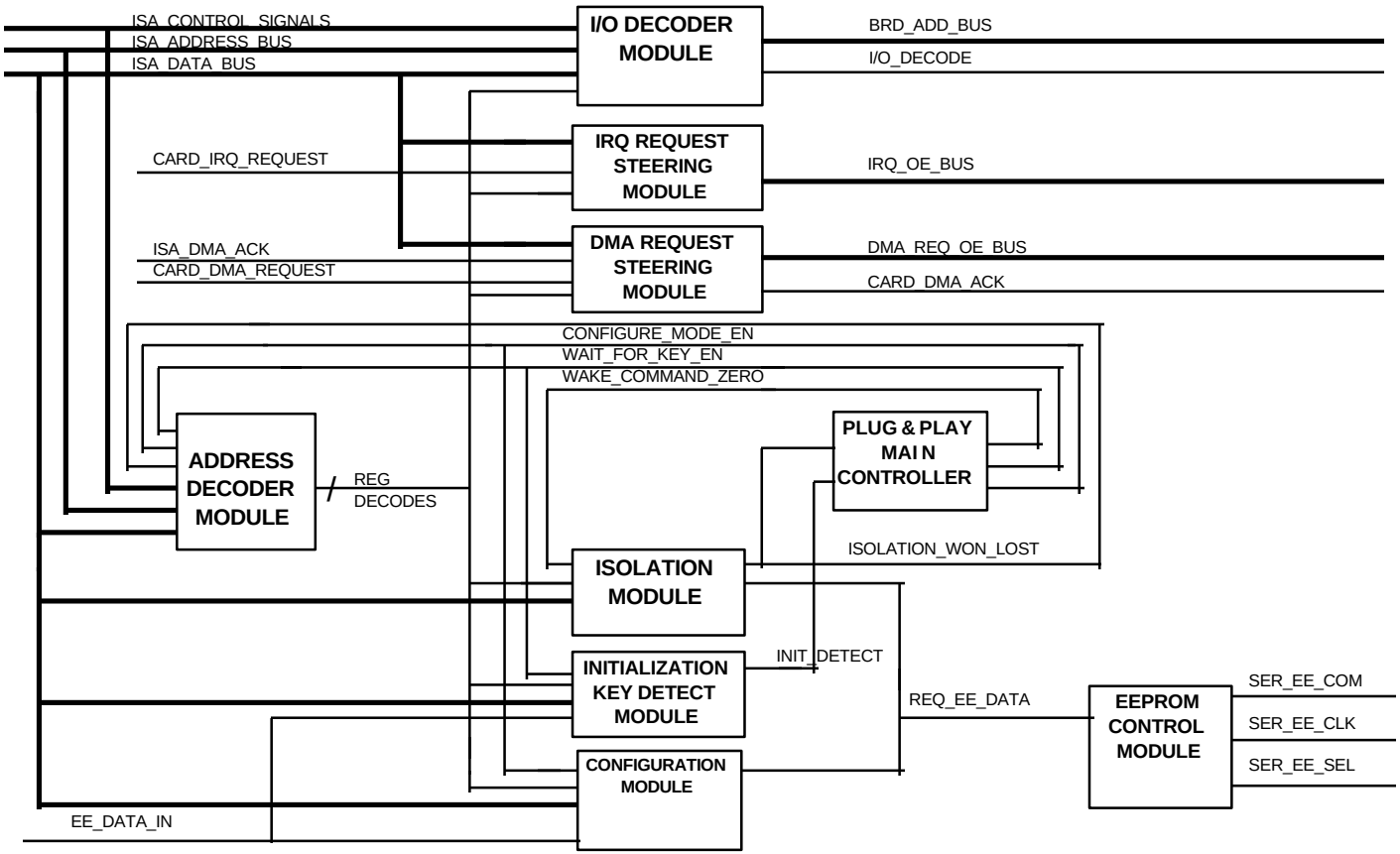
  - Unique for every card
  - Recorded internally or in EEPROM

- Isolation State Machine
- All non-isolated cards compete in each isolation round



REFERENCE

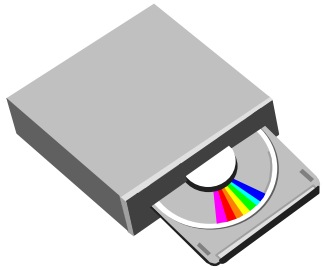
Xilinx Plug and Play Solution



On the CD-ROM

Xilinx Plug and Play ISA Application Notes

- "A Plug and Play Interface with Xilinx FPGAs" Application Note/Design
  - Fully compatible with Plug and Play ISA 1.0a
  - Supports 8-bit ISA bus interface, expandable to 16 bits
  - Supports all 7 DMA channels
  - Supports all 15 IRQ channels
  - Optional serial EEPROM interface for serial ID and card data
  - Built using XC4003 or XC5200
  - **VIEWdraw schematics and ABEL source files**
- "Plug and Play ISA" background
- E-Mail: **`PnP@xilinx.com`**
  - Literature requests
  - Technical questions



PCMCIA

Personal Computer Memory Card Interface Association

"People Can't Memorize Computer Industry Acronyms"

Why PCMCIA?

- Originally developed as a memory card interface
- Extended to add I/O and other capabilities
- Popular in lap-tops and portable systems
- Ideally, cards are interchangeable and easy to install
- Applications in industrial markets
- PC Card ‘95 Specification adds:
  - CardBus 32-bit bus master interface
  - 3.3 volt cards (Xilinx ZERO+ 3.3 volt devices)
  - Multifunction cards

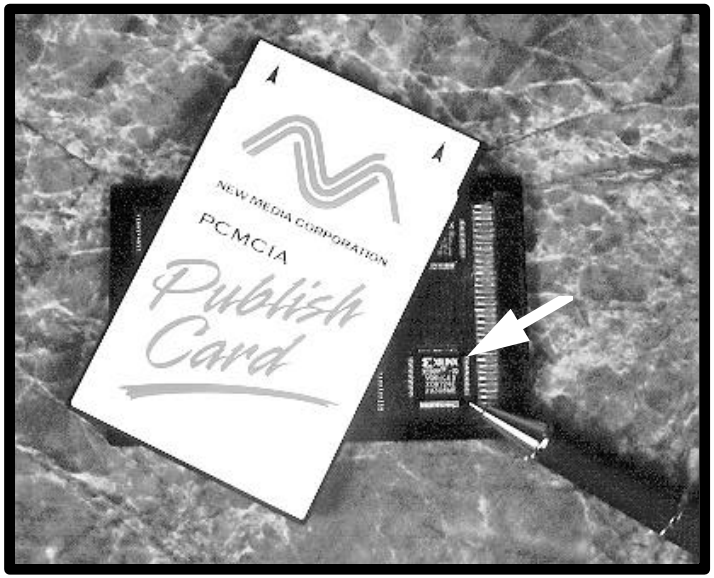
PCMCIA Technical Challenges

- Advanced Packaging
  - Three defined card thicknesses
    - Type 1: 3.3 mm
    - Type 2: 5.0 mm
    - Type 3: 10.5 mm
  - Need Very-Thin Packaging
    - VQFP (1.27 mm high) for double-sided Type 1 cards
    - TQFP (1.55 mm high) for single-sided Type 1 cards
  - Devices requiring a programmer are difficult to handle
- Need low-cost solution for high-volume PCMCIA market
- Short life cycles — need fast time-to-volume

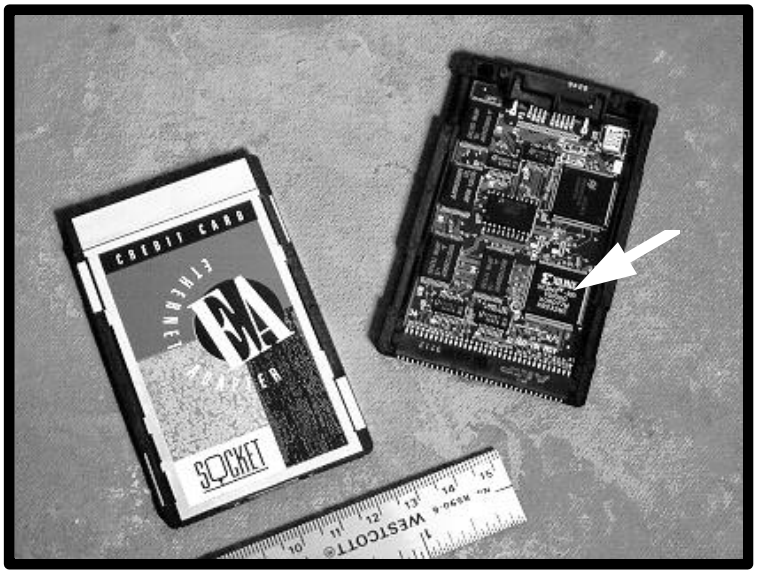
Xilinx Advance Surface-Mount Packaging Options

- Wide variety of devices available in**T**hin **Q**uad **F**lat **P**ack (TQFP) and **V**ery-thin **Q**uad **F**lat **P**ack (VQFP) packages
  - XC3000A (VQ64, VQ100, TQ100, TQ144, TQ176)
  - XC4000 (VQ100, TQ144)
  - XC5200 (VQ100, TQ144) *Up to 10,000 gates!*
- Serial PROM available in easy-to-program 8-pin very-thin SOIC
- FPGAs are in-system programmable—mount directly on board, no programming
- 3.3 volt versions available including Xilinx HardWire gate arrays

PCMCIA Products Using Xilinx



New Media

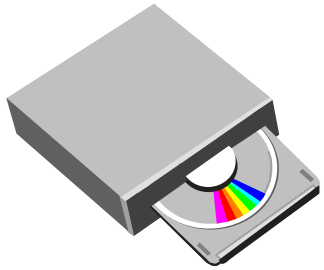


Socket Communications

- Over 100 volume-production designs to date
  - Mostly XC2000, XC3000A FPGAs (XC4000 in many new designs)
  - XC2318 and XC3x00 HardWire gate arrays

Xilinx PCMCIA Application Notes

- PCMCIA backgrounder
- “Speed PCMCIA Modem Design with FPGAs”
  - Application Note
  - VIEWlogic schematics
- “Incorporating CIS into XC4000 PCMCIA Designs”
- E-Mail: **pcmcia@xilinx.com**
  - Literature requests
  - Technical questions



Xilinx Third-Party Support for PCMCIA

- Complete PCMCIA development systems, debugger software and tools available from:

B&C Microsystems

750 North Pastoria Avenue
Sunnyvale, CA 94086
(408) 730-5511

Focus Microsystems

1735 N. First Street
Suite 307
San Jose, CA 95112
(408) 436-2336

Mobile Media Research

1977 O'Toole Ave B-207
San Jose, CA 95131
(408) 428-0310

- PCMCIA recommended design guide for host and card systems:

Sycard Technology

651 Smoke Tree Way
Sunnyvale, CA 94086
(408) 247-0730

REFERENCE

Designing for High-Volume, Low-Cost Applications

- Computer solutions are usually high-volume applications
- Big opportunities in new markets
  - Specifications are in a state of flux
  - First-to-volume reaps the profits
  - Later in life cycle, need to compete on price
- The Winning Combination: Xilinx “Design Once” Methodology
  - Xilinx programmable solutions for development and initial production
  - Cuts your time-to-market and provides maximum flexibility
  - Migrate design to Xilinx HardWire gate arrays for cost reduction
  - 100% compatibility reduces your risk

Conclusion

- Xilinx provides successful solutions for important computer applications
  - PCI
  - Plug and Play ISA
  - PCMCIA
- Design assistance improves your time-to-volume
  - Technical requirements understood and addressed
  - Application notes and reference designs
  - Examples of successful end-user products
- “Design Once” methodology provides start-to-finish success for high-volume, low-cost applications
  - Xilinx programmable logic
  - Xilinx HardWire gate arrays