Session 7.7

Field Configurable System-on-Chip: Device Architecture

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Agenda

- **Industry Trends**
- **The Next Logical Step: A Configurable System-on-Chip**
- **Technical Challenges**
  - System communication, device structure
  - Debugging
  - Maintaining hardware/software design flows
- **Summary/Questions**

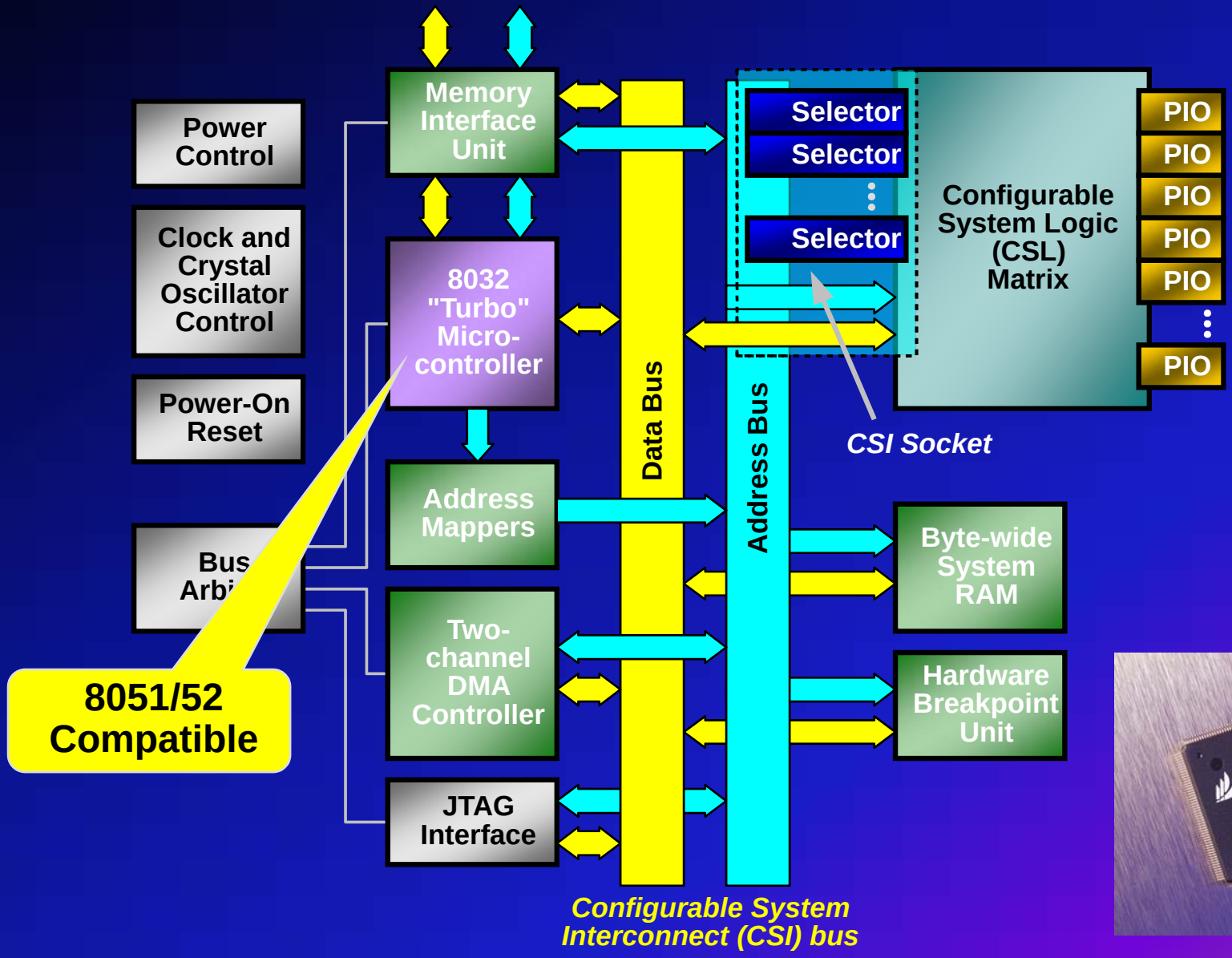
Industry Trends

- Advanced process technologies enable cost-effective system-on-a-chip designs and multi-million-gate FPGAs
- ASIC/FPGA densities now outstrip the capabilities to easily verify a design
- Adaptability is a desirable attribute
- Integrating system logic (memory, CPU) is expensive in FPGA logic

Configurable System-on-Chip (CSoC)

- Pre-verified, configurable system--integrated on a single chip
- Leverages standard logic design and processor development tools
- Leverages the design advantages of both processors and programmable logic
- Fast time-to-market for embedded systems
- System-on-a-chip for the masses

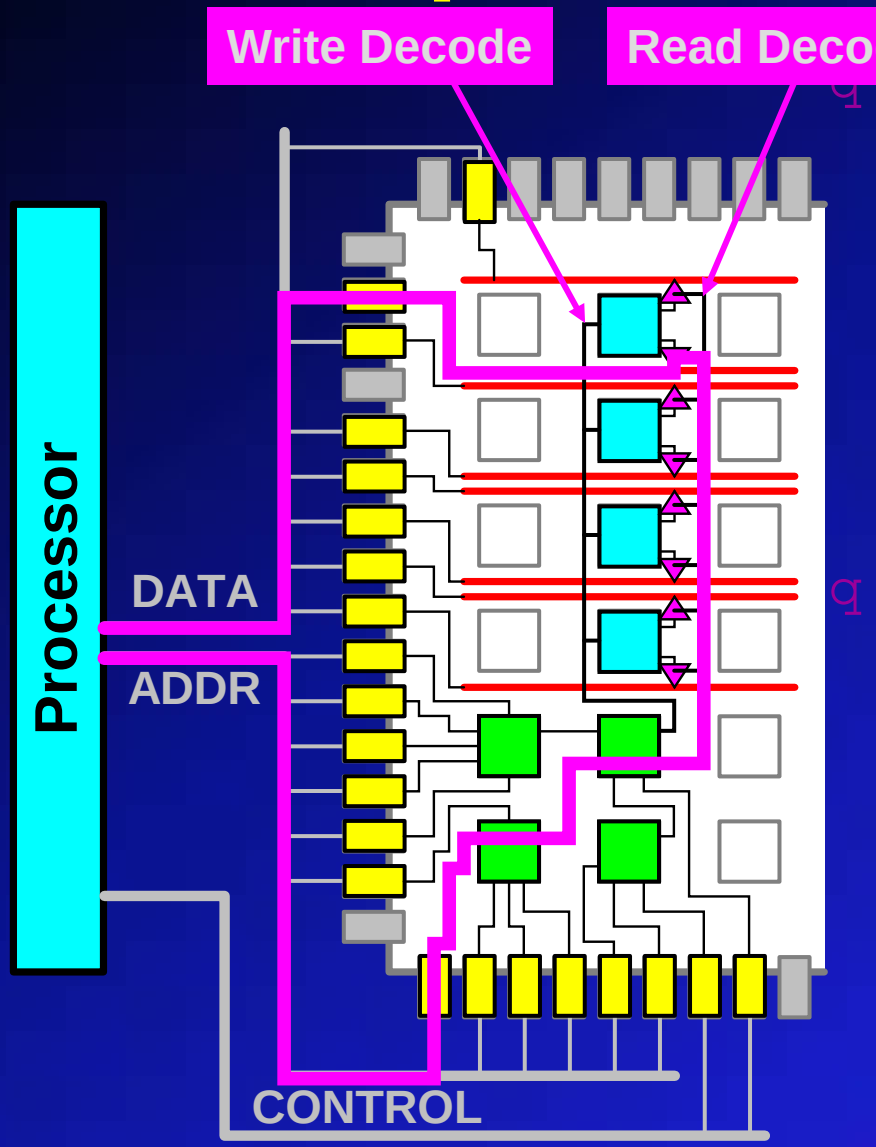
E5 Configurable System-on-Chip



CSoC Technical Challenges

- Communication between the system and programmable logic functions
  - Connecting to the data and address bus
  - Decoding/controlling bus transactions
  - Register intimacy
  - Debugging a system with both processor and programmable logic
- Maintain standard development flows
  - Leverage available compilers, debuggers
  - Leverage existing logic design tools

Two-Chip Solution: CPU+FPGA



I/Os between devices

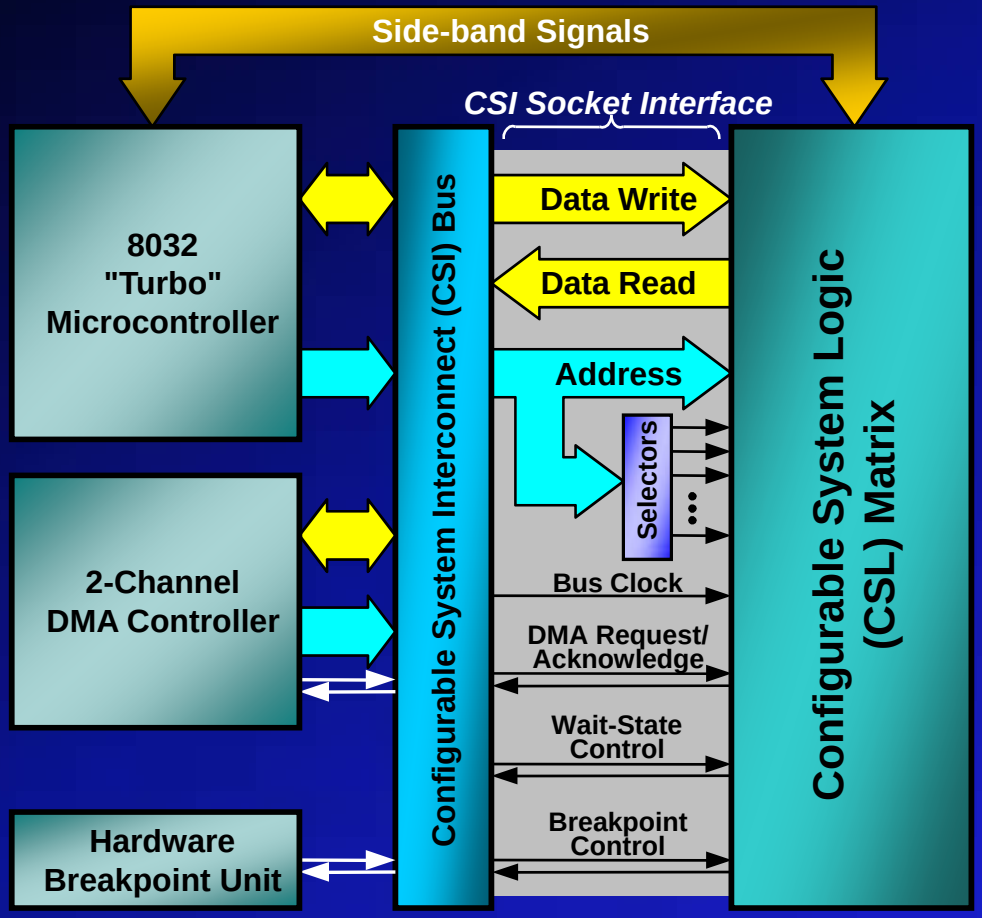
- Many pins, even for basic 8-bit interface
- Delay in critical path
- Extra power consumption, EMI

Distributing address/ data on-chip

- Uses programmable interconnect
- More critical path delay
- Variable delays in some architectures
- Bidirectional data

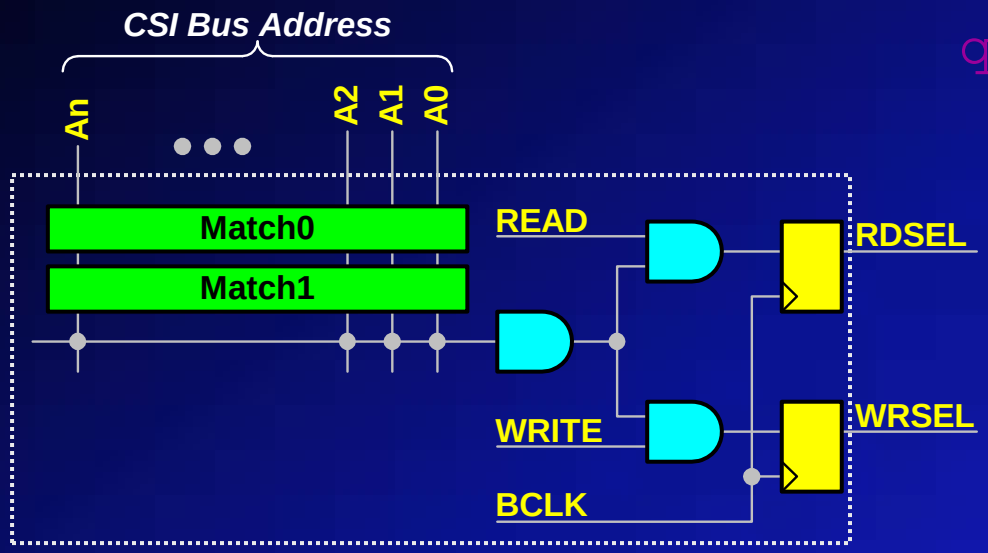
CSI Bus Socket

(Configurable System Interconnect)

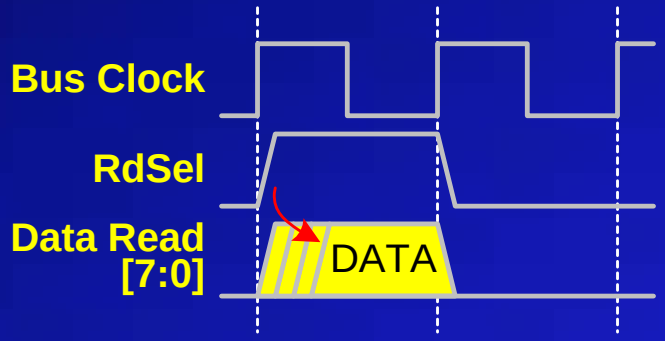


- Distributes bus signals to embedded program-mable logic
- No I/O required
- Predictable, synchronous timing
- Forward compatible with future device families
- Contention-free bussing
- Wait-state control
- DMA access
- Integrated debugging

Selector (Address Decoder)



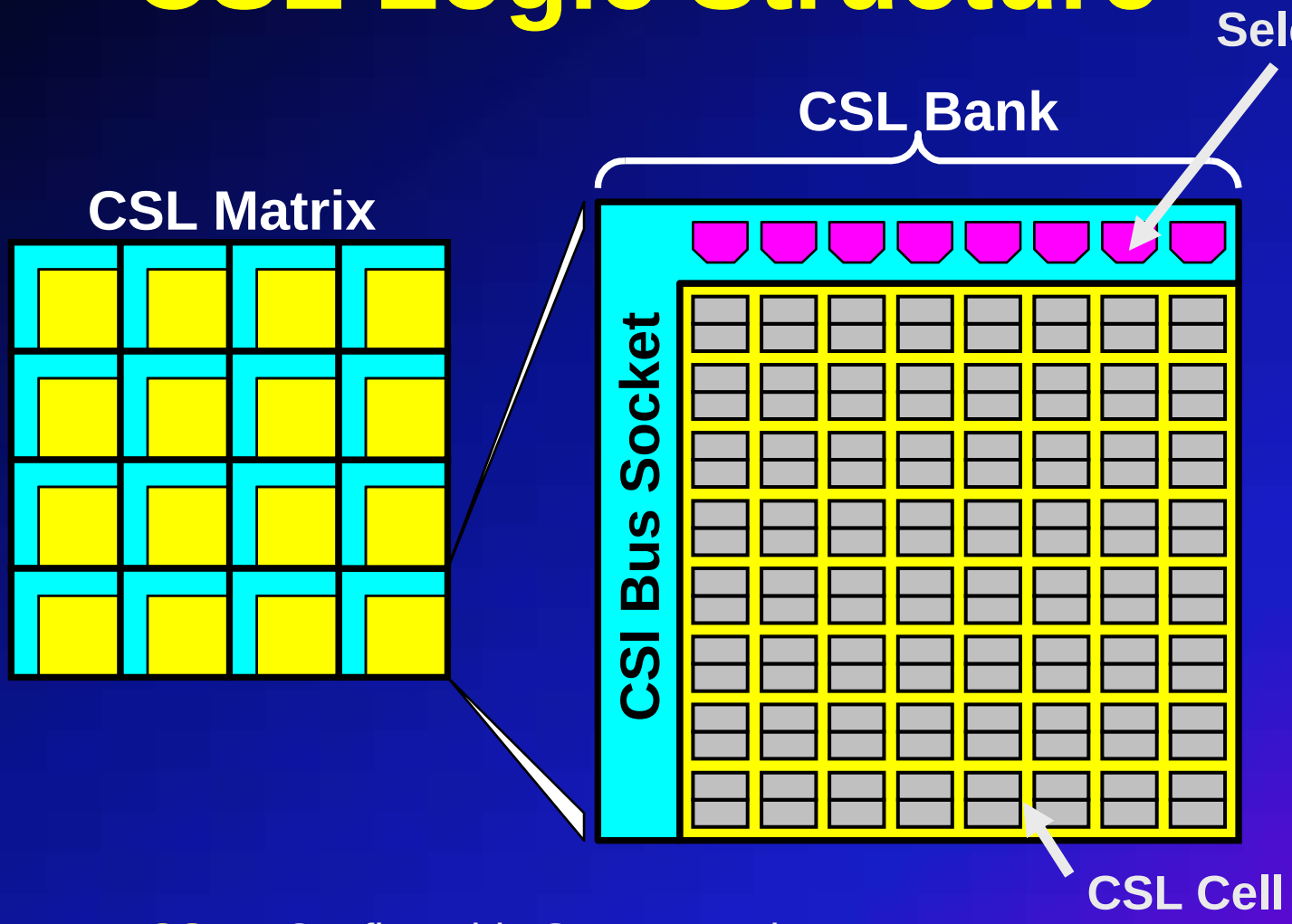
- **Fast address decoding**
  - Any address range
  - Access type
    - Code
    - Data
    - Special Function Register (SFR)



- **Decode delay is constant (less than 5 ns after clock)**

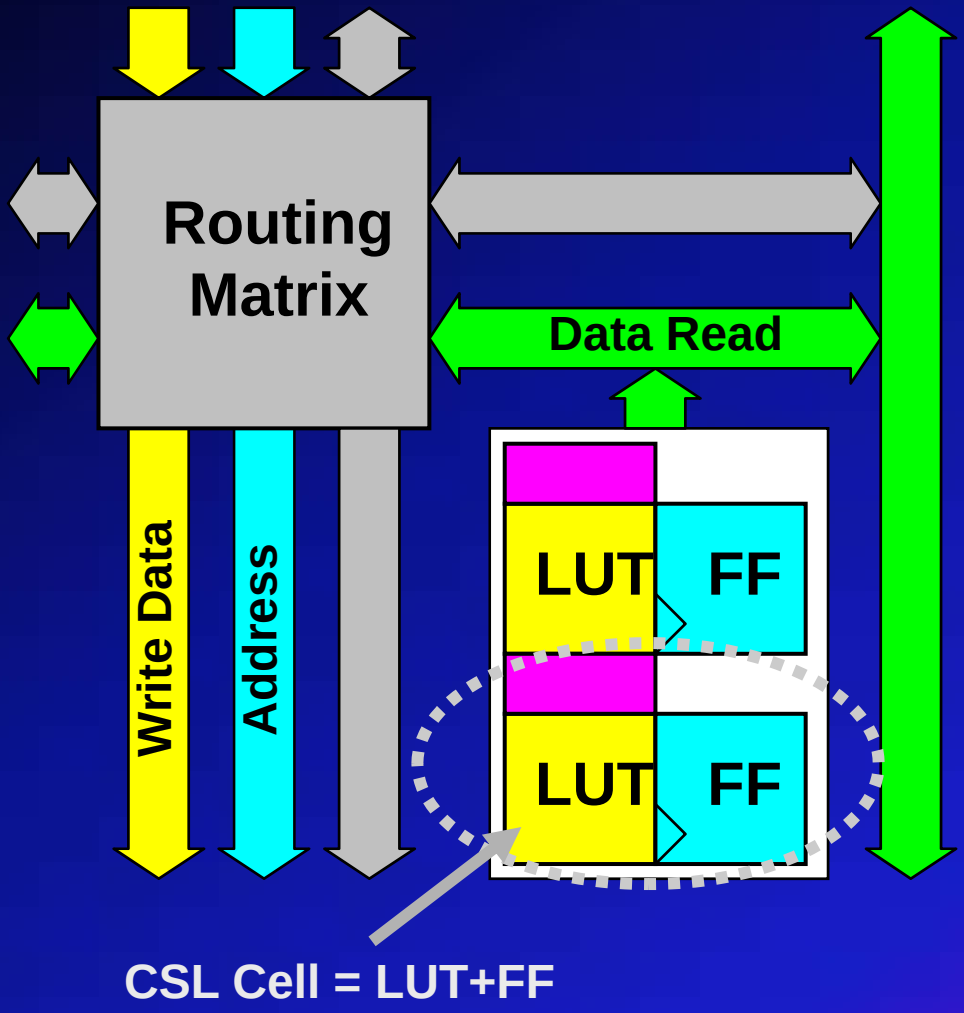
Device	Selectors
TE502	16
TE505	32
TE512	72
TE520	128
TE532	200

CSL Logic Structure



- **CSL** = Configurable System Logic
- **CSI** = Configurable System Interconnect

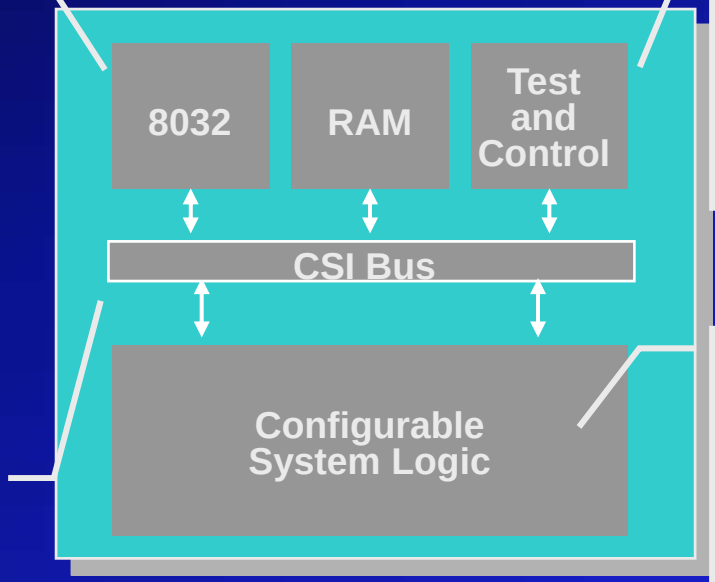
CSL Cell Structure



- **CSL cell perform various functions**
  - Logic
  - Arithmetic
  - Memory
  - Bus
  - Sequential
- **Intimate connection to the CSI system bus**

Configurable System-on-Chip Debugging Capabilities

Access to all address mapped and other key processor resources

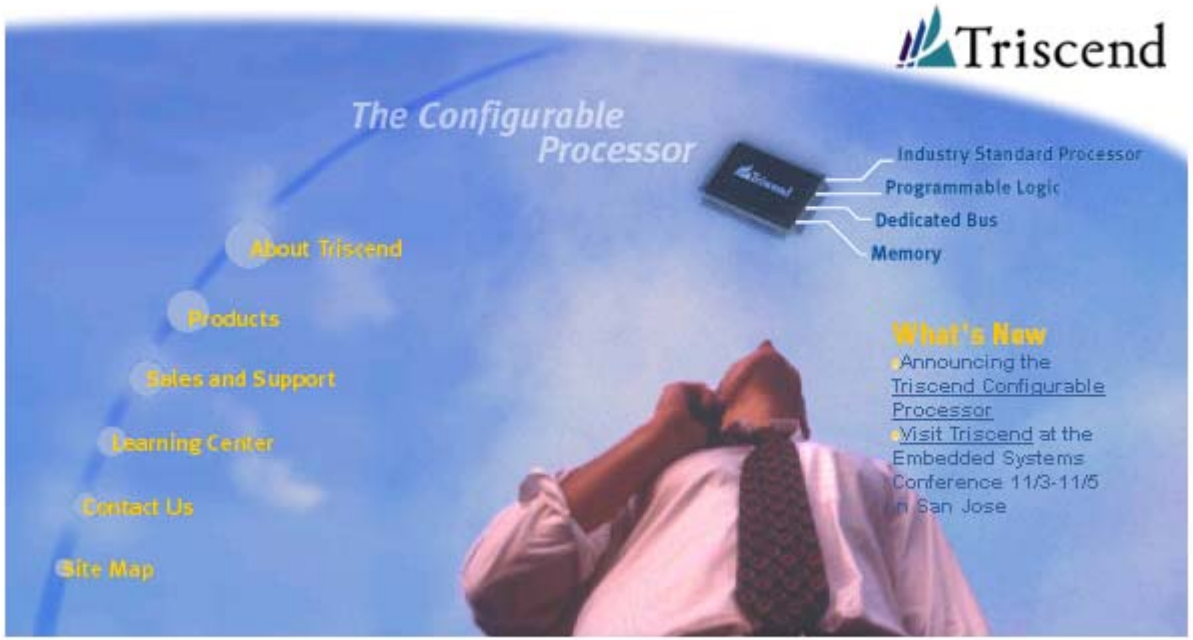


Commands from 3rd party debuggers translated to JTAG instructions

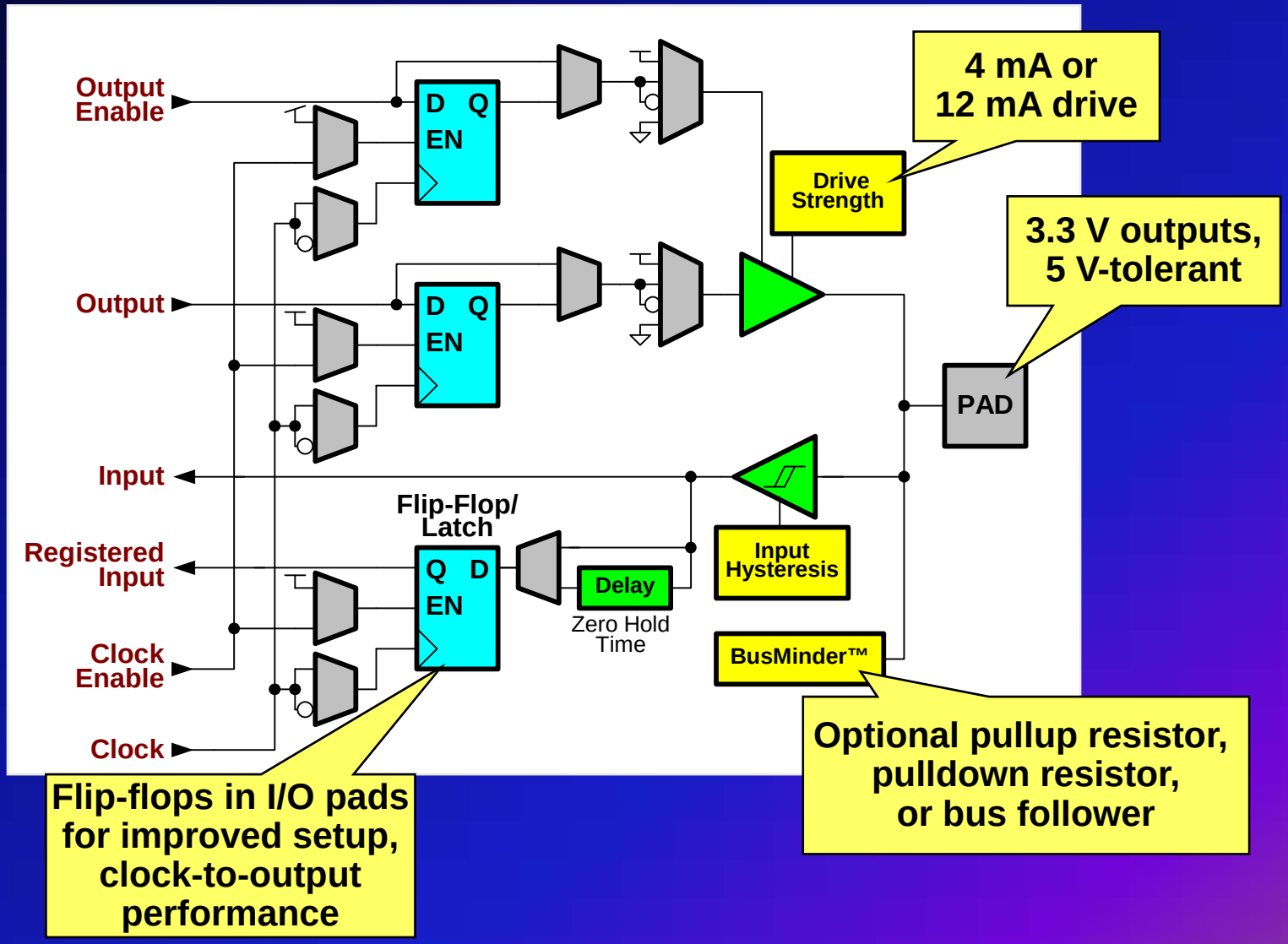
Breakpoint unit snoops the internal bus, providing complex runtime control features

All sequential and combinatorial logic nodes have complete observability

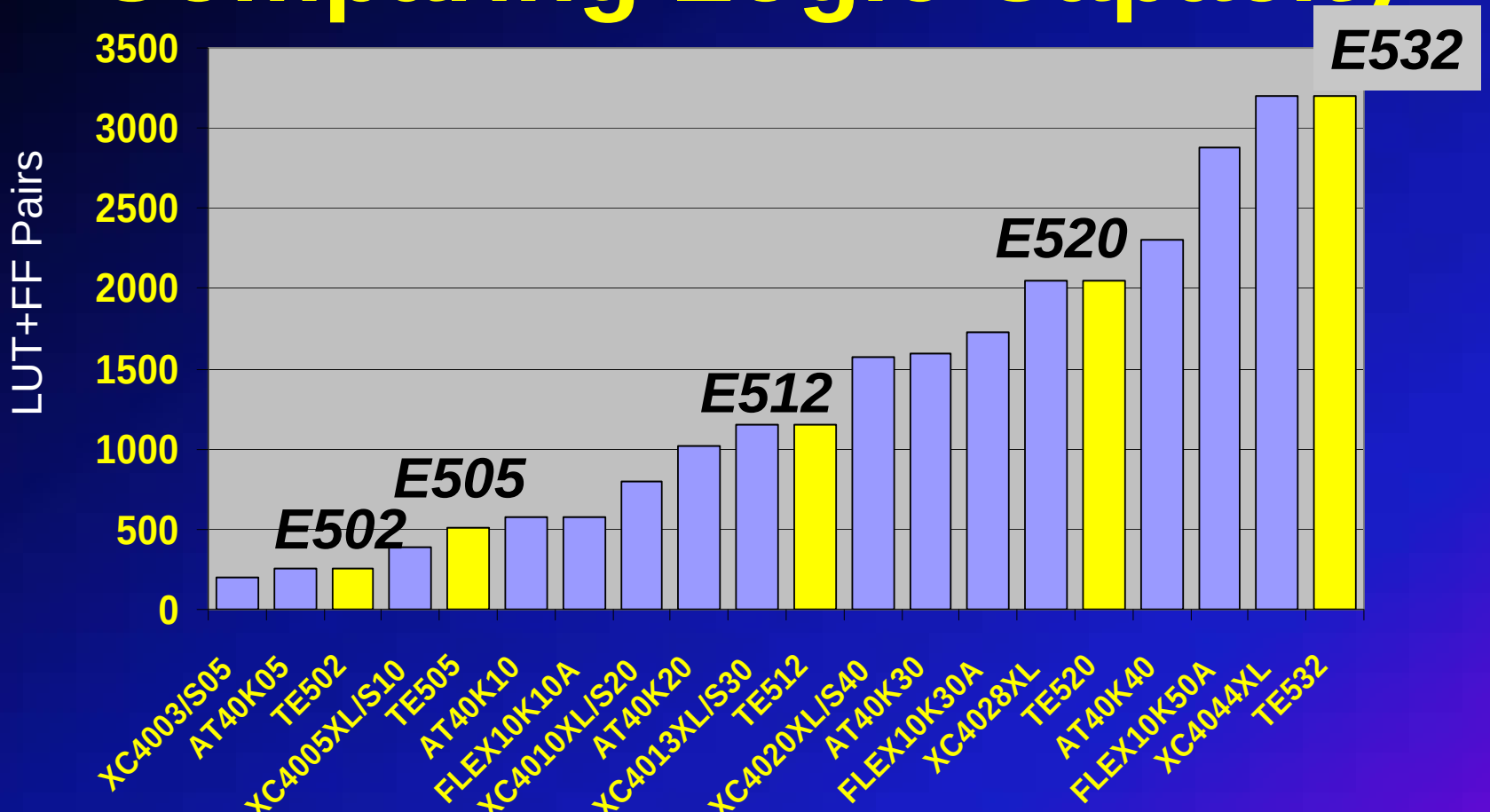
For More Information



Programmable I/O (PIO)



Comparing Logic Capacity



- Triscend CSL cell = 1 LUT4+FF pair
- Xilinx CLB = 2 LUT4+FF pair
- Altera FLEX LE = 1 LUT4+FF pair
- Atmel logic cell = 1 LUT4+FF pair