Using the Triscend LiteLoader™ Software

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Introduction

The Triscend LiteLoader™ is a set of ANSI-C software routines that allow a host processor to program a Triscend E5 CSoC device, in system, via a bit-banged JTAG interface. As illustrated in Figure 1, LiteLoader either directly programs an E5 device or downloads a configuration image to an external Flash or serial PROM connected to the E5's Memory Interface Unit (MIU).

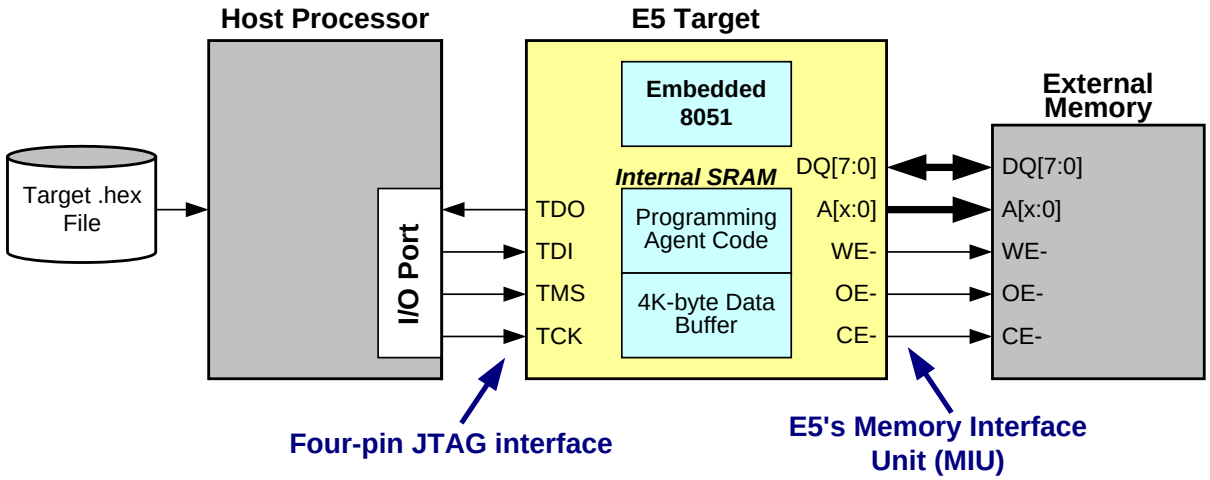

Figure 1. LiteLoader either directly programs an E5 device or downloads the E5 initialization data to an external memory connected to the E5's Memory Interface Unit (MIU).

The host processor is some type of intelligent host. It can be another processor or microcontroller in the same system or be an external host like a piece of automated test equipment (ATE) or even a personal computer or handheld computer. In the design example provided, the host processor is another E5 CSoC device.

There is no need to separately compile or modify LiteLoader if using a PC as the intelligent host. Simply use the Triscend FastChip Device Link (FDL) graphical interface or the **`csoc download`** command-line function.

The following is a partial list of potential LiteLoader applications.

- A method to configure a stand-alone E5 device that does not have another initialization source. In these types of applications, there is no Flash or serial PROM connected to the E5's MIU interface. Almost all of the MIU pins would be available to the application as user PIO pins.
- A convenient method to update hardware and software images, either remotely or in the field, without consuming other E5 hardware resources.
- A method to download and execute test functions on an E5 device mounted on the application board via automated test equipment (ATE). The test program running on the E5 device offloads time-consuming or complex tests from the ATE equipment. At the end of the test, the ATE equipment can monitor the status of the test. If the test were successful, the ATE

equipment would then download and program the Flash device connected to the E5 with the latest production release of the hardware and software image.

Host Processor Requirements

The host-side requirements are fairly minimal, as shown below. The communication channel between the host processor and the E5 Target is via a four-line JTAG interface. The LiteLoader code implements a JTAG TAP (Test Access Port) controller in software, via a bit-banged interface.

- Three addressable output port pins (TCK, TMS, TDI)
- One addressable input port pin (TDO)
- The host processor is supported by an ANSI-C compiler
- Ability to access the raw Hex file data to download to the E5 Target device.

In the provided design example, the host E5 device implements a memory-mapped I/O port using Configurable System Logic (CSL) and Programmable Input/Output (PIO) resources. The I/O register is assigned in memory by FastChip using the symbolic address, regJtagTap. The bit definitions for the JTAG interface signals are shown below.

Register Name: `regJtagTap`

	7	*6*	*5*	*4*	*3*	*2*	*1*	*0*
Read	—	—	—	—	TDO	TDI	TMS	TCK
Write	—	—	—	—		TDI	TMS	TCK

Supported Target E5 Download Methods

The LiteLoader program downloads initialization code for the Target E5 to a variety of memory types, as shown below.

- Directly to the Target E5's internal SRAM (download Agent not required)
- External byte-wide Flash memory connected via the Target E5's MIU interface.
- External, in-system programmable serial PROM (Atmel AT17-series) memory connected via the Target E5's MIU interface.
- External byte-wide SRAM memory connected via the Target E5's MIU interface.

LiteLoader Download Process

Access to Target Hex File

The data for the E5 Target is saved somewhere as an Intel Hex file. It could be stored in Flash memory, stored on a disk, or received via some other communications channel. The specific storage mechanism does not matter. The Hex image is created using the normal FastChip Device Link (FDL) or **`csoc config`** configuration flow.

Download Software Agent to Target E5 Device

The host begins the download process by first downloading a software Agent to the E5 Target device and starts it running. This Agent handles the low-level programming of any external memory. The Agent executes standard 8051 code which is downloaded and executed from the Target E5's internal SRAM memory. The Agent receives data from the host processor in 4K-byte buffer, again

implemented using the Target E5's internal SRAM. Similarly, the host is able to determine the status of the Agent via the JTAG interface.

The host processor then downloads the Flash or Serial PROM (SPROM) algorithm that was previously specified in a data file. The host then sends the Agent a command to erase the external Flash or serial PROM.

Erase External Memory

The Agent, executing on the Target E5 device, then erases the external memory using the appropriate algorithm, verifies that the external memory was actually erased, and reports status via a register queried by the host processor over JTAG.

Download Hex File Data and Program External Memory

Upon receiving confirmation that the external memory was erased, the host processor downloads the Target Hex image to the Target E5 device. Because the entire Hex image is too big to fit into the Target E5's internal SRAM, the host processor downloads the Hex file in 4K-byte blocks, which are temporarily stored in the Target E5's internal SRAM. After sending a block of data, the host processor issues a command to the Agent to program external memory. This process continues until the entire image is downloaded.

The Agent executing on the Target E5 device then programs the external memory upon receiving each program command from the host. The Agent also verifies that the data was correctly programmed into external memory.

Reset Target E5 CSoC Device, Load New Initialization Data

After receiving confirmation that the entire image was downloaded and programmed into external memory, the host processor issues a CSoC Reset command to the Target E5 device via JTAG. The CSoC Reset command is equivalent to asserting the RST- pin on the Target E5 device. On the E5 family, this command is only available via the JTAG interface. The CSoC Reset command forces the Target E5 device to re-initialize itself, booting from external Flash or SPROM. The Target E5 then loads its new configuration data and application code and then begins to execute the new function.

The Target HEX image that is created is then loaded through the Target E5 into FLASH, Serial EEPROM or External RAM (make flash, make SEEPROM, make extsram are the commands used to format the data). The parameters of the memory device to be programmed on the Target E5 board are specified in the respective .DAT files, and can be modified as required.

Example Design

The LiteLoader™ design example includes a FastChip project, called FCJtagTap, that implements a bit-banged JTAG interface using a Triscend E5 CSoC device as the host processor. As defined in the Makefile, the created JTAG controller is loaded into CSL and then executes the LiteLoader™ Master Download software from the external RAM on the E5 Development board.

The Target Download Agent is the application code for the Target E5 that is downloaded to the Target E5 by the Master Download software.

LiteLoader™ File structure

FCJtagTap — FastChip Project Directory

Hex — HEX File Directory

_Flash.dat	Flash device parameter file
_seeprom.dat	SEEPROM device parameter file
_ExtSram.dat	External SRAM device parameter file
Makefile	Cygwin Makefile used to build the download.hex file, download.cfg file and download to the Master E5 board or download the demo example to the host E5 board

Demonstration Examples

Dncounter.ext.hex	Down Counter demo for External SRAM
Dncounter.internal.hex	Down Counter demo for Internal SRAM
Dncounter.seeprom.hex	Down Counter demo for SEEPROM
Upcounter.ext.hex	Up Counter demo for External SRAM
Upcounter.seeprom.hex	Up Counter demo for SEEPROM
Mydesign.seeprom.hex	Mydesign demo for SEEPROM

Keil — JtagTap Output Directory

JtagTap	
JtagTap.hex	Master HEX file
JtagTap.m51	
JtagTap.prj	

Src — LiteLoader™ C Source Directory

JtagTap.h	
Te5disp.h	
Te5dl.h	
Te5flash.h	Target Download Agent for Flash
Te5jtag.h	
Te5sprom.h	Target Download Agent for SEEPROM
Te5tap.h	
Te5types.h	Master data types
Te5utils.h	
JtagTap.c	Master Main
Te5disp.c	Master 7-segment Display Routines
Te5dl.c	Master Download Routines
Te5jtag.c	Master to Target JTAG Routines
Te5tap.c	Master TAP Software State Machine

Te5utils.c	Master Little/Big Endian Conversion Routines
e5flash.hex	Target Download Agent FLASH HEX file
e5seeprom.hex	Target Download Agent SEEPROM HEX file
HexSplitter.pl	Perl script used to split a single HEXFILE created by HexToDownload.pl into multiple hex files so that each output file only contains a range of addresses within 64K.
HexToDownloader.pl	Perl script used to combine the memory device '.dat' files, Master software and Target HEX image into the download.hex file.
HexToStruct.pl	Perl script to convert Flash and SEEPROM Target Download Agents to header files.

LiteLoader™ Instructions

1. Use FastChip Device Link (FDL) to create the Target HEX image by selecting the HEX output format.
2. Copy the resulting HEX file into the LiteLoader™ HEX directory.
3. Configure the appropriate device file for the memory device on the Target E5 board.
   - **_Flash.dat** — Flash device file
   - **_Seeprom.dat** — SEEPROM device file
   - **_ExtSram.dat** — External SRAM device file
4. With the appropriate *.dat file, configure the following variables.
   - **@IMAGES = ("**<Target HEX image>**.hex");**
   - $**MEMORY_CAP = **<Size of device in kilobytes (KB)>**;**
   - **$MEMORY_ALG = "**<Device name from support list>**";**
5. Run Makefile for the appropriate target
   - **make flash** — build for FLASH on the Target E5 board
   - **make seeprom** — build for SEEPROM on the Target E5 board
   - **make extsram** — build for External SRAM on the Target E5 board
   - **make demo** — download the demo examples to the Target E5 board

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Revision History

Revision	Date	Comment
1.0	JAN-2002	Initial release

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