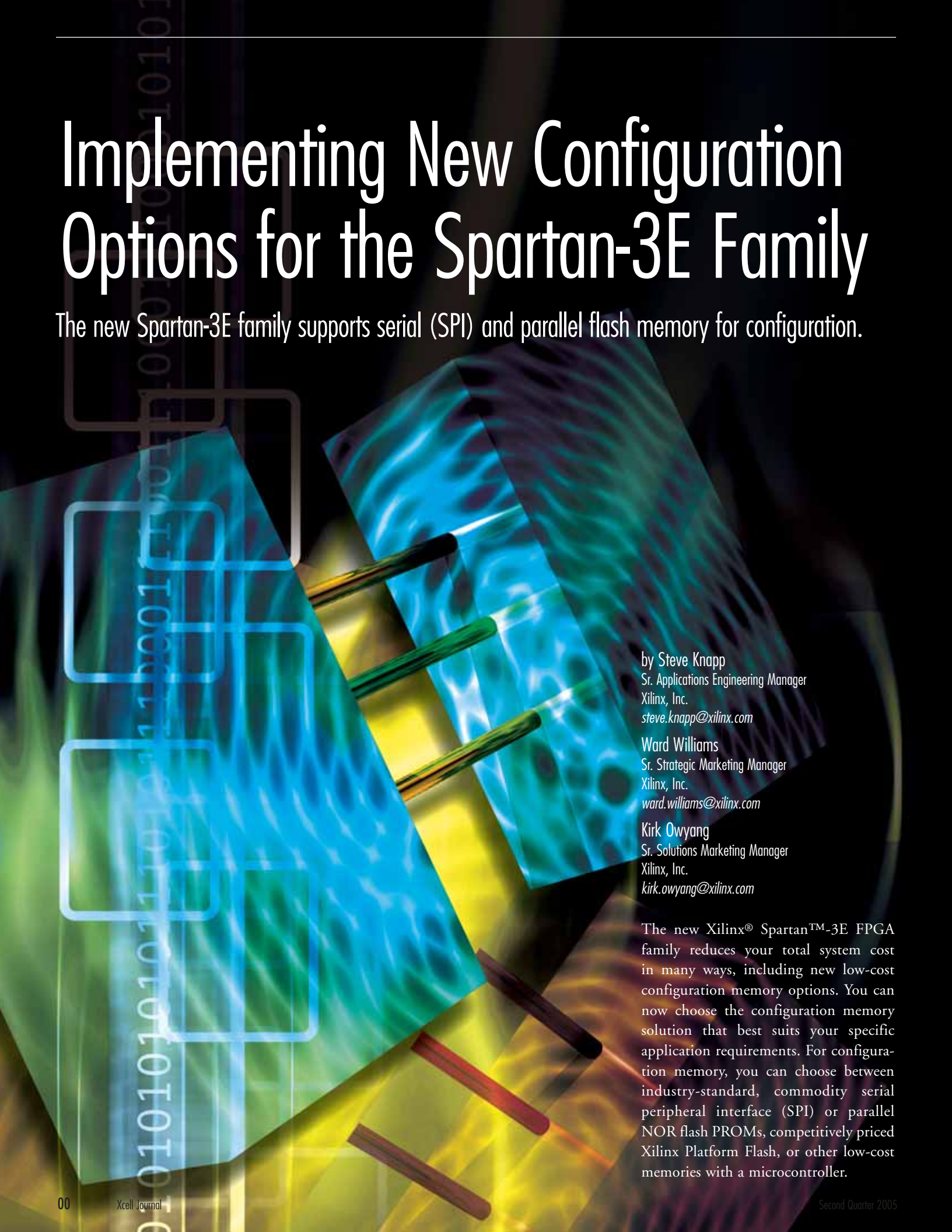
Implementing New Configuration Options for the Spartan-3E Family

The new Spartan-3E family supports serial (SPI) and parallel flash memory for configuration.



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The new Xilinx® Spartan™-3E FPGA family reduces your total system cost in many ways, including new low-cost configuration memory options. You can now choose the configuration memory solution that best suits your specific application requirements. For configuration memory, you can choose between industry-standard, commodity serial peripheral interface (SPI) or parallel NOR flash PROMs, competitively priced Xilinx Platform Flash, or other low-cost memories with a microcontroller.

Nearly all of the Spartan-3E configuration pins become available as user I/Os after configuration. Consequently, you can leverage any remaining space in the configuration memory for application data, such as code for an embedded MicroBlaze™ processor, serial numbers, or Ethernet MAC IDs. SPI and parallel flash PROMs additionally offer random-accessible, byte-addressable, read/write memory. If the application requires additional space, upgrade to the next larger PROM. Most SPI and parallel flash PROMs are available in a common footprint across multiple densities.

Xilinx Platform Flash still provides an excellent solution for stand-alone two-chip programmable logic solutions (FPGA + dedicated configuration PROM), with competitive cost-per-megabit pricing. Platform Flash also excels with features such as JTAG in-system programmability and patented compression technology.

SPI flash PROMs are popular in high-volume consumer electronics applications, where they store system parameters or code for an embedded processor. SPI flash PROMs also offer a low-cost pin-saving configuration solution for Spartan-3E FPGAs. SPI flash memory is multi-sourced and multiple densities are available within the same package footprint.

Parallel NOR flash is the preferred solution for FPGA applications with an embedded processor such as the MicroBlaze soft-core processor. At power-on, the FPGA configures from one end of the parallel flash. After configuration, the MicroBlaze processor either executes directly from the opposite end of memory or shadows the code to external SDRAM.

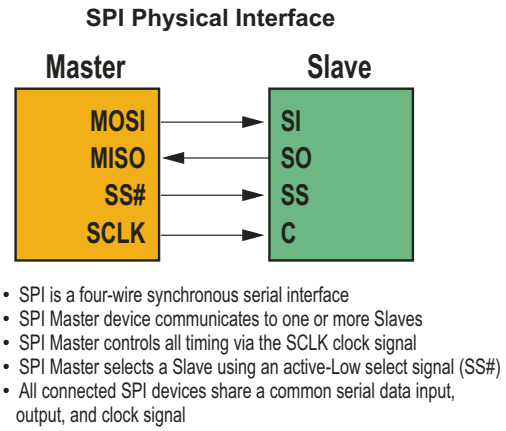

Figure 1 – SPI physical interface

SPI Serial Flash Vendor	Tested SPI Flash Family
Atmel	AT45DBxxx
NexFlash	NX25Pxx
Programmable Microelectronics Corporation (PMC)	Pm25LVxxx
Silicon Storage Technology (SST)	SST25LFxxxA SST25VFxxxA SST25VFxx *
ST Microelectronics	M25Pxx

** SST25VFxx supports only the READ (0X03) SPI read command; all others support the FAST_Read (0X0B) command.*

Table 1 – SPI flash memory families supported by Spartan-3E FPGAs

Spartan-3E Device	Configuration Bits	Minimum SPI Device Capacity	Unused Memory After Configuration
XC3S100E	581K	1 Mb	443K
XC3S250E	1,352K	2 Mb	696K
XC3S500E	2,267K	4 Mb	1,829K
XC3S1200E	3,832K	4 Mb	264K
XC3S1600E	5,958K	8 Mb	2,234K

Table 2 – Required SPI device sizes and estimated cost

What is SPI?

The serial peripheral interface (SPI) interface is a four-wire synchronous interface (Figure 1). SPI was originally pioneered as a serial communications interface between CPUs, MCUs, peripherals, and other devices supporting this protocol. Now SPI is popular in the embedded processing and consumer electronics markets. Many modern microcontrollers use this interface, as well as a wide variety of third-party peripherals.

SPI Flash Suppliers

Although SPI is a standard four-wire interface, the various available SPI flash PROMs use different command protocols. Spartan-3E FPGAs support up to four different command protocols. Currently, SPI flash PROMS from five vendors (Atmel, NexFlash, Programmable Microelectronics Corporation [PMC], Silicon Storage Technology [SST], and ST Microelectronics) are tested and supported, as shown in Table 1. Devices from other SPI suppliers are being tested and will be supported in the near future.

Memory Requirements

A single Spartan-3E FPGA requires roughly 600K to 6M bits for configuration, a small amount of memory relative to the large SPI capacities available today. Table 2 lists the amount of configuration memory required by each Spartan-3E device type, the minimum required SPI device size, and the extra memory that is available for other purposes. Note that it is not necessary to have a dedicated configuration memory device for each FPGA.

Multiple FPGAs can share a single SPI flash PROM in a configuration daisy chain.

Interfacing to SPI

Figure 2 shows the typical connections between a Spartan-3E FPGA and SPI flash memory, as well as the FPGA I/O pins used to control the configuration procedure. When the FPGA is in SPI flash configuration mode, three dual-pur-

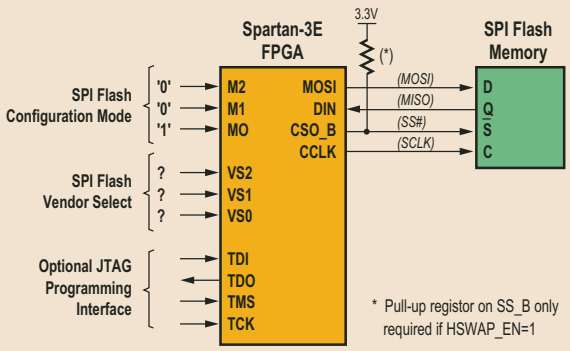

Figure 2 – Interface between Spartan-3E FPGA and SPI flash memory

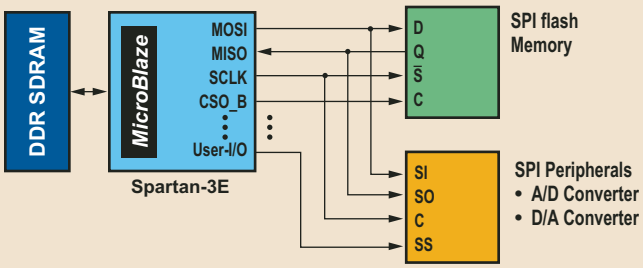

Figure 3 – Connecting SPI flash memory to multiple devices

pose pins, called VS[2:0], define the type of attached SPI flash and operate as follows:

- These pins are only activated in SPI configuration mode (M[2:0]="001")
- The VS pins are sampled when INIT_B goes high
- The VS pins are reusable as user I/O after FPGA configuration completes (DONE goes high)

Then, the FPGA issues the command sequence appropriate for the selected SPI flash.

After Configuration

After configuration, all of the pins connected to the SPI flash PROM are available as user I/O pins. If not using the SPI flash PROM after configuration, drive the FPGA's CSO_B pin high to disable the PROM, freeing the FPGA's MOSI, DIN, and CCLK pins as user I/O.

If large enough, the SPI flash PROM can also contain non-volatile application data, such as MicroBlaze processor code or data such as serial numbers and Ethernet MAC IDs. Figure 3 shows an example of using SPI flash memory for multiple purposes.

Third-Party Peripherals

In addition to flash memory, many peripherals utilize the same SPI. These include:

- Memories (EEPROM, EPROM)
- Analog-to-digital converters (ADCs)
- Digital-to-analog converters (DACs)
- Thermal management
- Display drivers
- Microprocessors, microcontrollers (MCUs), and digital signal processors (DSPs)
- Many application-specific standard products (ASSPs)

After configuration, the FPGA user application can remain as the SPI bus master and communicate with the attached SPI flash PROM and any attached SPI peripherals. All of the attached SPI peripherals share common serial-input, serial-output, and clock signals. Each SPI peripheral has a separate select input. The SPI flash PROM used for configuration is selected through the FPGA's CSO_B pin. Each additional SPI peripheral is selected by a separate user I/O pin.

Parallel NOR Flash

Spartan-3E FPGAs also provide a parallel configuration interface, primarily designed to configure the FPGA from industry-standard parallel NOR flash. The FPGA's asynchronous memory interface is flexible and can connect to a variety of memory devices such as EEPROM, OTP EPROM, masked ROM, NVRAM, or even asynchronous SRAM.

The memory requirements are fairly simple. During configuration, the FPGA provides up to 24 address lines and receives byte-wide data. The FPGA has four control lines driving the memory's chip-select, output-enable, write-enable, and an optional byte-enable for high-density flash PROMs with a x8/x16 mode control (BYTE#). The memory must be 3.3V, 2.5V, or 1.8V and must have a read access time of 200 ns or faster.

Conclusion

In addition to low device costs, the new low-cost Spartan-3E FPGA family lowers overall system cost in many ways, including new support for inexpensive SPI and parallel flash memory for configuration. Currently, a number of flash memory families are supported and more memory vendors will announce their support for Spartan-3E devices in the coming months. Please check the Spartan-3E pages on the Xilinx website for a current list of supported SPI flash, *www.xilinx.com/spartan3e/.*